

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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Keep safety first in your circuit designs!

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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# 2SK2912(L), 2SK2912(S)

Silicon N Channel MOS FET  
High Speed Power Switching

**RENESAS**

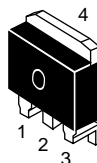
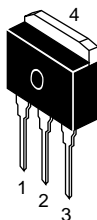
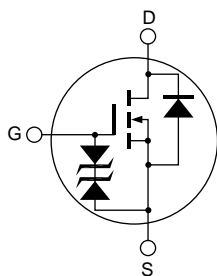
ADE-208-495A (Z)  
1st. Edition  
Mar. 2001

## Features

- Low on-resistance  
 $R_{DS} = 15 \text{ m}\Omega$  typ.
- High speed switching
- 4V gate drive device can be driven from 5V source

## Outline

LDBPAK



1. Gate
2. Drain
3. Source
4. Drain

## 2SK2912(L), 2SK2912(S)

### Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	60	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	40	A
Drain peak current	$I_{D(pulse)}^{*1}$	160	A
Body to drain diode reverse drain current	$I_{DR}$	40	A
Avalanche current	$I_{AP}^{*3}$	40	A
Avalanche Energy	$E_{AR}^{*3}$	137	mJ
Channel dissipation	$P_{ch}^{*2}$	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

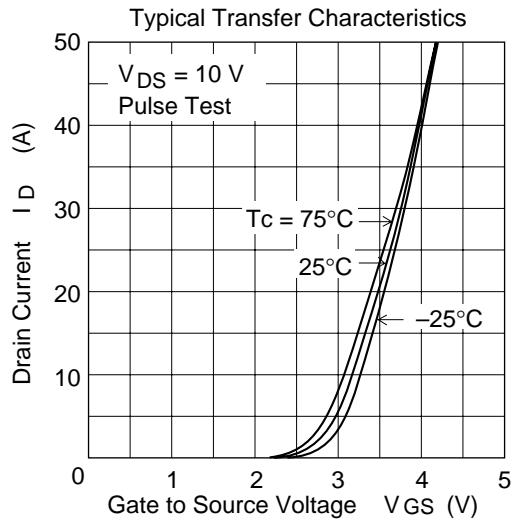
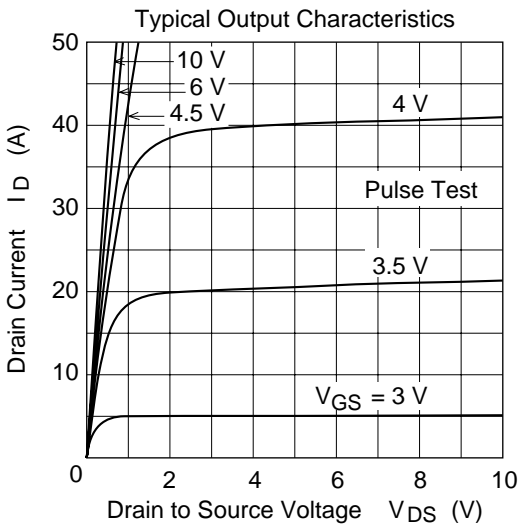
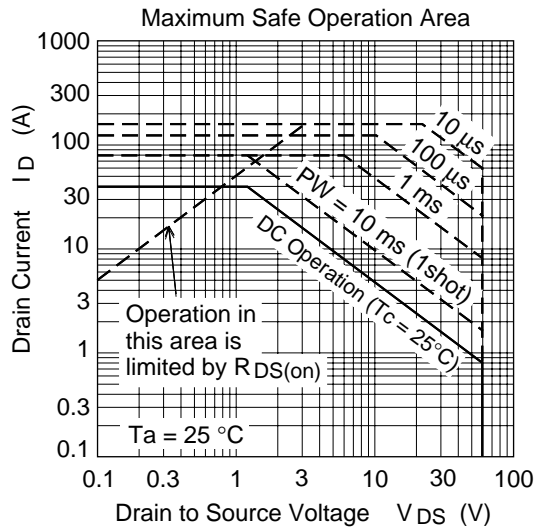
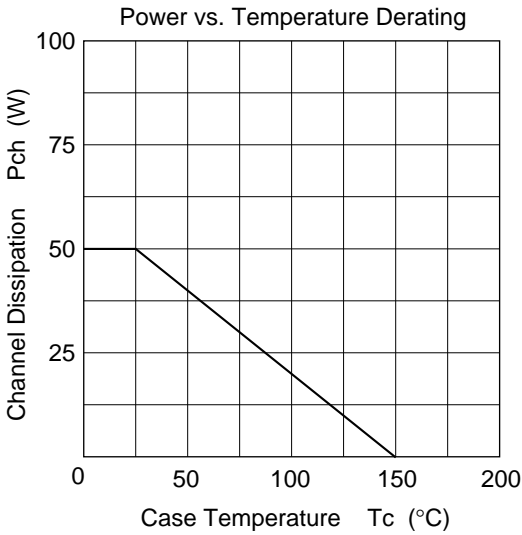
- Notes: 1.  $PW \leq 10\mu s$ , duty cycle  $\leq 1\%$   
2. Value at  $T_c = 25^\circ C$   
3. Value at  $T_{ch} = 25^\circ C$ ,  $R_g \geq 50 \Omega$

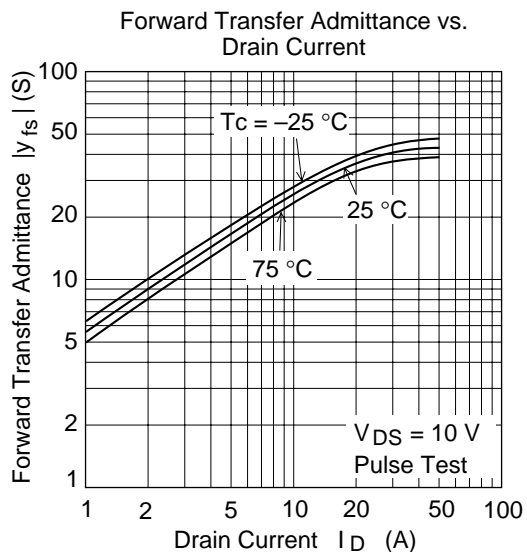
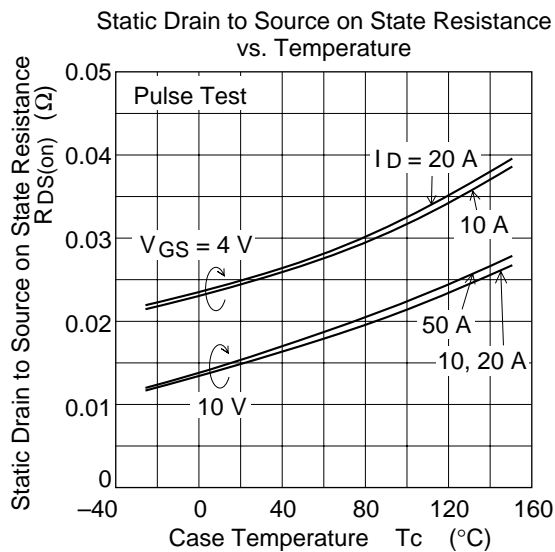
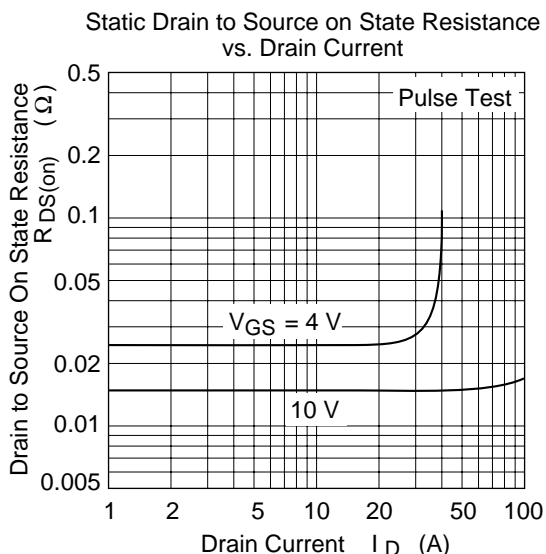
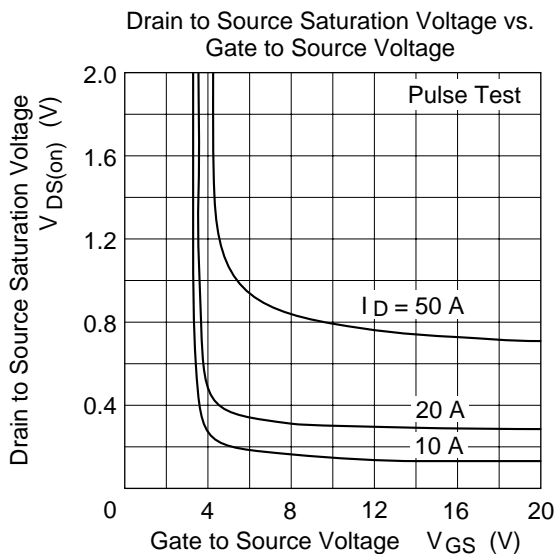
## Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10mA, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = ±100μA, V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±10	μA	$V_{GS} = ±16V, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	μA	$V_{DS} = 60V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	$I_D = 1mA, V_{DS} = 10V$
Static drain to source on state resistance	$R_{DS(on)}$	—	15	20	mΩ	$I_D = 20A, V_{GS} = 10V^{*1}$
	$R_{DS(on)}$	—	25	40	mΩ	$I_D = 20A, V_{GS} = 4V^{*1}$
Forward transfer admittance	$ y_{fs} $	20	35	—	S	$I_D = 20A, V_{DS} = 10V^{*1}$
Input capacitance	$C_{iss}$	—	1500	—	pF	$V_{DS} = 10V$
Output capacitance	$C_{oss}$	—	720	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	200	—	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$I_D = 20A, V_{GS} = 10V$
Rise time	$t_r$	—	180	—	ns	$R_L = 1.5Ω$
Turn-off delay time	$t_{d(off)}$	—	200	—	ns	
Fall time	$t_f$	—	200	—	ns	
Body to drain diode forward voltage	$V_{DF}$	—	0.95	—	V	$I_F = 40A, V_{GS} = 0$
Body to drain diode reverse recovery time	$t_{rr}$	—	70	—	V	$I_F = 40A, V_{GS} = 0$ $diF/dt = 50A/μs$

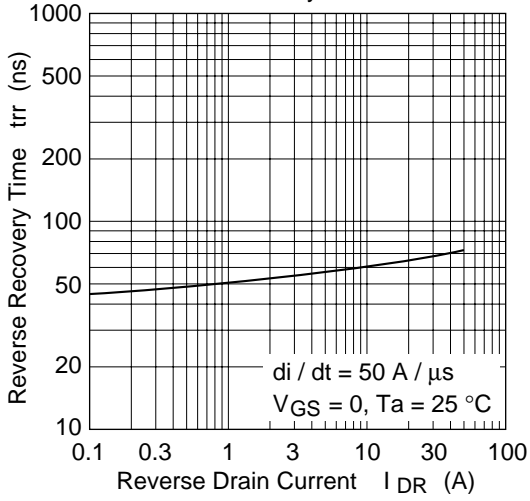
Note: 1. Pulse test

Main Characteristics

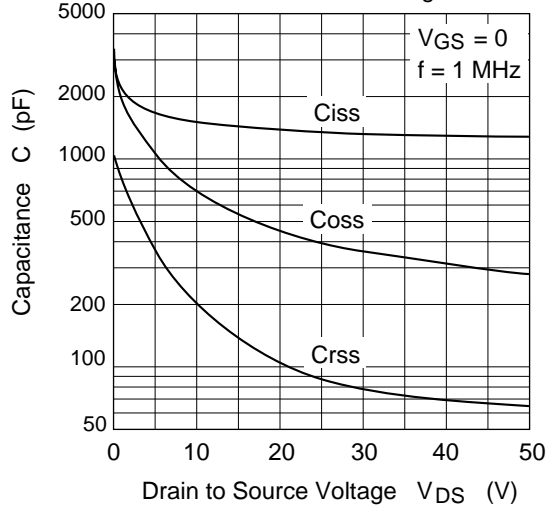




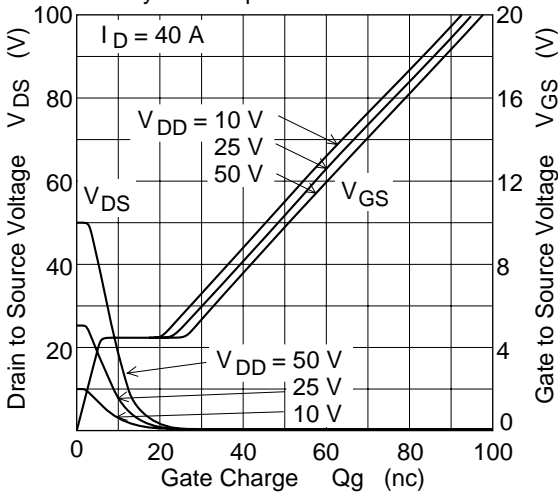
Body to Drain Diode Reverse Recovery Time



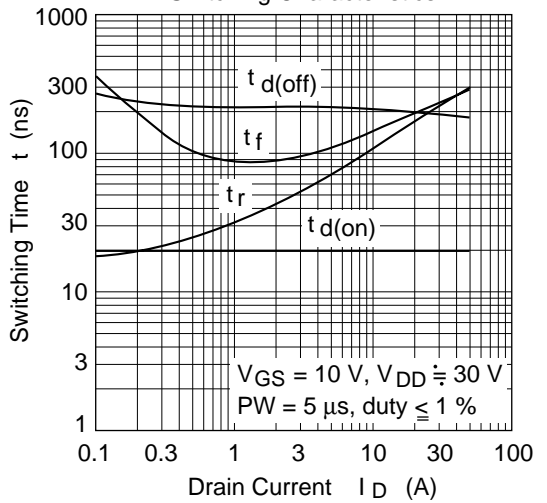
Typical Capacitance vs. Drain to Source Voltage

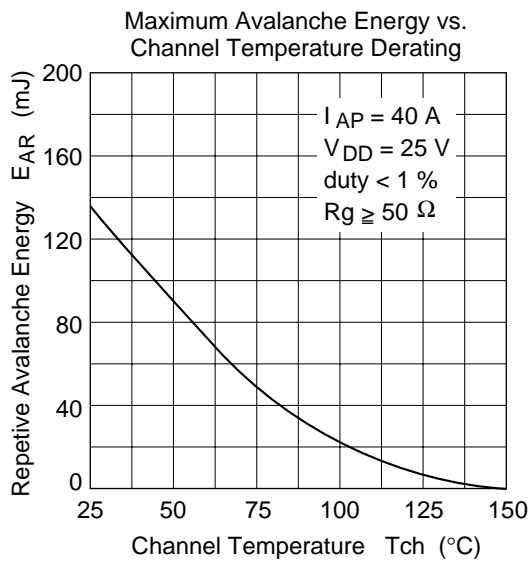
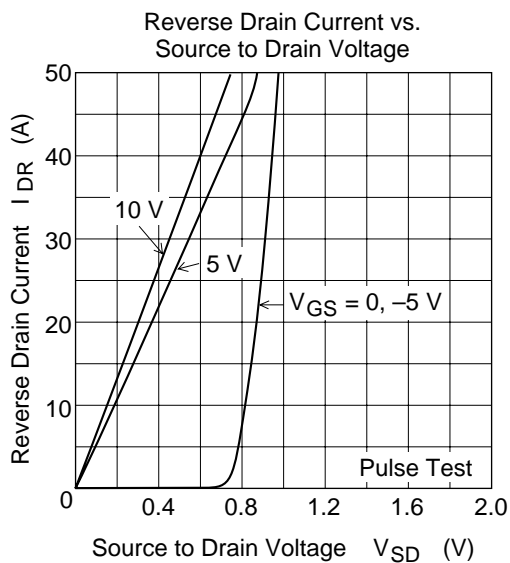


Dynamic Input Characteristics

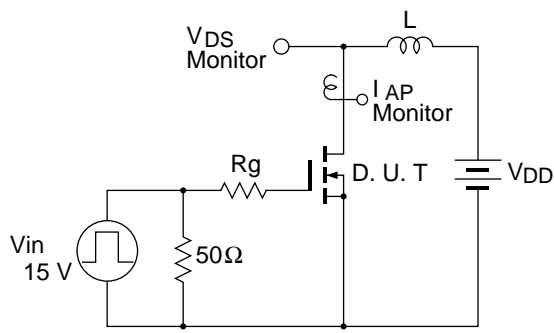


Switching Characteristics

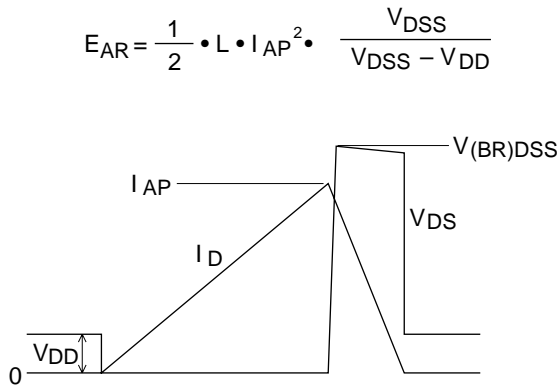




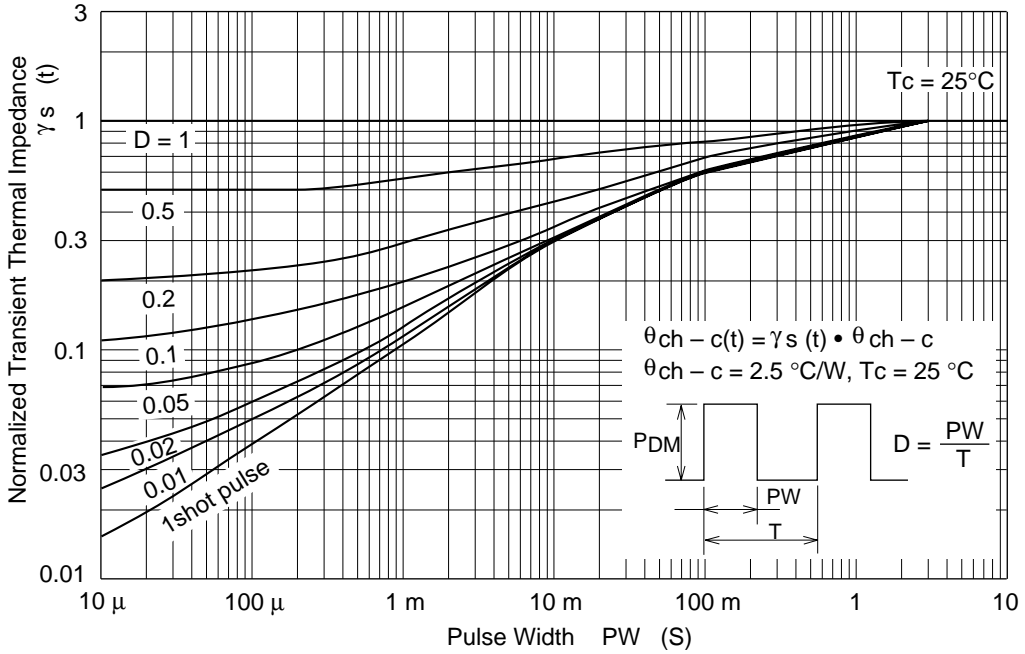
Avalanche Test Circuit



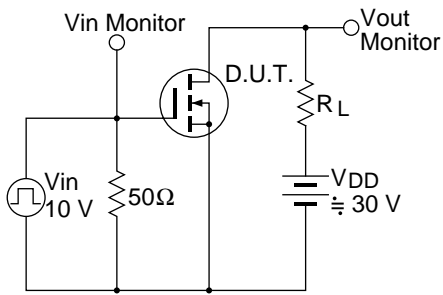
Avalanche Waveform



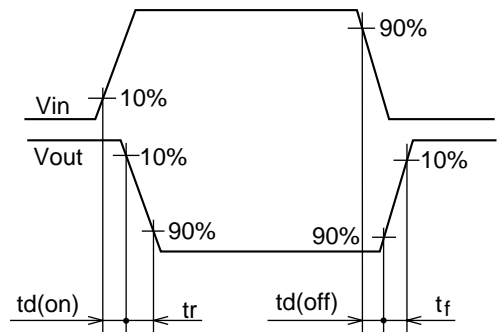
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

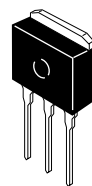
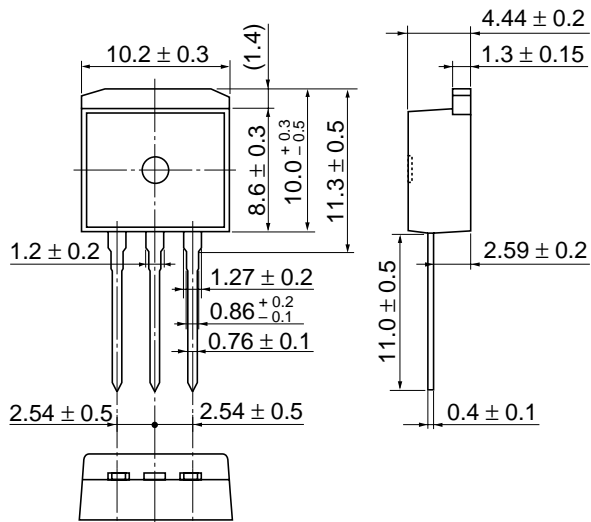


Switching Time Waveforms



Package Dimensions

As of January, 2001  
Unit: mm

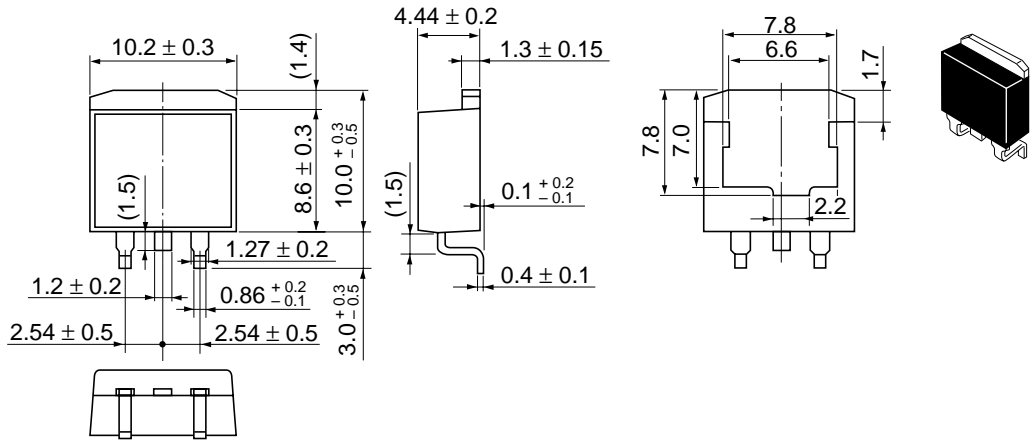


Hitachi Code	LDBAK (L)
JEDEC	—
EIAJ	—
Mass (reference value)	1.4 g

# 2SK2912(L), 2SK2912(S)

As of January, 2001

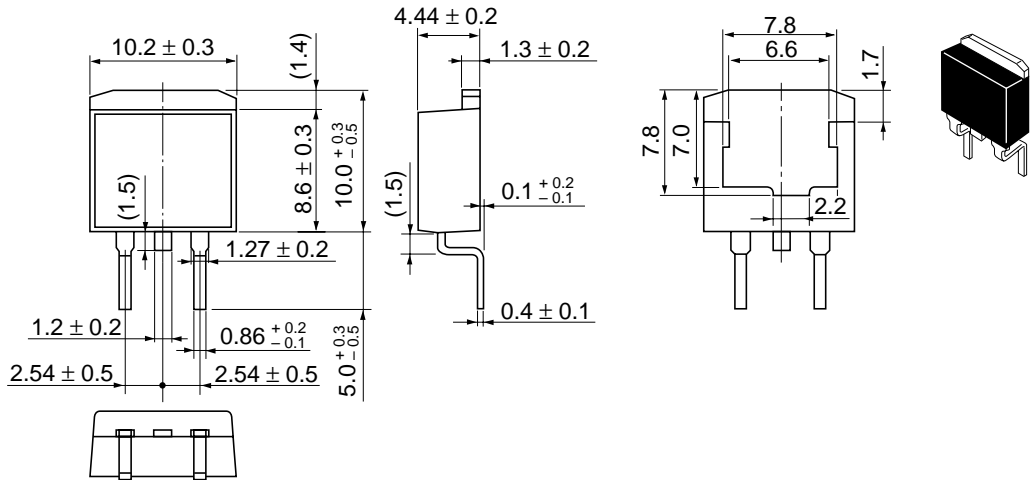
Unit: mm



Hitachi Code	LDPAK (S)-(1)
JEDEC	—
EIAJ	—
Mass (reference value)	1.3 g

As of January, 2001

Unit: mm



Hitachi Code	LDBAK (S)-(2)
JEDEC	—
EIAJ	—
Mass (reference value)	1.35 g

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