

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (L²-π-MOSV)

2SK2745

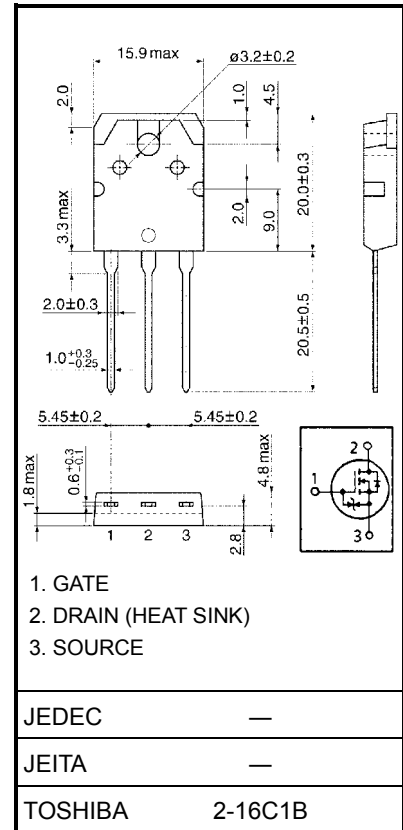
Chopper Regulator, DC-DC Converter and Motor Drive Applications

Unit: mm

- 4 V gate drive
- Low drain-source ON resistance : $R_{DS(ON)} = 7.0 \text{ m}\Omega$ (typ.)
- High forward transfer admittance : $|Y_{fs}| = 50 \text{ S}$ (typ.)
- Low leakage current : $I_{DSS} = 100 \text{ }\mu\text{A}$ (max) ($V_{DS} = 50 \text{ V}$)
- Enhancement-mode : $V_{th} = 0.8\sim 2.0 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$)

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	50	V
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)	V_{DGR}	50	V
Gate-source voltage	V_{GSS}	± 20	V
Drain current	DC (Note 1)	I_D	50
	Pulse (Note 1)	I_{DP}	200
Drain power dissipation ($T_c = 25^\circ\text{C}$)	P_D	150	W
Single pulse avalanche energy (Note 2)	E_{AS}	747	mJ
Avalanche current	I_{AR}	50	A
Repetitive avalanche energy (Note 3)	E_{AR}	15	mJ
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	-55~150	°C



Weight: 4.6 g (typ.)

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	0.833	°C / W
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	50	°C / W

Note 1: Please use devices on condition that the channel temperature is below 150°C.

Note 2: $V_{DD} = 25 \text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 368 \text{ }\mu\text{H}$, $R_G = 25 \text{ }\Omega$, $I_{AR} = 50 \text{ A}$

Note 3: Repetitive rating: Pulse width limited by maximum channel temperature

This transistor is an electrostatic sensitive device.
Please handle with caution.

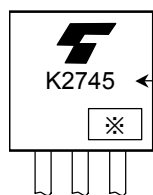
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 10	μA
Drain cut-off current		I_{DSS}	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	50	—	—	V
Gate threshold voltage		V_{th}	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	0.8	—	2.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = 4\text{ V}, I_D = 25\text{ A}$	—	11	16	m Ω
			$V_{GS} = 10\text{ V}, I_D = 25\text{ A}$	—	7	9.5	
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 25\text{ A}$	30	50	—	S
Input capacitance		C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	4000	—	pF
Reverse transfer capacitance		C_{rss}		—	800	—	
Output capacitance		C_{oss}		—	2000	—	
Switching time	Rise time	t_r		—	25	—	ns
	Turn-on time	t_{on}		—	40	—	
	Fall time	t_f		—	120	—	
	Turn-off time	t_{off}		—	360	—	
Total gate charge (gate-source plus gate-drain)		Q_g	$V_{DD} \approx 40\text{ V}, V_{GS} = 10\text{ V}, I_D = 50\text{ A}$	—	130	—	nC
Gate-source charge		Q_{gs}		—	90	—	
Gate-drain ("miller") Charge		Q_{gd}		—	40	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	50	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	200	A
Forward voltage (diode)	V_{DSF}	$I_{DR} = 50\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.7	V
Reverse recovery time	t_{rr}	$I_{DR} = 50\text{ A}, V_{GS} = 0\text{ V}, dI_{DR}/dt = 50\text{ A}/\mu\text{s}$	—	140	—	ns
Reverse recovery charge	Q_{rr}		—	80	—	μC

Marking

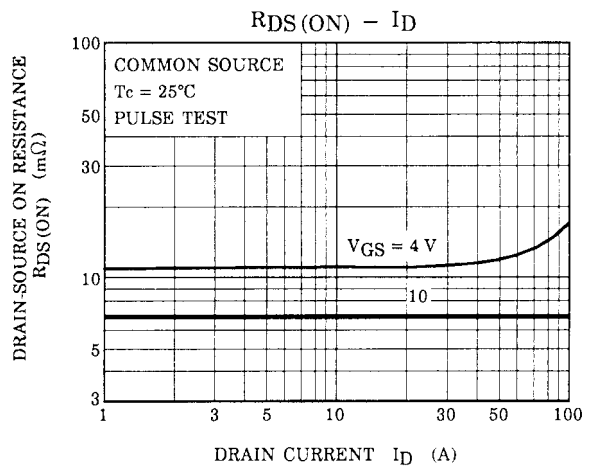
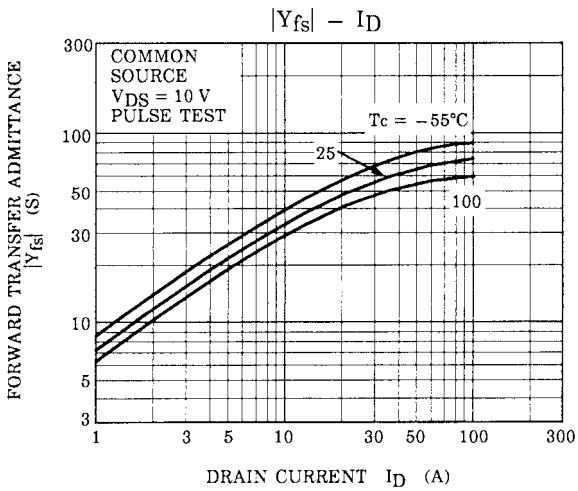
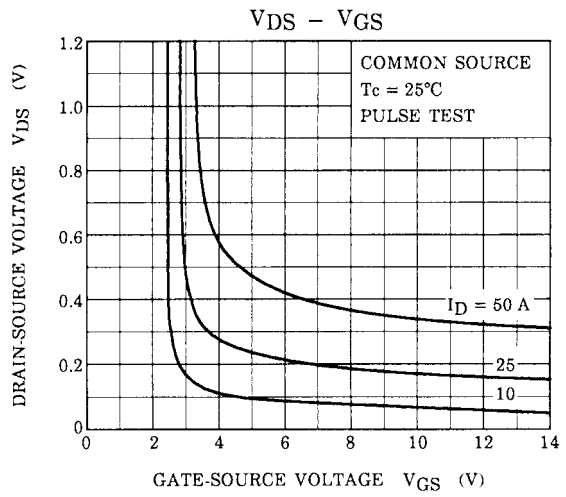
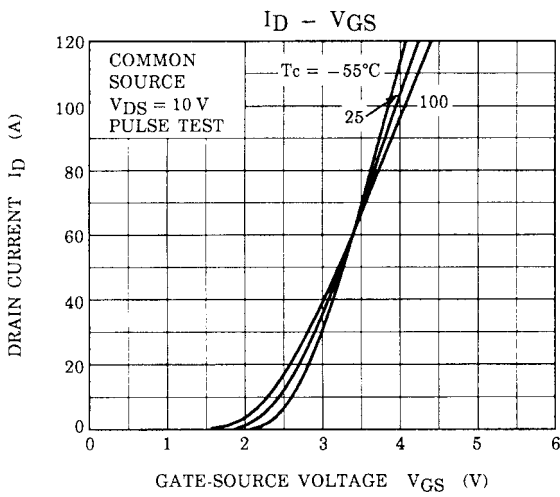
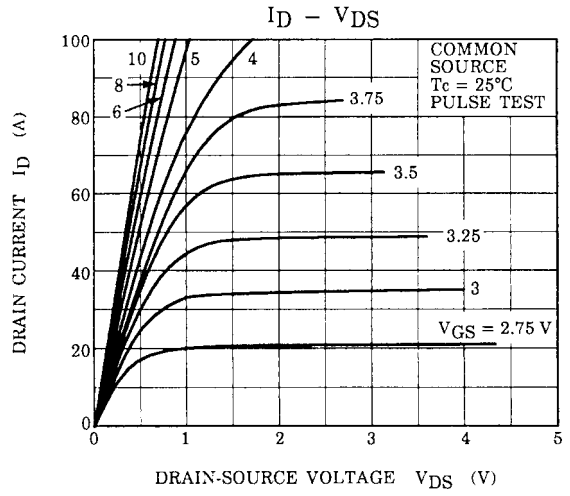
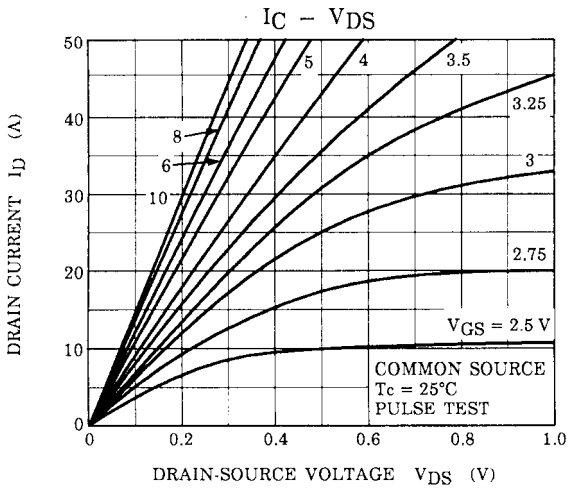


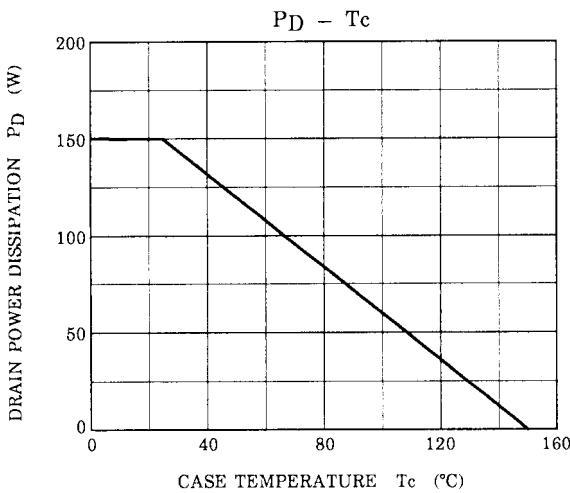
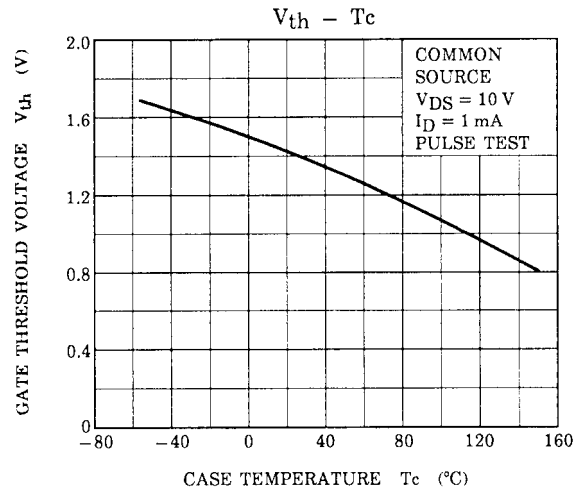
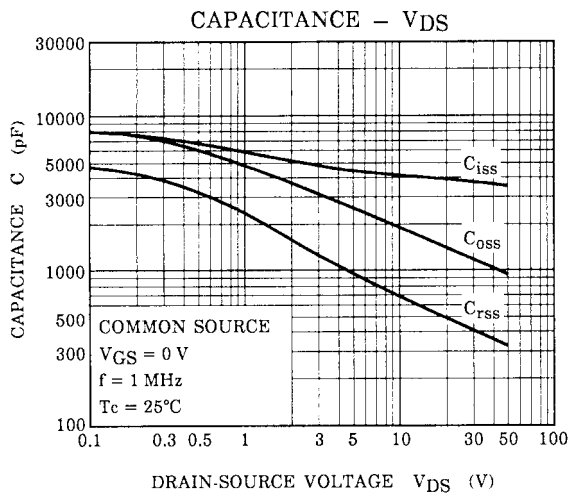
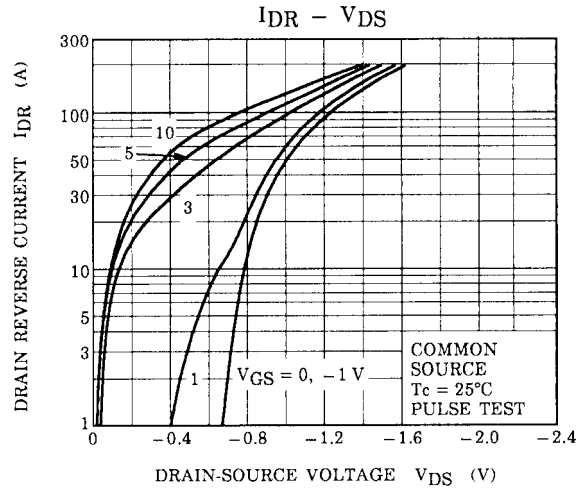
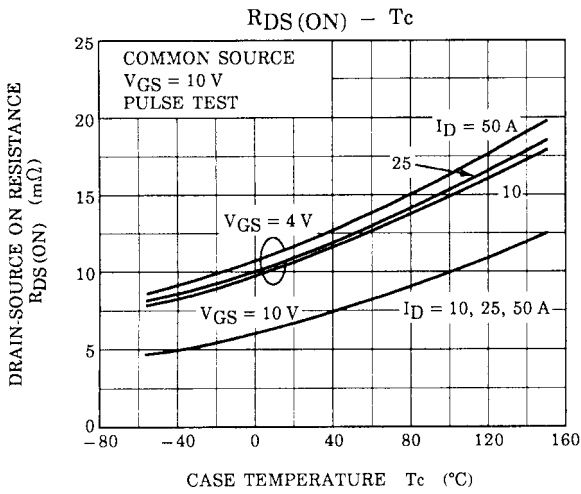
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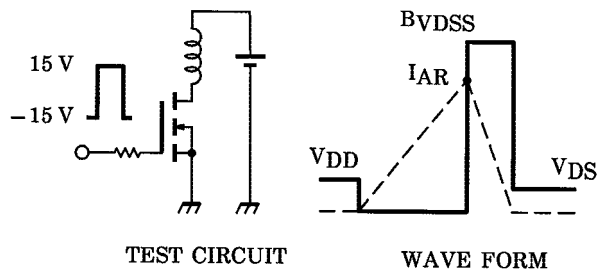
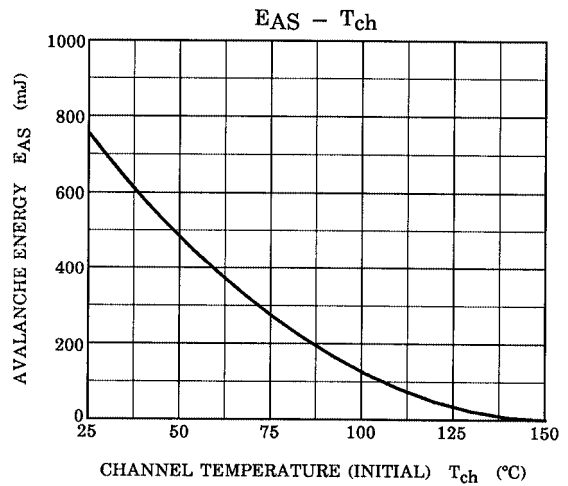
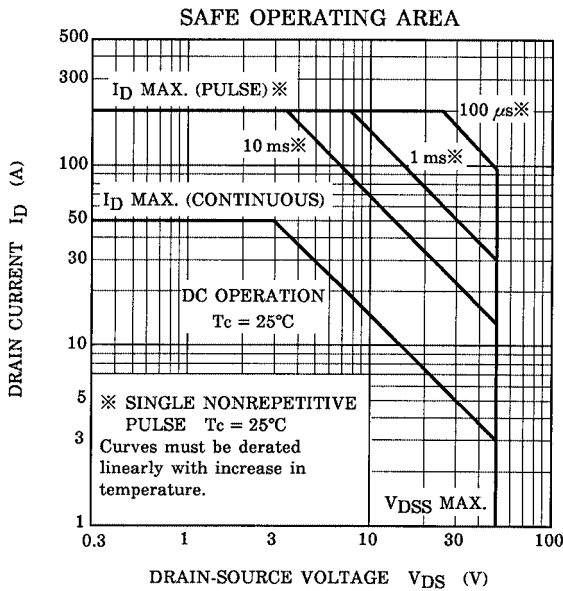
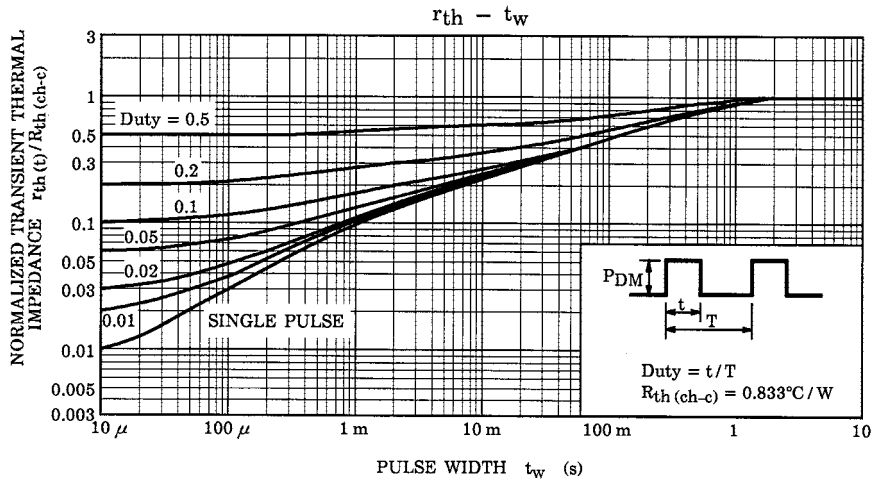
※ Lot Number

□ □ — Month (starting from alphabet A)

□ — Year (last number of the christian era)







$R_G = 25 \Omega$
 $V_{DD} = 25 \text{ V}, L = 368 \mu\text{H}$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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