

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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# 2SK2553(L), 2SK2553(S)

Silicon N Channel MOS FET  
High Speed Power Switching

**RENESAS**

ADE-208-357H (Z)  
9th. Edition  
Feb. 1999

## Application

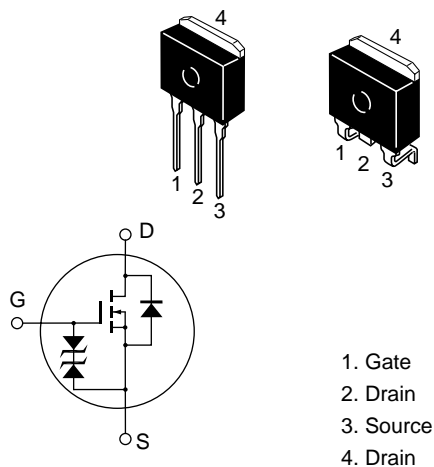
High speed power switching

## Features

- Low on-resistance
- $R_{DS(on)} = 7 \text{ m}\Omega$  typ.
- High speed switching
- 4 V gate drive device can be driven from 5 V source

## Outline

LDDPAK



**Absolute Maximum Ratings** ( $T_a = 25^\circ\text{C}$ )

<b>Item</b>	<b>Symbol</b>	<b>Ratings</b>	<b>Unit</b>
Drain to source voltage	$V_{DSS}$	60	V
Gate to source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	$I_D$	50	A
Drain peak current	$I_{D(pulse)}$ <sup>Note 1</sup>	200	A
Body to drain diode reverse drain current	$I_{DR}$	50	A
Avalanche current	$I_{AP}$ <sup>Note 3</sup>	45	A
Avalanche energy	$E_{AR}$ <sup>Note 3</sup>	174	mJ
Channel dissipation	$P_{ch}$ <sup>Note 2</sup>	75	W
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

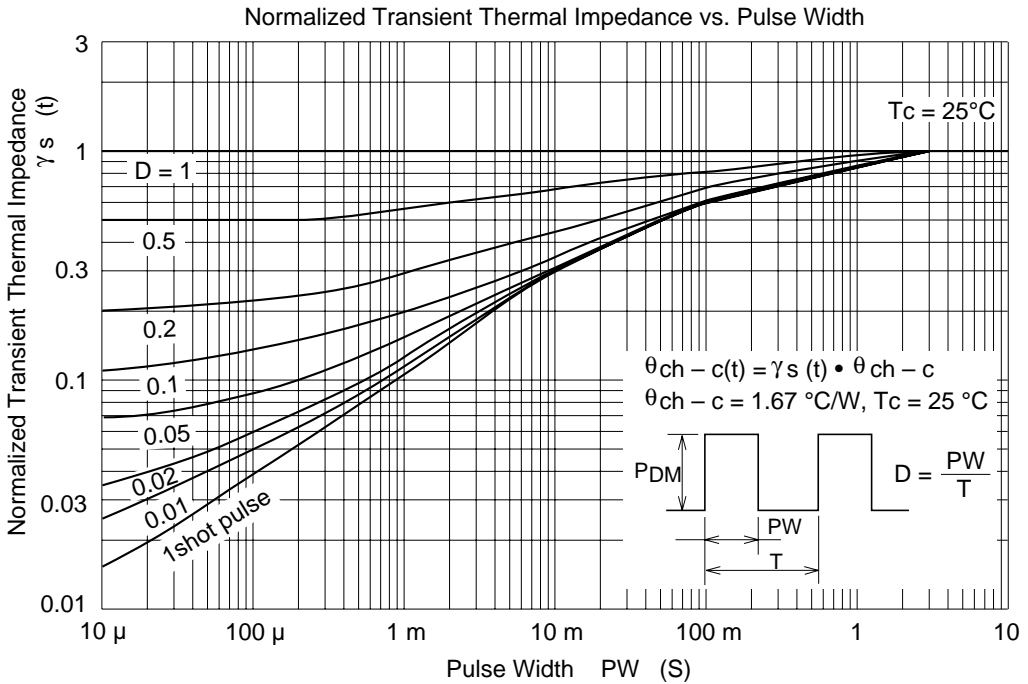
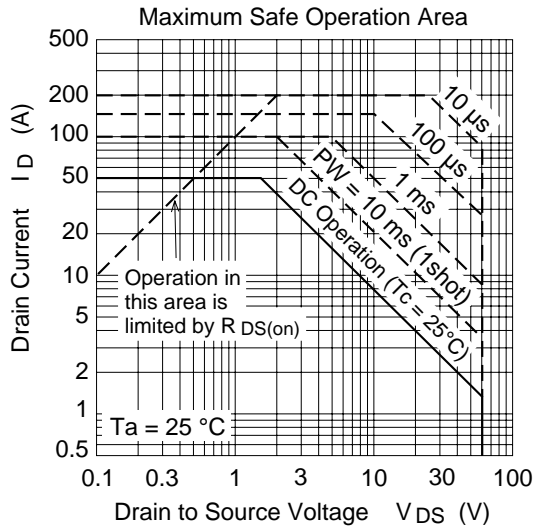
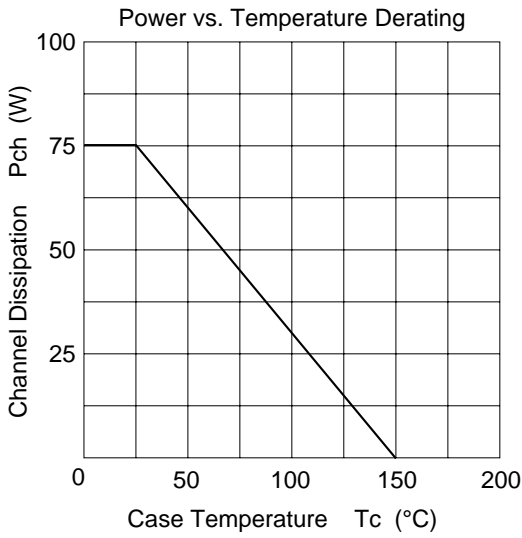
- Notes
1. PW 10  $\mu\text{s}$ , duty cycle 1 %
  2. Value at  $T_c = 25^\circ\text{C}$
  3. Value at  $T_{ch} = 25^\circ\text{C}$ ,  $R_g = 50 \Omega$

## Electrical Characteristics (Ta = 25°C)

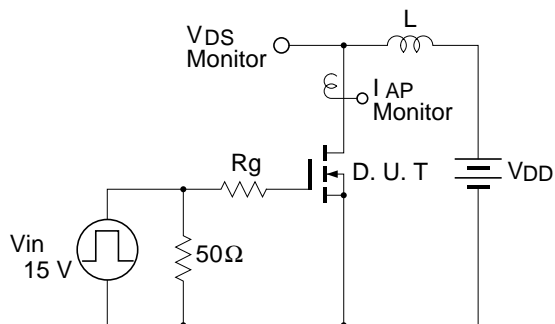
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	$\mu\text{A}$	$V_{DS} = 60 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$I_D = 1 \text{ mA}$ , $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	7	10	m	$I_D = 25 \text{ A}$ $V_{GS} = 10 \text{ V}$ Note 1
		—	10	16	m	$I_D = 25 \text{ A}$ $V_{GS} = 4 \text{ V}$ Note 1
Forward transfer admittance	$ y_{fs} $	35	55	—	S	$I_D = 25 \text{ A}$ $V_{DS} = 10 \text{ V}$ Note 1
Input capacitance	$C_{iss}$	—	3550	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	1760	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	500	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	35	—	ns	$I_D = 25 \text{ A}$
Rise time	$t_r$	—	230	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	470	—	ns	$R_L = 1.2$
Fall time	$t_f$	—	360	—	ns	
Body to drain diode forward voltage	$V_{DF}$	—	0.85	—	V	$I_F = 50 \text{ A}$ , $V_{GS} = 0$
Body to drain diode reverse recovery time	$t_{rr}$	—	135	—	ns	$I_F = 50 \text{ A}$ , $V_{GS} = 0$ $di_F / dt = 50 \text{ A} / \mu\text{s}$

Note 1. Pulse Test

See characteristic curves of 2SK2529.

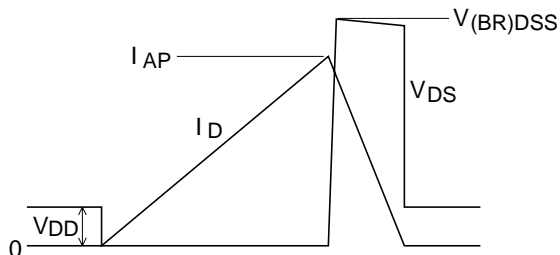


Avalanche Test Circuit

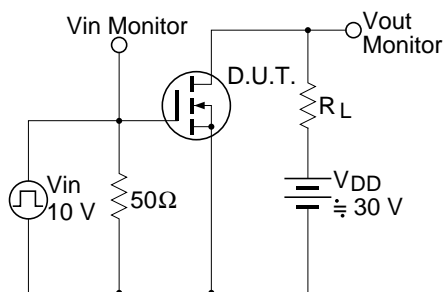


Avalanche Waveform

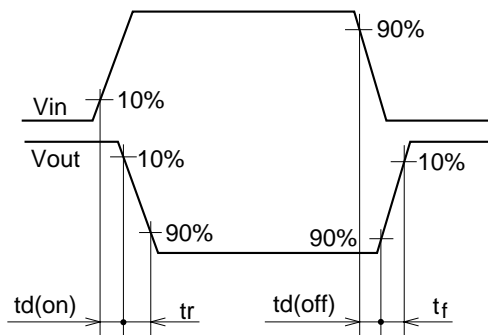
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

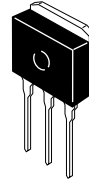
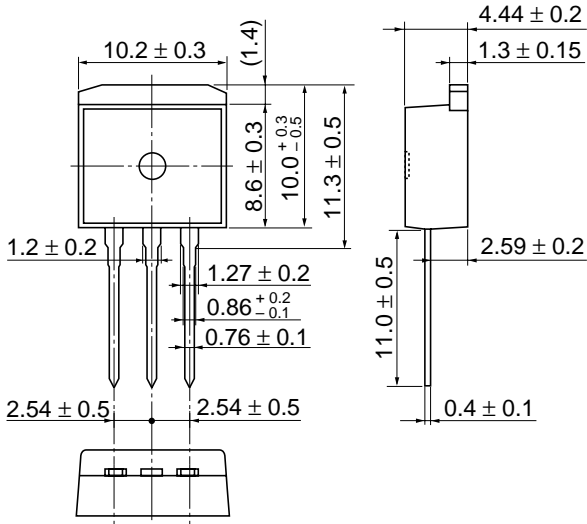


Waveform



Package Dimensions

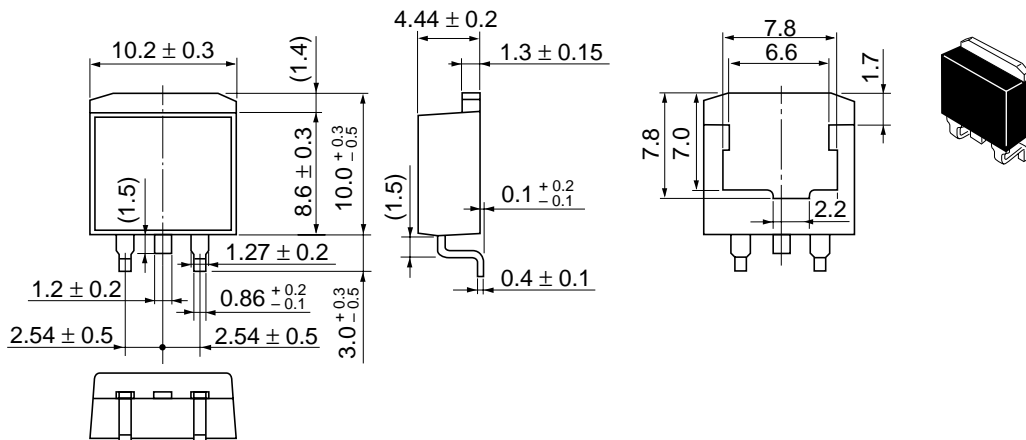
As of January, 2001  
Unit: mm



Hitachi Code	LDPAK (L)
JEDEC	—
EIAJ	—
Mass (reference value)	1.4 g

As of January, 2001

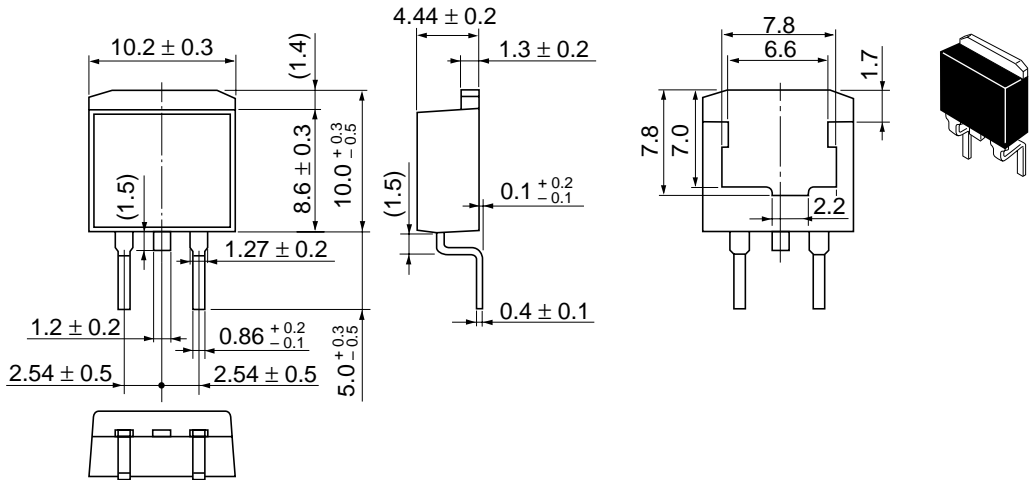
Unit: mm



Hitachi Code	LPAK (S)-(1)
JEDEC	—
EIAJ	—
Mass (reference value)	1.3 g

As of January, 2001

Unit: mm



Hitachi Code	LDPAK (S)-(2)
JEDEC	—
EIAJ	—
Mass (reference value)	1.35 g

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