

2SJ588

Silicon P Channel MOS FET
High Speed Switching

HITACHI

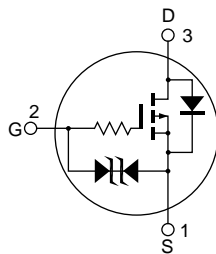
ADE-208-802 (Z)
1st.Edition.
June 1999

Features

- Low on-resistance
 $R_{DS} = 2.8$ typ. ($V_{GS} = -10$ V, $I_D = -50$ mA)
 $R_{DS} = 5.7$ typ. ($V_{GS} = -4$ V, $I_D = -50$ mA)
- 4 V gate drive device.

Outline

SPAK



1. Source
2. Drain
3. Gate

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-30	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	-100	mA
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	-400	mA
Body-drain diode reverse drain current	I_{DR}	-100	mA
Channel dissipation	Pch	300	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Note: 1. PW 10 μ s, duty cycle 1%

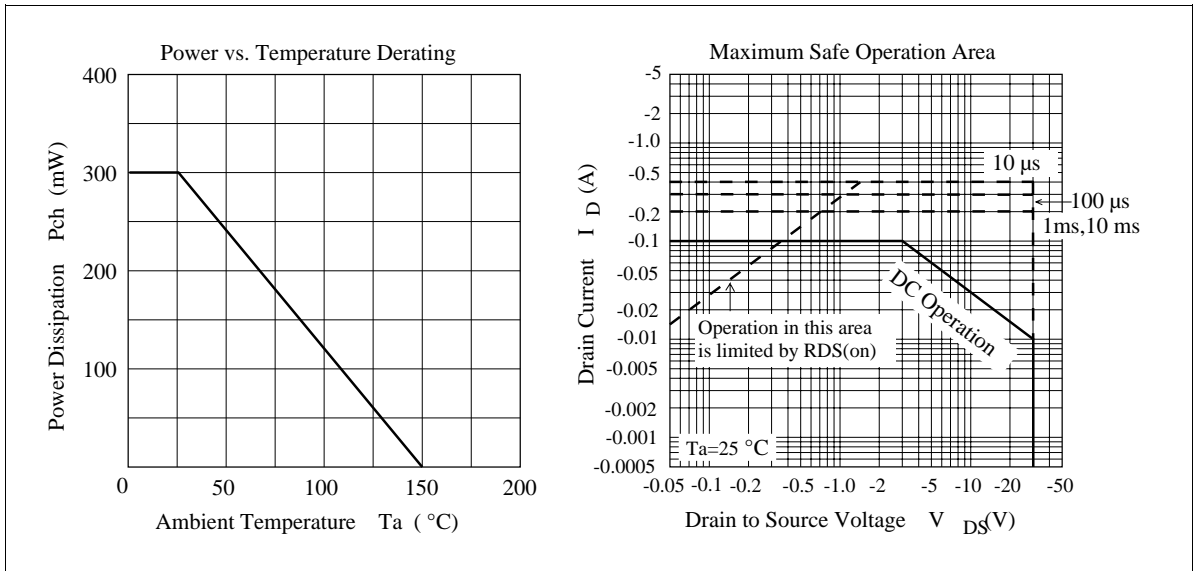
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -100 \mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \mu A, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 5	μA	$V_{GS} = \pm 16 V, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30 V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.3	—	-2.3	V	$I_D = -10 \mu A, V_{DS} = -5 V$
Static drain to source on state resistance	$R_{DS(on)}$	—	2.8	3.3		$I_D = -50 mA, V_{GS} = -10 V$ ^{Note 2}
	$R_{DS(on)}$	—	5.7	7.9		$I_D = -50 mA, V_{GS} = -4 V$ ^{Note 2}
Forward transfer admittance	$ y_{fs} $	68	105	—	mS	$I_D = -50 mA, V_{DS} = -10 V$ ^{Note 2}
Input capacitance	C_{iss}	—	25	—	pF	$V_{DS} = -10 V$
Output capacitance	C_{oss}	—	20	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	8	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	$I_D = -50 mA, V_{GS} = -10 V$
Rise time	t_r	—	15	—	ns	$R_L = 200$
Turn-off delay time	$t_{d(off)}$	—	40	—	ns	
Fall time	t_f	—	45	—	ns	

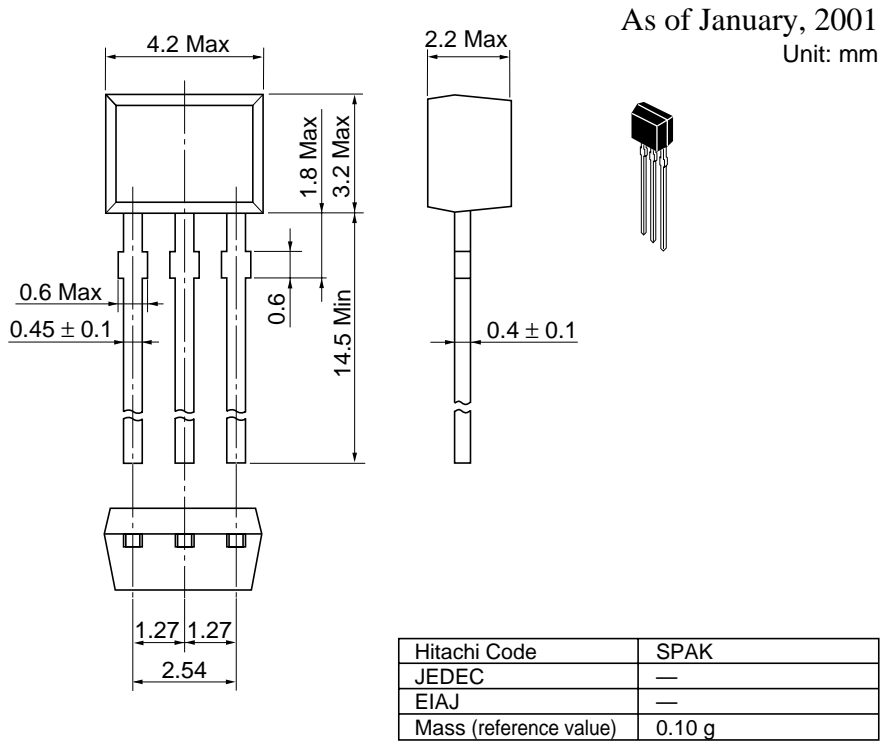
Note: 2. Pulse test

See characteristics curves of 2SJ575

Main Characteristics



Package Dimensions



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