

# 2SJ574

Silicon P Channel MOS FET  
High Speed Switching

# HITACHI

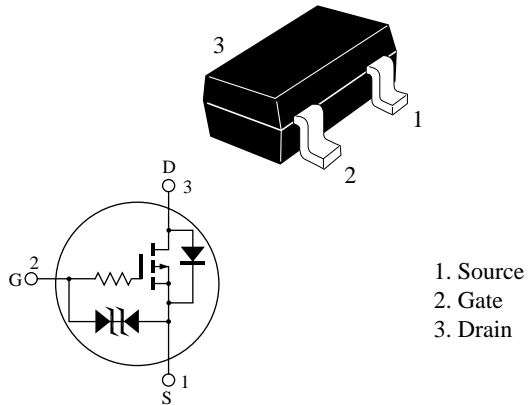
ADE-208-739B (Z)  
3rd.Edition.  
June 1999

## Features

- Low on-resistance  
 $R_{DS} = 1.1$  typ. ( $V_{GS} = -10$  V,  $I_D = -150$  mA)  
 $R_{DS} = 2.2$  typ. ( $V_{GS} = -4$  V,  $I_D = -150$  mA)
- 4 V gate drive device.
- Small package (MPAK)

## Outline

MPAK



## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-30	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	-300	mA
Drain peak current	$I_{D(pulse)}$ <sup>Note 1</sup>	-1.2	A
Body-drain diode reverse drain current	$I_{DR}$	-300	mA
Channel dissipation	Pch <sup>Note 2</sup>	400	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Note: 1. PW 10 μs, duty cycle 1%

2. Value on the alumina ceramic board (12.5x20x0.7mm)

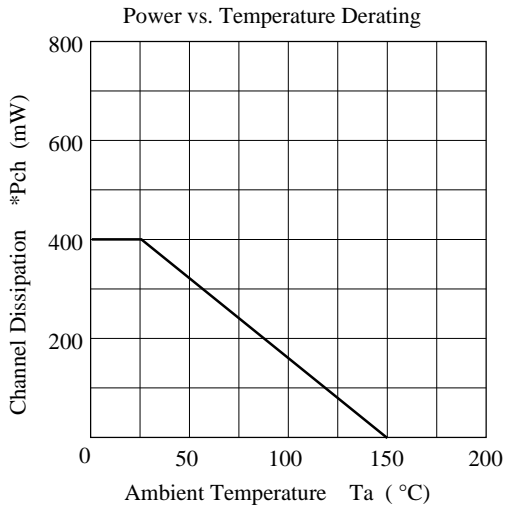
## Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -100 \mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \mu A, V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±5	μA	$V_{GS} = \pm 16 V, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-1	μA	$V_{DS} = -30 V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.3	—	-2.3	V	$I_D = -10 \mu A, V_{DS} = -5 V$
Static drain to source on state resistance	$R_{DS(on)}$	—	1.1	1.3		$I_D = -150 mA, V_{GS} = -10 V$ <sup>Note 3</sup>
	$R_{DS(on)}$	—	2.2	3.1		$I_D = -150 mA, V_{GS} = -4 V$ <sup>Note 3</sup>
Forward transfer admittance	$ y_{fs} $	195	300	—	mS	$I_D = -150 mA, V_{DS} = -10 V$ <sup>Note 3</sup>
Input capacitance	Ciss	—	50	—	pF	$V_{DS} = -10 V$
Output capacitance	Coss	—	40	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	15	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$I_D = -150 mA, V_{GS} = -10 V$
Rise time	$t_r$	—	50	—	ns	$R_L = 66.6$
Turn-off delay time	$t_{d(off)}$	—	110	—	ns	
Fall time	$t_f$	—	105	—	ns	

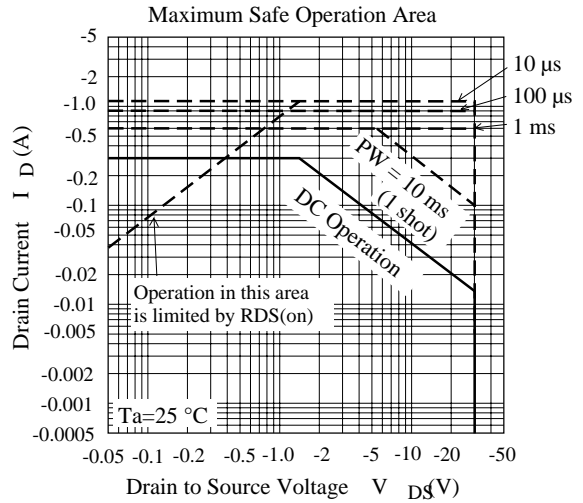
Note: 3. Pulse test

4. Marking is BP

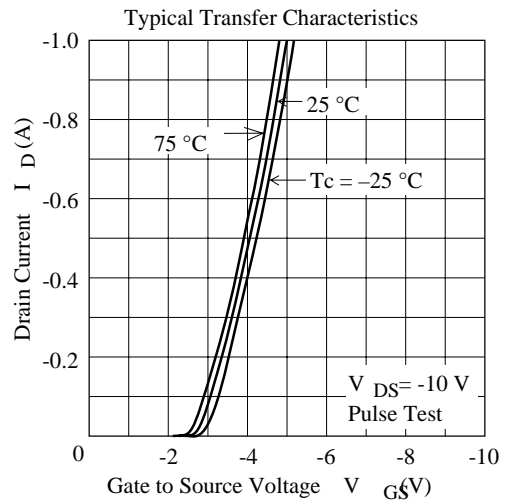
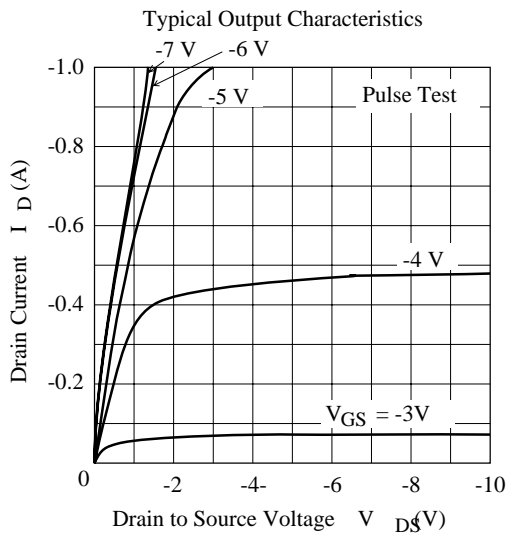
## Main Characteristics



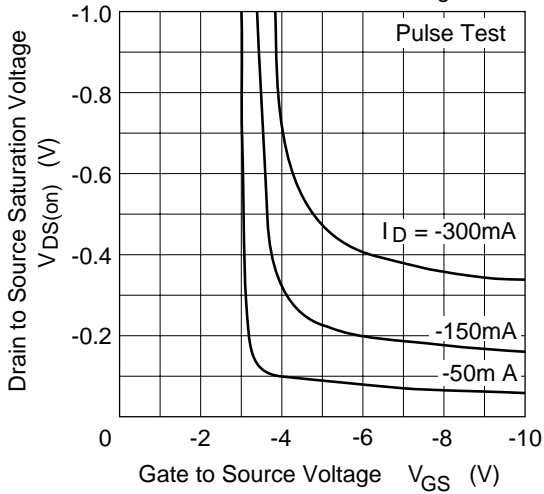
\*Value on the alumina ceramic board.(12.5x20x0.7mm)



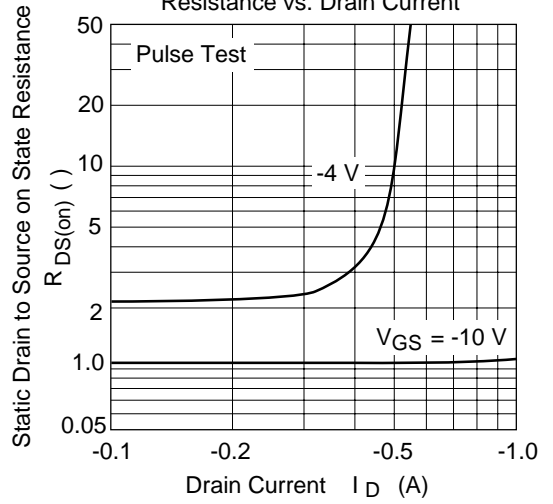
Value on the alumina ceramic board.(12.5x20x0.7mm)



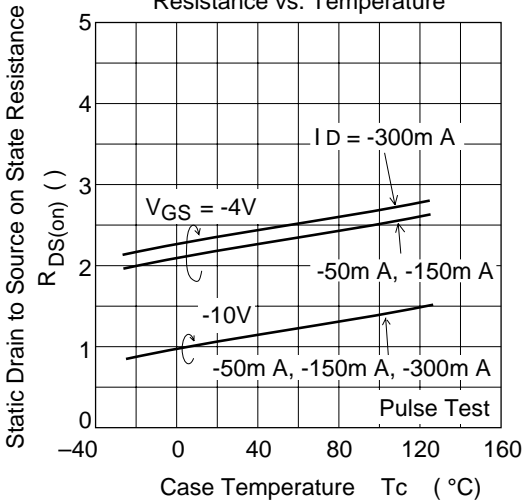
Drain to Source Saturation Voltage vs. Gate to Source Voltage



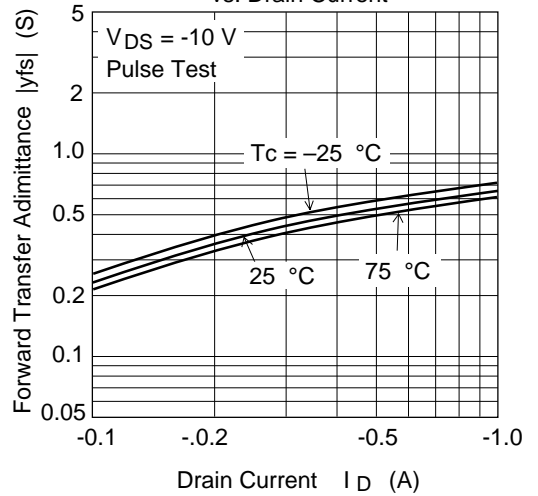
Static Drain to Source on State Resistance vs. Drain Current



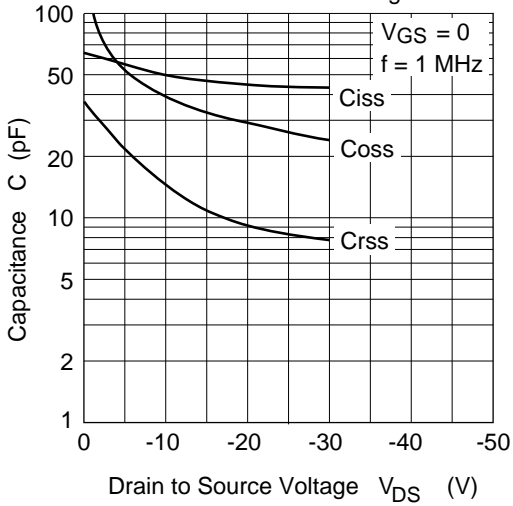
Static Drain to Source on State Resistance vs. Temperature



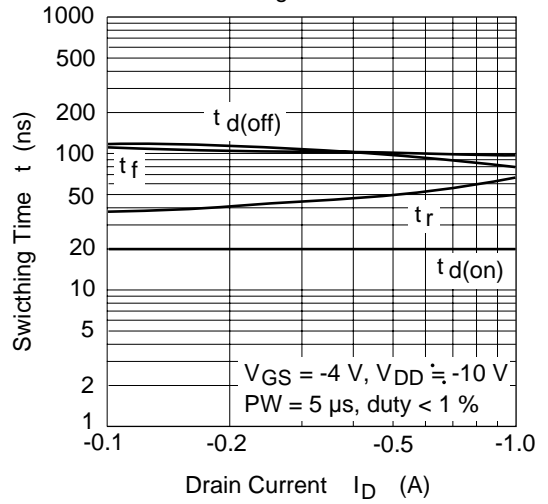
Forward Transfer Admittance vs. Drain Current



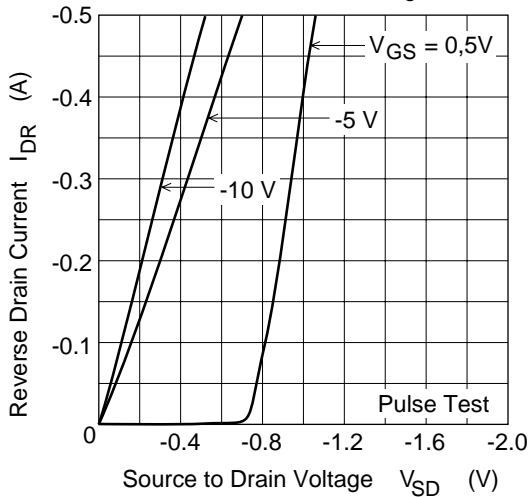
Typical Capacitance vs. Drain to Source Voltage



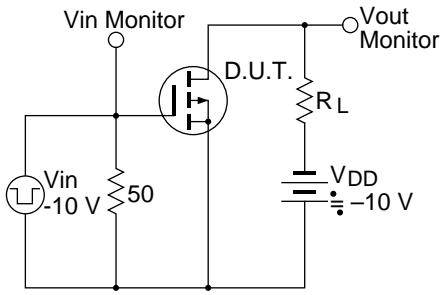
Switching Characteristics



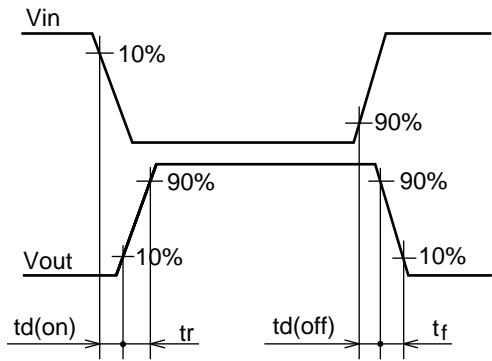
Reverse Drain Current vs. Source to Drain Voltage



Switching Time Test Circuit



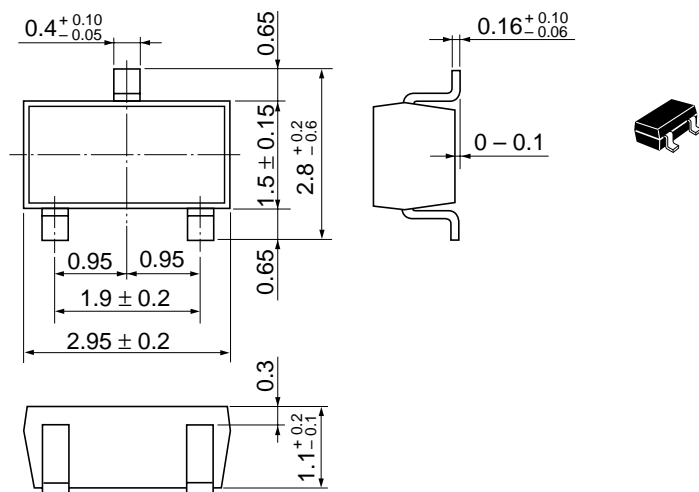
Waveforms



## Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	MPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.011 g

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**Hitachi, Ltd.**

Semiconductor & Integrated Circuits.  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	NorthAmerica	: <a href="http://semiconductor.hitachi.com/">http://semiconductor.hitachi.com/</a>
	Europe	: <a href="http://www.hitachi-eu.com/hel/ecg">http://www.hitachi-eu.com/hel/ecg</a>
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**For further information write to:**

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive,  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1> (408) 433-0223

Hitachi Europe GmbH  
Electronic Components Group  
Dornacher Straße 3  
D-85622 Feldkirchen, Munich  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Group.  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 585160

Hitachi Asia Ltd.  
Hitachi Tower  
16 Collyer Quay #20-00,  
Singapore 049318  
Tel : <65>-538-6533/538-8577  
Fax : <65>-538-6933/538-3877  
URL : <http://www.hitachi.com.sg>

Hitachi Asia Ltd.  
(Taipei Branch Office)  
4/F, No. 167, Tun Hwa North Road,  
Hung-Kuo Building,  
Taipei (105), Taiwan  
Tel : <886>-(2)-2718-3666  
Fax : <886>-(2)-2718-8180  
Telex : 23222 HAS-TP  
URL : <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower,  
World Finance Centre,  
Harbour City, Canton Road  
Tsim Sha Tsui, Kowloon,  
Hong Kong  
Tel : <852>-(2)-735-9218  
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