

2SJ555

Silicon P Channel MOS FET
High Speed Power Switching

HITACHI

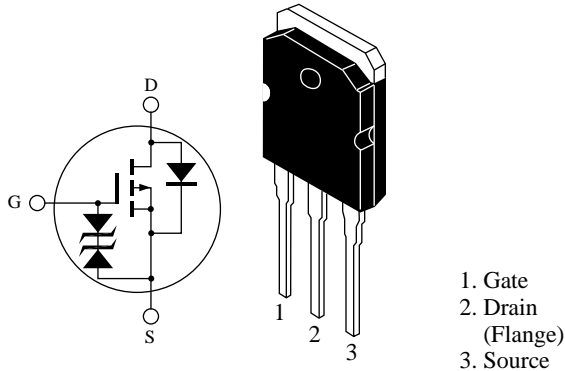
ADE-208-634A (Z)
2nd. Edition
Jul. 1998

Features

- Low on-resistance
 $R_{DS(on)} = 0.017\Omega$ typ.
- Low drive current.
- 4V gate drive devices.
- High speed switching.

Outline

TO-3P



Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-60	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	-60	A
Drain peak current	$I_{D(pulse)}^{Note1}$	-240	A
Body-drain diode reverse drain current	I_{DR}	-60	A
Avalanche current	I_{AP}^{Note3}	-60	A
Avalanche energy	E_{AR}^{Note3}	308	mJ
Channel dissipation	P_{ch}^{Note2}	125	W
Channel temperature	Tch	150	$^\circ\text{C}$
Storage temperature	Tstg	-55 to +150	$^\circ\text{C}$

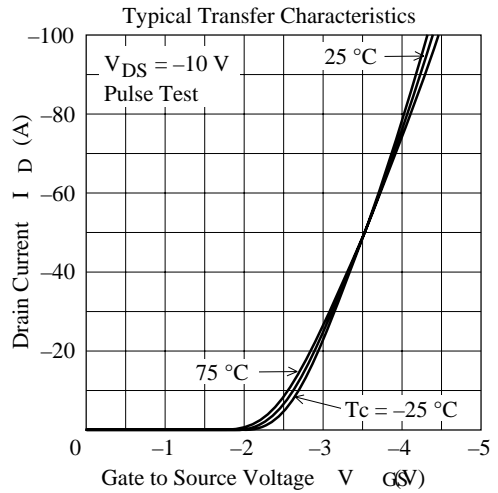
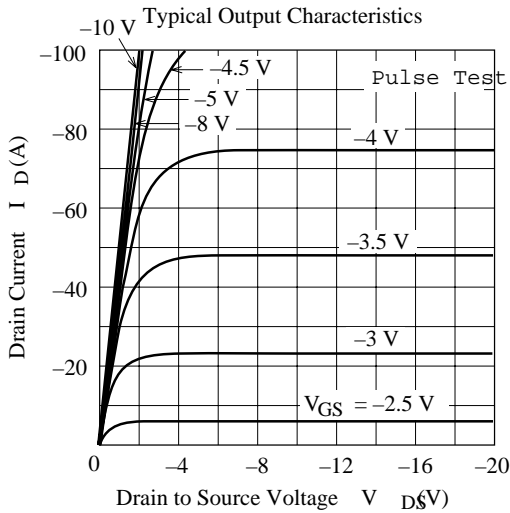
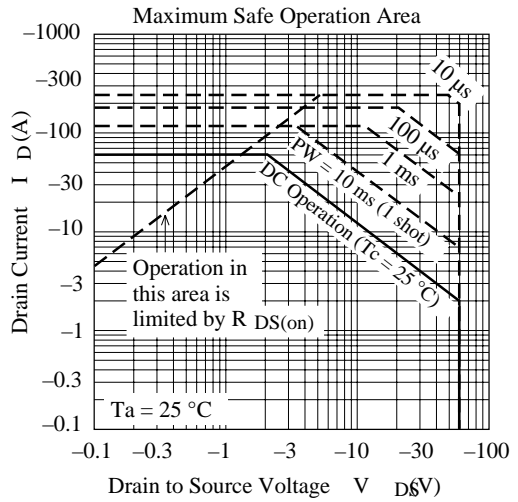
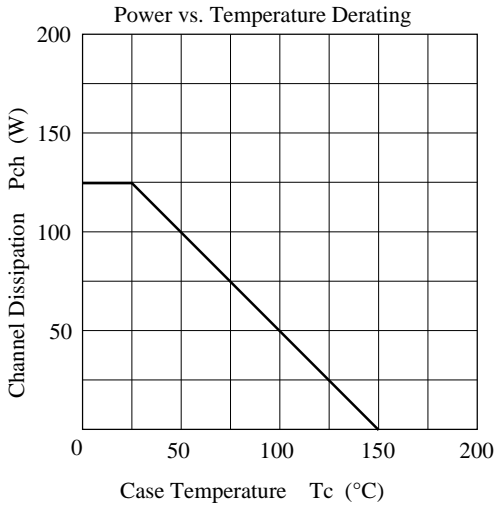
Note: 1. $PW \leq 10\mu\text{s}$, duty cycle $\leq 1\%$
2. Value at $T_c = 25^\circ\text{C}$
3. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50\ \Omega$

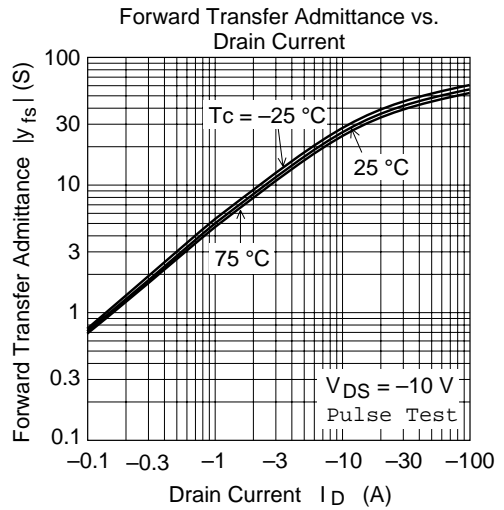
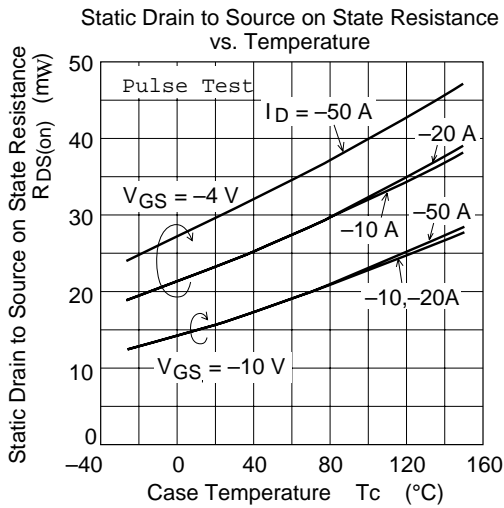
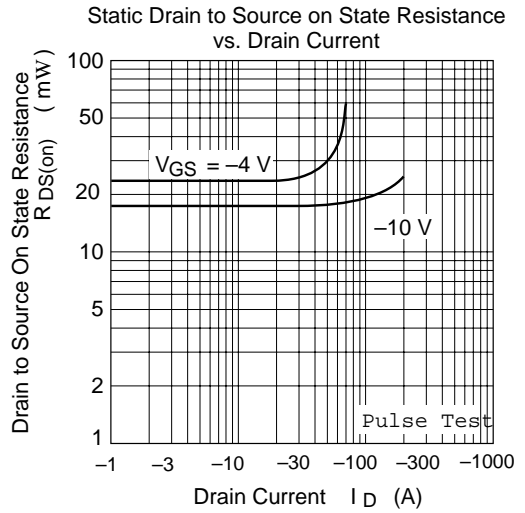
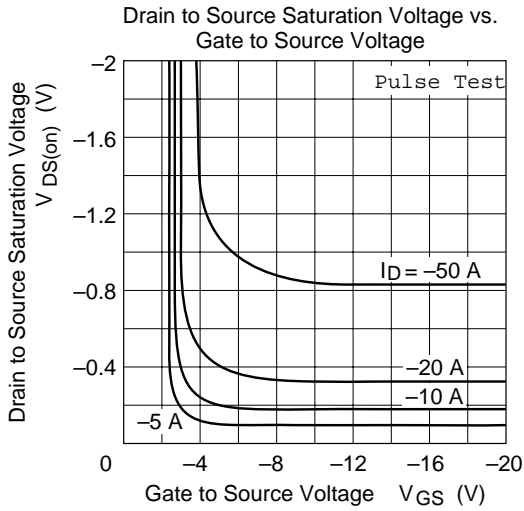
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10\text{mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -60\text{V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16\text{V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1\text{mA}$, $V_{DS} = -10\text{V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.017	0.022	Ω	$I_D = -30\text{A}$, $V_{GS} = -10\text{V}$ ^{Note4}
	$R_{DS(on)}$	—	0.024	0.036	Ω	$I_D = -30\text{A}$, $V_{GS} = -4\text{V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	27	45	—	S	$I_D = -30\text{A}$, $V_{DS} = -10\text{V}$ ^{Note4}
Input capacitance	C_{iss}	—	4100	—	pF	$V_{DS} = -10\text{V}$
Output capacitance	C_{oss}	—	2100	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	450	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	32	—	ns	$V_{GS} = -10\text{V}$, $I_D = -30\text{A}$
Rise time	t_r	—	270	—	ns	$R_L = 1\Omega$
Turn-off delay time	$t_{d(off)}$	—	570	—	ns	
Fall time	t_f	—	360	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-1.1	—	V	$I_F = -60\text{A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	115	—	ns	$I_F = -60\text{A}$, $V_{GS} = 0$ $di_F/dt = 50\text{A}/\mu\text{s}$

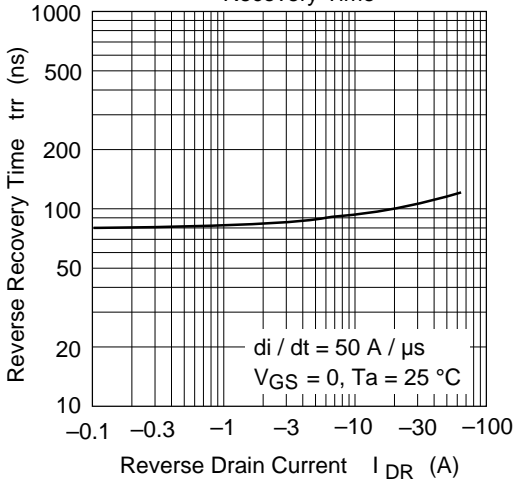
Note: 4. Pulse test

Main Characteristics

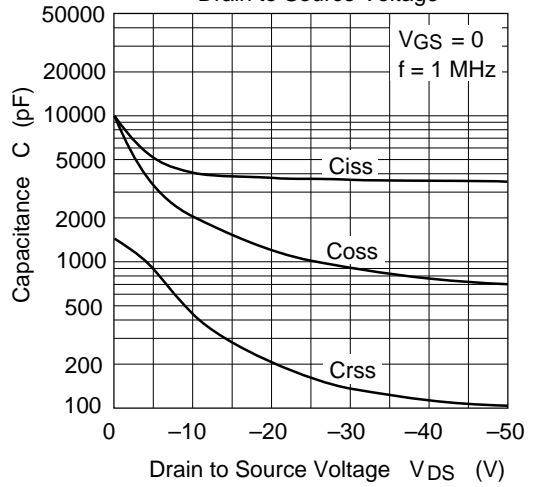




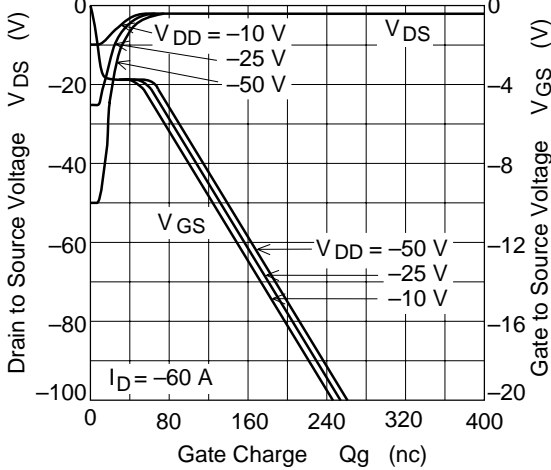
Body-Drain Diode Reverse Recovery Time



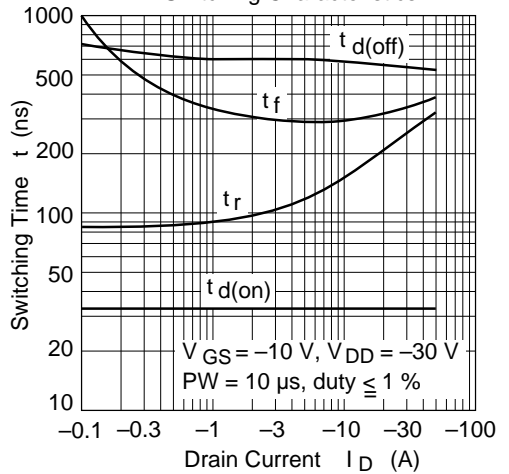
Typical Capacitance vs. Drain to Source Voltage

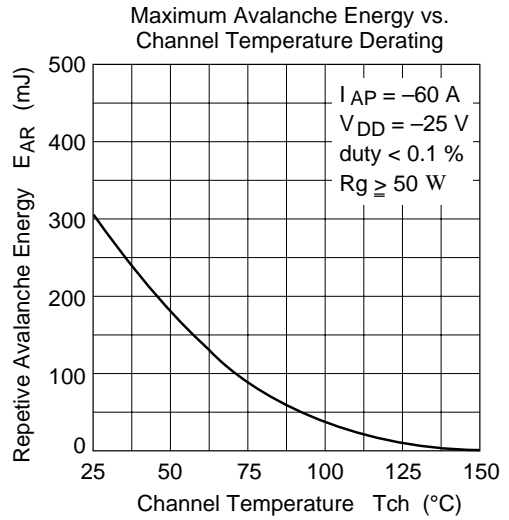
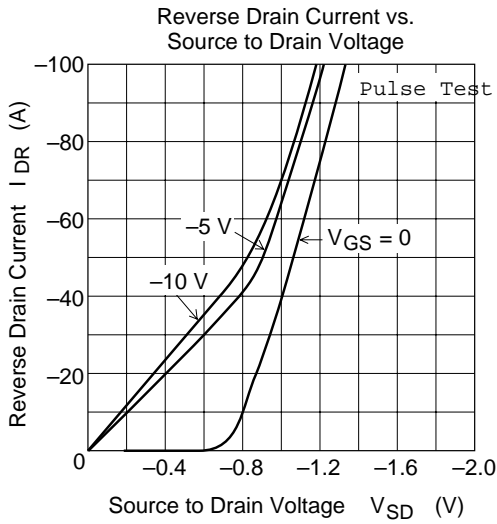


Dynamic Input Characteristics

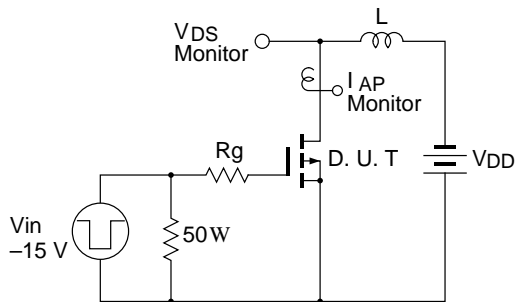


Switching Characteristics



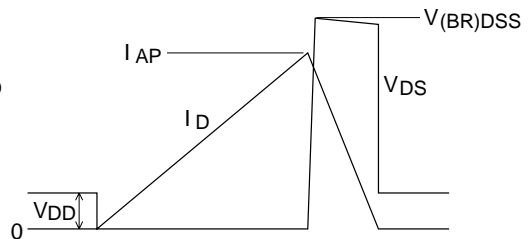


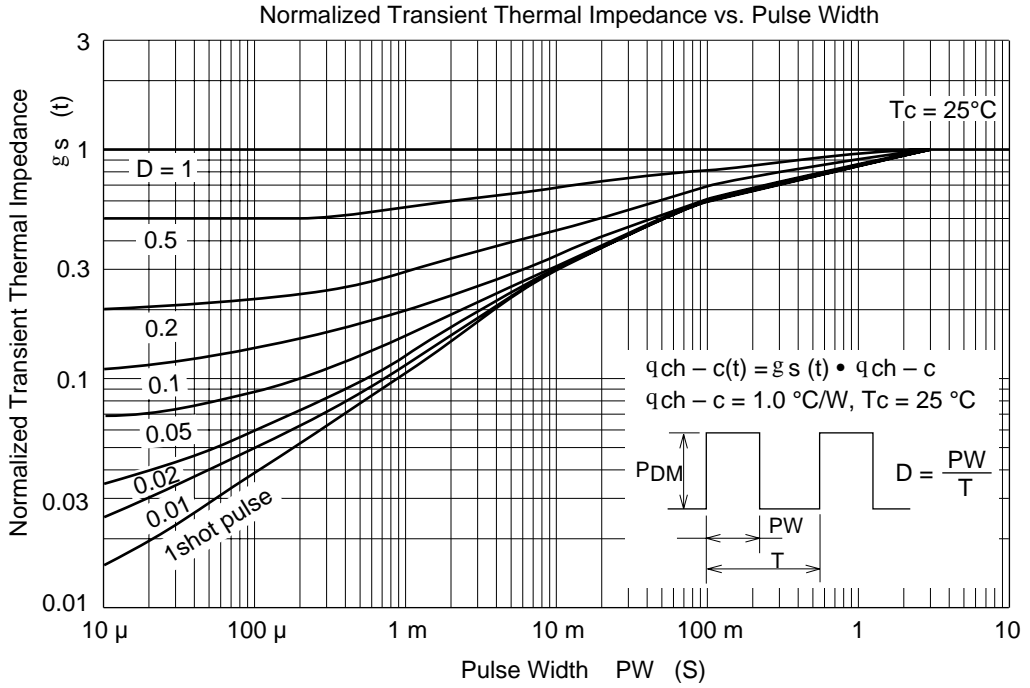
Avalanche Test Circuit



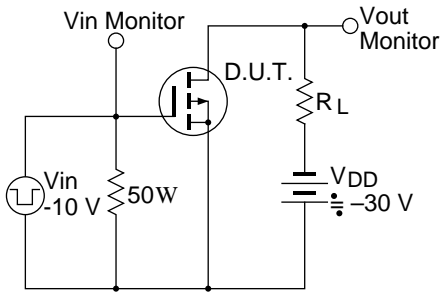
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

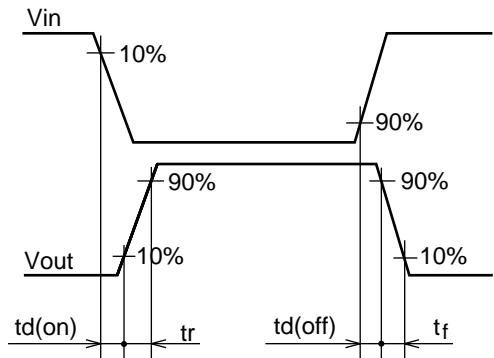




Switching Time Test Circuit



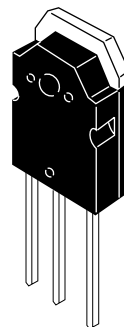
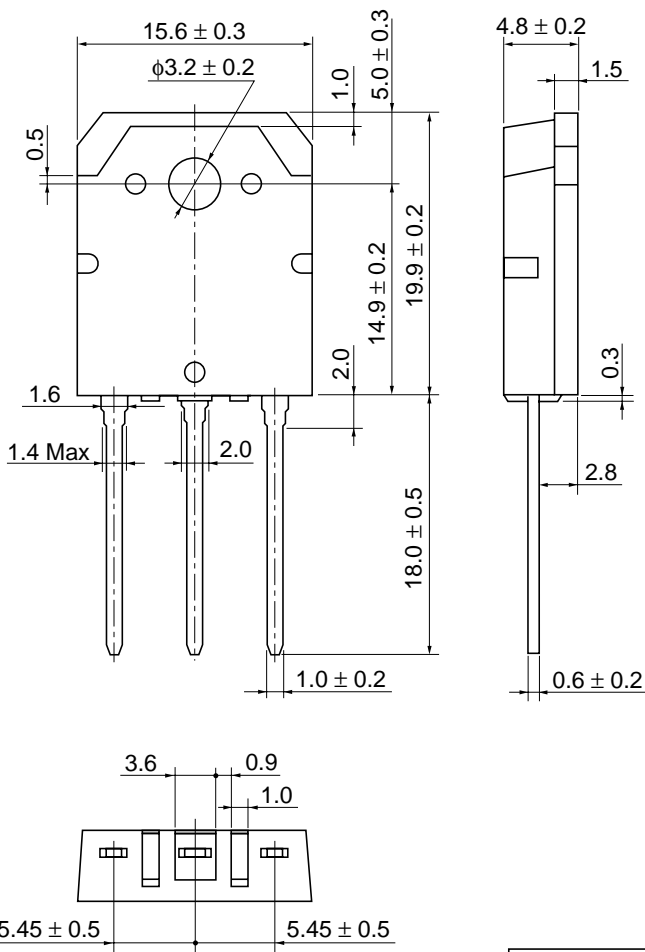
Waveform



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	TO-3P
JEDEC	—
EIAJ	Conforms
Mass (reference value)	5.0 g

Cautions

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