

2SJ554

Silicon P Channel MOS FET
High Speed Power Switching

HITACHI

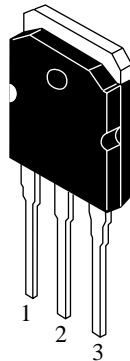
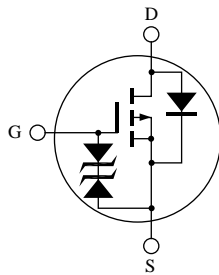
ADE-208-628B (Z)
3rd. Edition
Jun. 1998

Features

- Low on-resistance
 $R_{DS(on)} = 0.028\Omega$ typ.
- Low drive current.
- 4V gate drive devices.
- High speed switching.

Outline

TO-3P



1. Gate
2. Drain
(Flange)
3. Source

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-60	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	-45	A
Drain peak current	$I_{D(pulse)}^{Note1}$	-180	A
Body-drain diode reverse drain current	I_{DR}	-45	A
Avalanche current	I_{AP}^{Note3}	-45	A
Avalanche energy	E_{AR}^{Note3}	173	mJ
Channel dissipation	P_{ch}^{Note2}	100	W
Channel temperature	Tch	150	$^\circ\text{C}$
Storage temperature	Tstg	-55 to +150	$^\circ\text{C}$

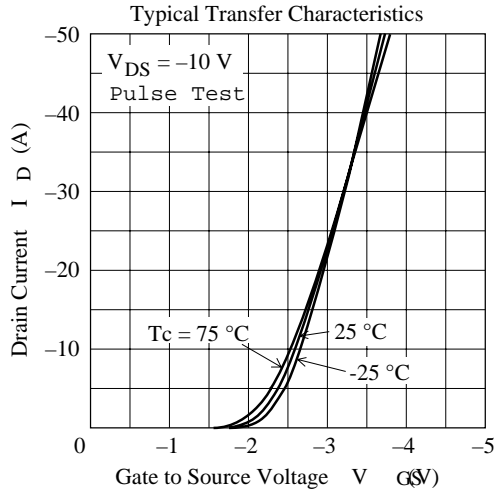
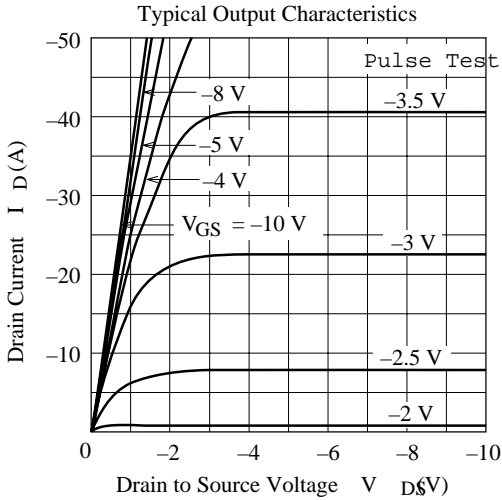
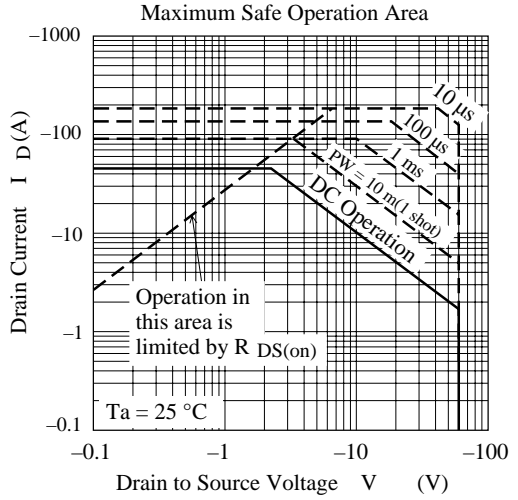
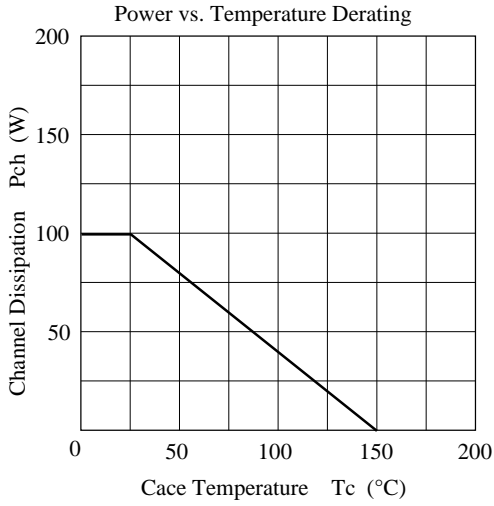
Note: 1. $PW \leq 10\mu\text{s}$, duty cycle $\leq 1\%$
2. Value at $T_c = 25^\circ\text{C}$
3. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50\ \Omega$

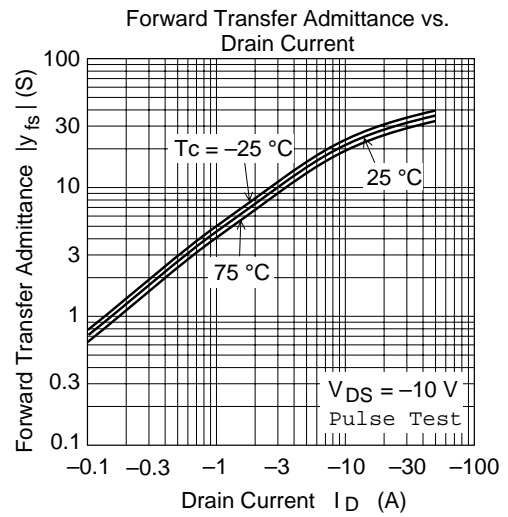
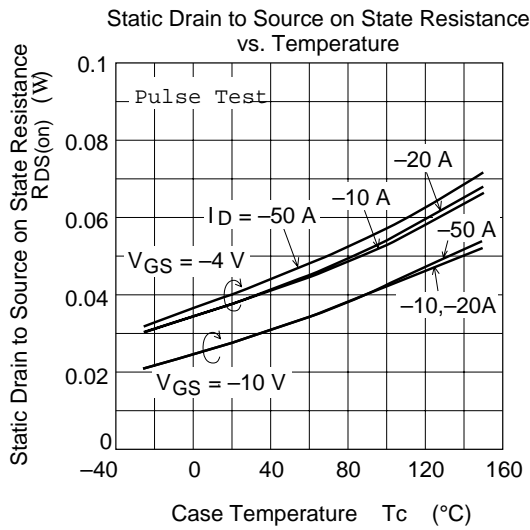
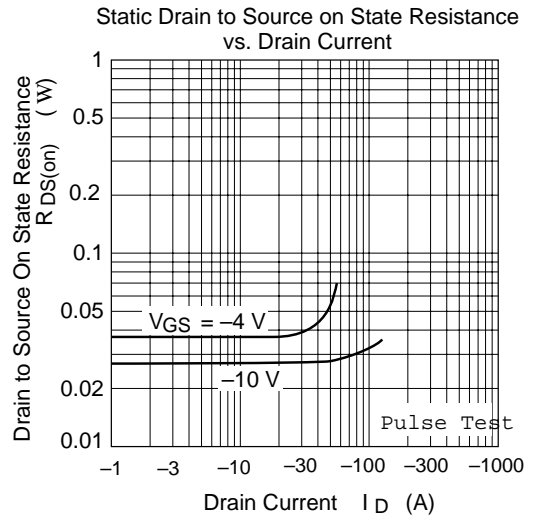
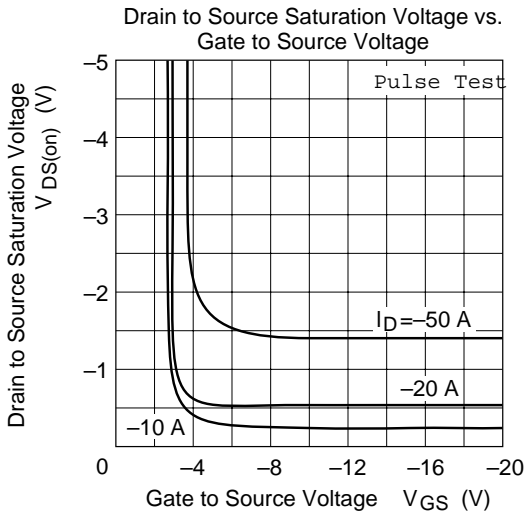
Electrical Characteristics (Ta = 25°C)

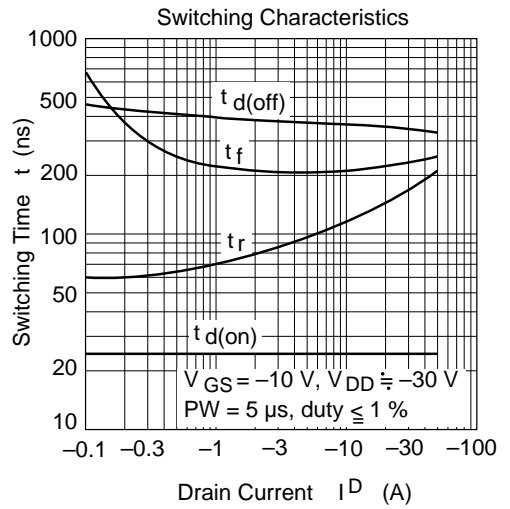
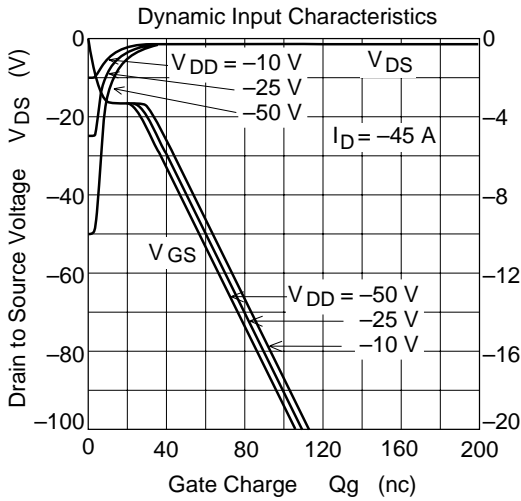
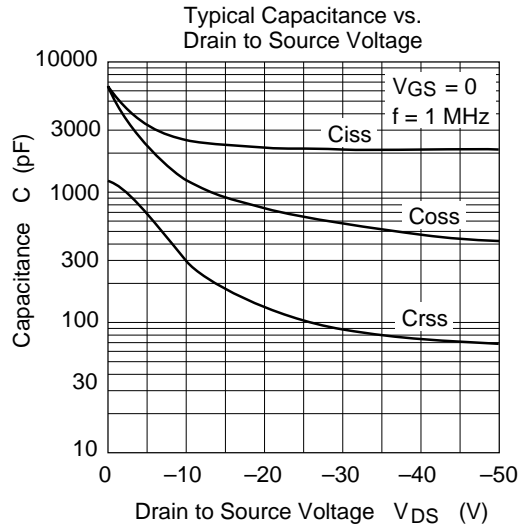
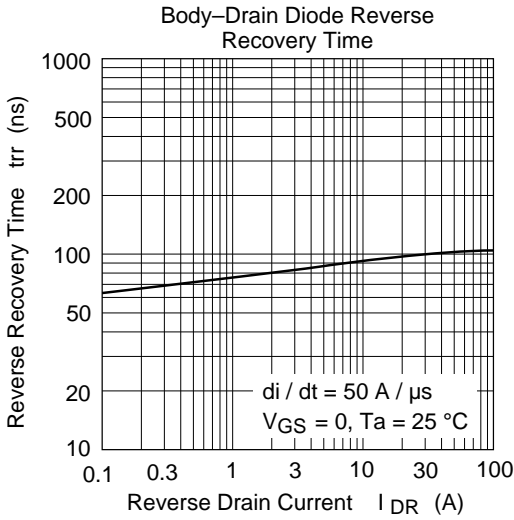
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10\text{mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -60\text{V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16\text{V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1\text{mA}$, $V_{DS} = -10\text{V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.028	0.037	Ω	$I_D = -25\text{A}$, $V_{GS} = -10\text{V}$ ^{Note4}
	$R_{DS(on)}$	—	0.038	0.055	Ω	$I_D = -25\text{A}$, $V_{GS} = -4\text{V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	18	30	—	S	$I_D = -25\text{A}$, $V_{DS} = -10\text{V}$ ^{Note4}
Input capacitance	C_{iss}	—	2500	—	pF	$V_{DS} = -10\text{V}$
Output capacitance	C_{oss}	—	1300	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	300	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	25	—	ns	$V_{GS} = -10\text{V}$, $I_D = -25\text{A}$
Rise time	t_r	—	160	—	ns	$R_L = 1.2\Omega$
Turn-off delay time	$t_{d(off)}$	—	350	—	ns	
Fall time	t_f	—	240	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-1.1	—	V	$I_F = -45\text{A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	100	—	ns	$I_F = -45\text{A}$, $V_{GS} = 0$ $diF/dt = 50\text{A}/\mu\text{s}$

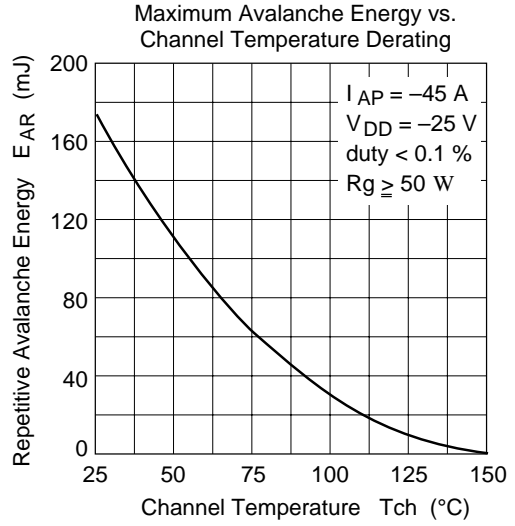
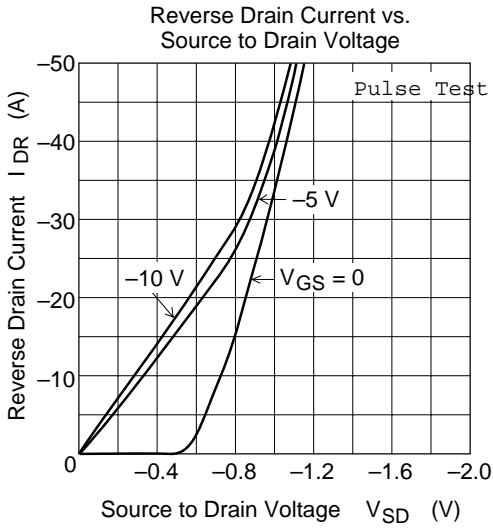
Note: 4. Pulse test

Main Characteristics

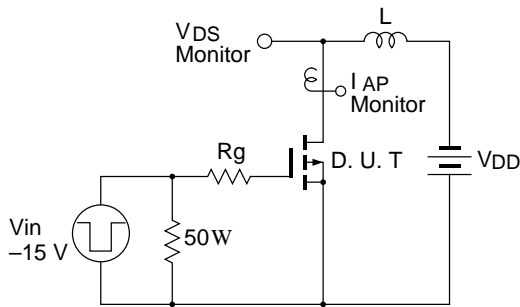






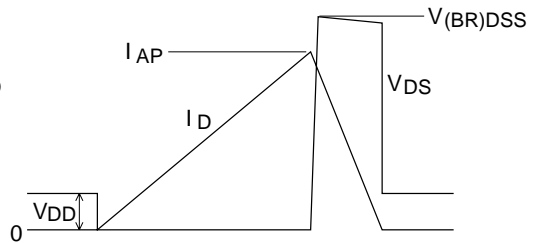


Avalanche Test Circuit

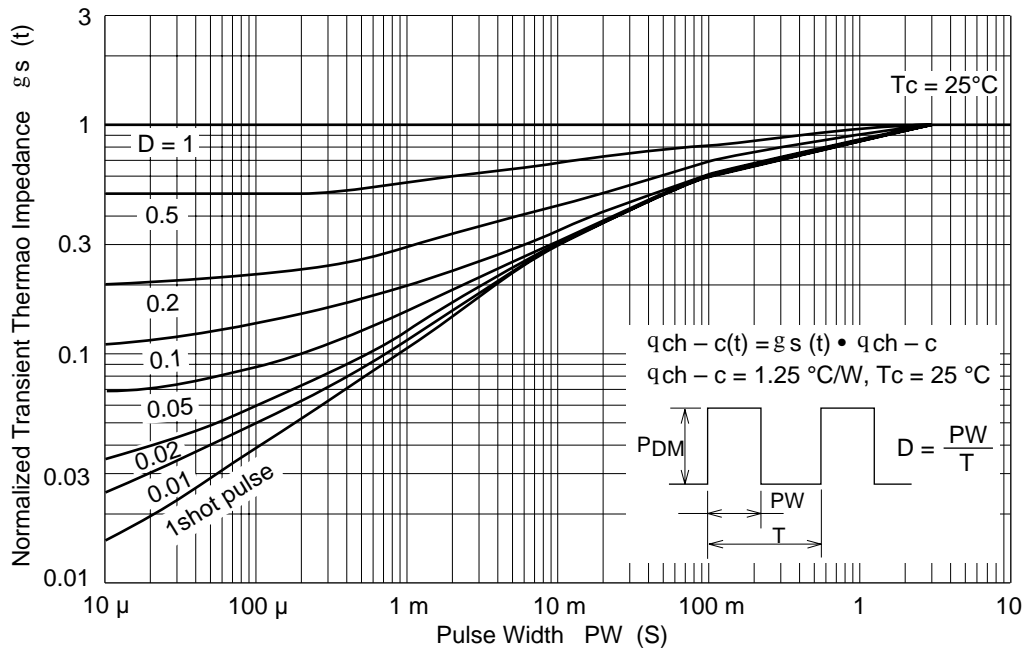


Avalanche Waveform

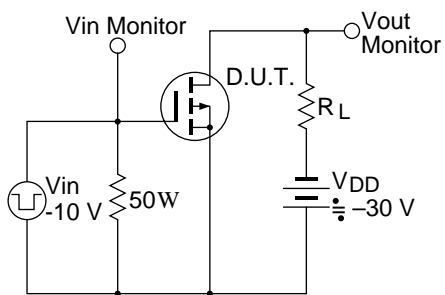
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



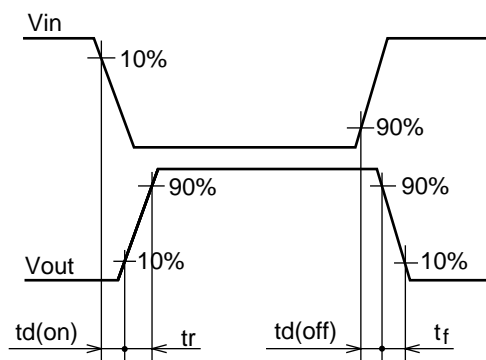
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



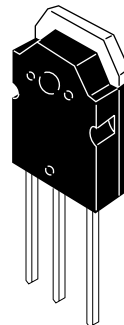
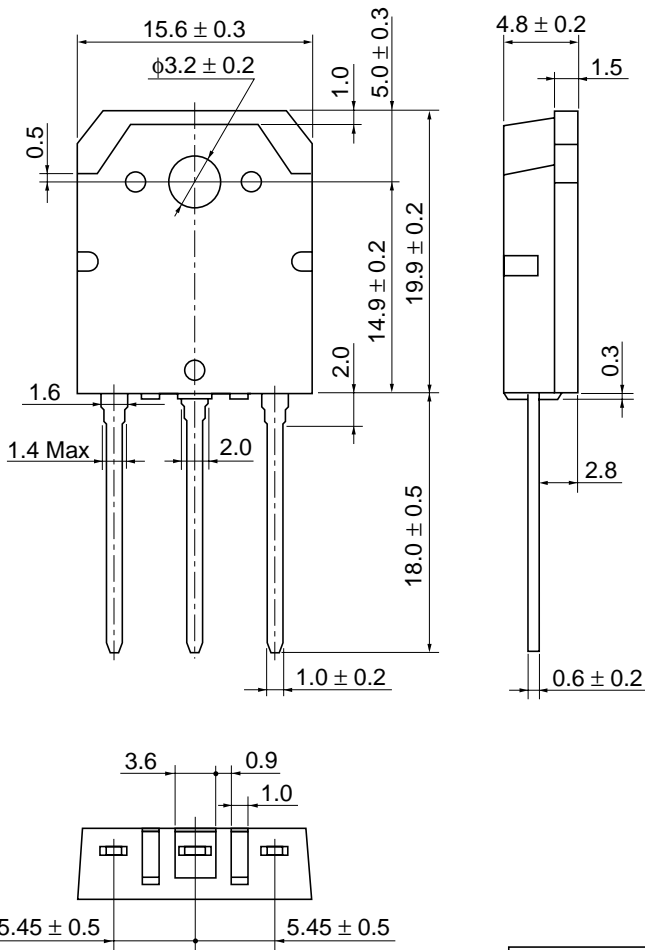
Waveform



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	TO-3P
JEDEC	—
EIAJ	Conforms
Mass (reference value)	5.0 g

Cautions

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Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	NorthAmerica	: http://semiconductor.hitachi.com/
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00,
Singapore 049318
Tel : <65>-538-6533/538-8577
Fax : <65>-538-6933/538-3877
URL : <http://www.hitachi.com.sg>

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road,
Hung-Kuo Building,
Taipei (105), Taiwan
Tel : <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon,
Hong Kong
Tel : <852>-(2)-735-9218
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Colophon 2.0



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