

MOS FIELD EFFECT POWER TRANSISTORS 2SJ324, 2SJ324-Z

SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SJ324 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 0.18 \Omega$ TYP. ($V_{GS} = -10$ V, $I_D = -1$ A)
 $R_{DS(on)} = 0.36 \Omega$ TYP. ($V_{GS} = -4$ V, $I_D = -0.8$ A)
- Low C_{iss} $C_{iss} = 330$ pF TYP.
- Built-in G-S Gate Protection Diode

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

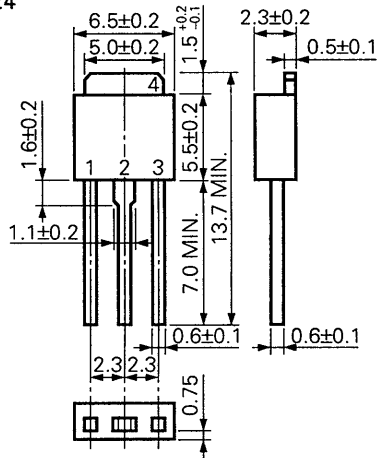
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	-30	V
Gate to Source Voltage (AC)	V_{GSS}	∓ 20	V
Gate to Source Voltage (DC)	V_{GSS}	-20, +10	V
Drain Current (DC)	$I_{D(DC)}$	∓ 2.0	A
Drain Current (pulse)	$I_{D(pulse)^*}$	∓ 8.0	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_{T1}	20	W
Total Power Dissipation ($T_a = 25^\circ\text{C}$)	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

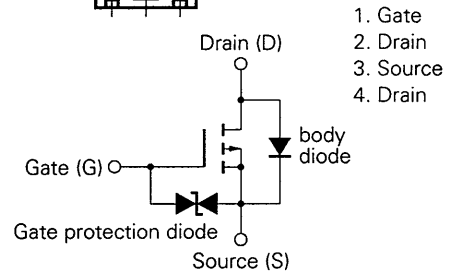
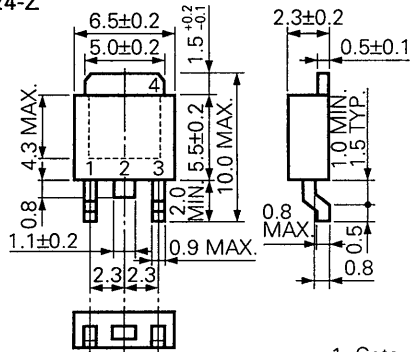
* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

PACKAGE DIMENSIONS in millimeters

2SJ324



2SJ324-Z

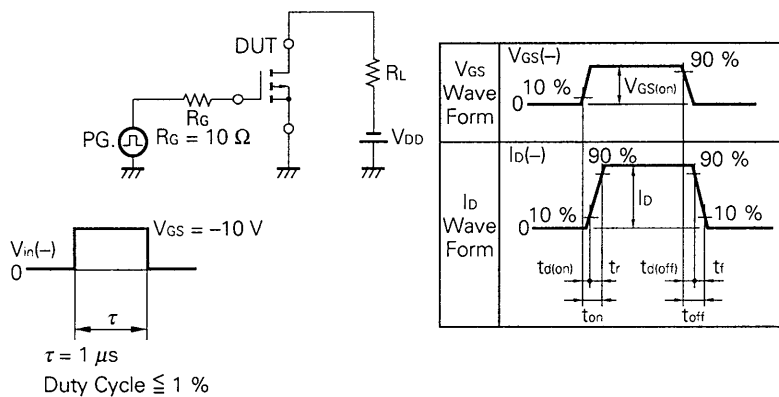


1. Gate
2. Drain
3. Source
4. Drain

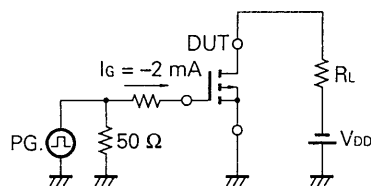
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		0.18	0.25	Ω	V _{GS} = -10 V, I _D = -1.0 A
Drain to Source On-state Resistance	R _{DS(on)}		0.36	0.52	Ω	V _{GS} = -4 V, I _D = -0.8 A
Gate to Source Cutoff Voltage	V _{GS(off)}	-1.0	-1.5	-2.0	V	V _{DS} = -10 V, I _D = -1 mA
Forward Transfer Admittance	y _{fs}	1.0	1.9		S	V _{DS} = -10 V, I _D = -1.0 A
Drain Leakage Current	I _{DSS}			-10	μA	V _{DS} = -30 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±16 V, V _{DS} = 0
Input Capacitance	C _{iss}		330		pF	V _{DS} = -10 V
Output Capacitance	C _{oss}		290		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		105		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		7		ns	V _{GS(on)} = -10 V
Rise Time	t _r		35		ns	V _{DD} = -15 V
Turn-Off Delay Time	t _{d(off)}		40		ns	I _D = -1.0 A, R _G = 10 Ω
Fall Time	t _f		30		ns	R _L = 15 Ω
Total Gate Charge	Q _G		12		nC	V _{GS} = -10 V
Gate to Source Charge	Q _{GS}		1.5		nC	I _D = -2.0 A
Gate to Drain Charge	Q _{GD}		4.5		nC	V _{DD} = -24 V
Body Diode Forward Voltage	V _F		0.9		V	I _F = 2.0 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		50		ns	I _F = 2.0 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		40		nC	di/dt = 50 A/μs
ESD	V _{ESD}		±130		V	C = 200 pF, R = 0, Single Pulse

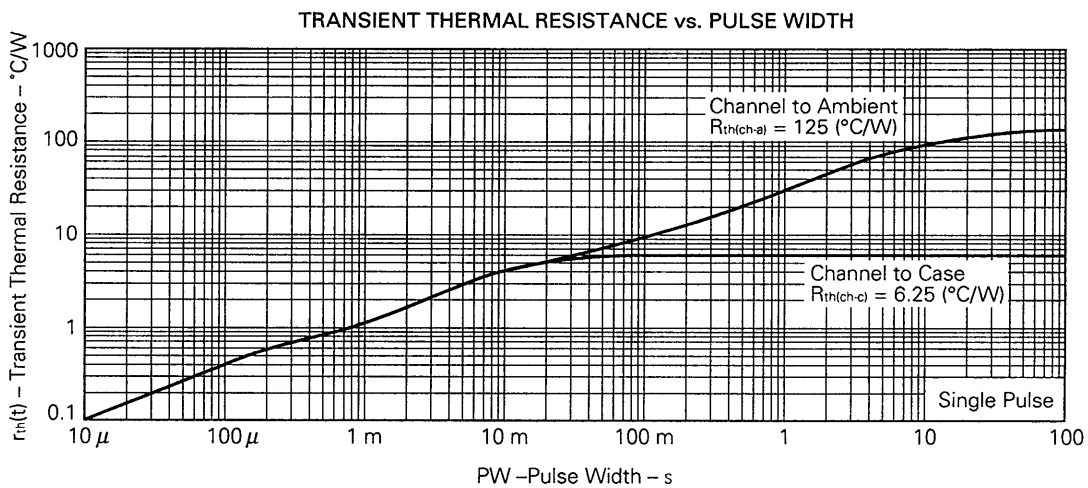
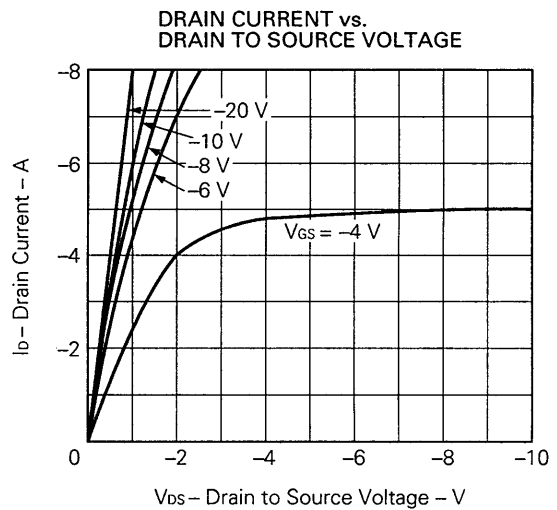
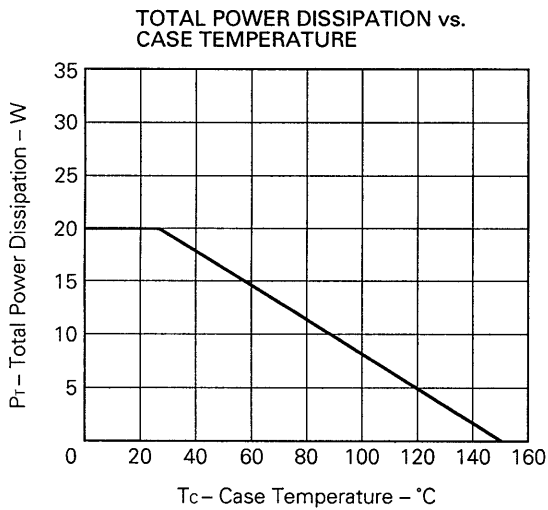
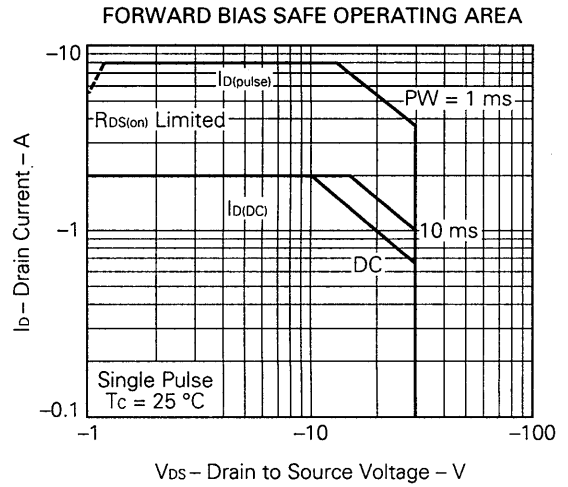
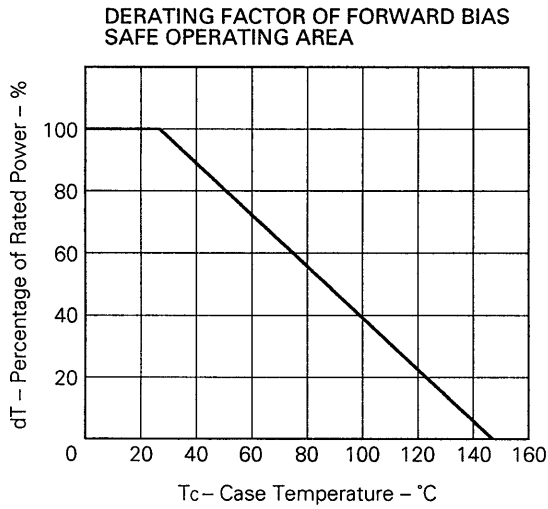
Test Circuit 1: Switching Time

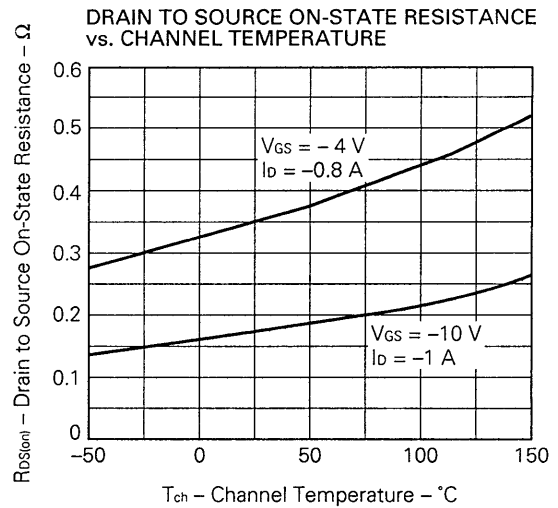
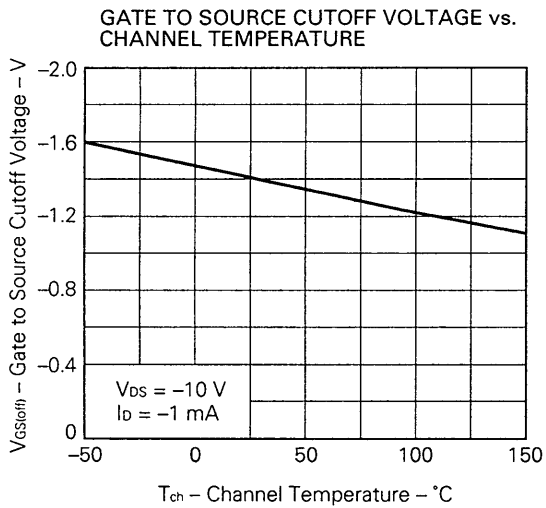
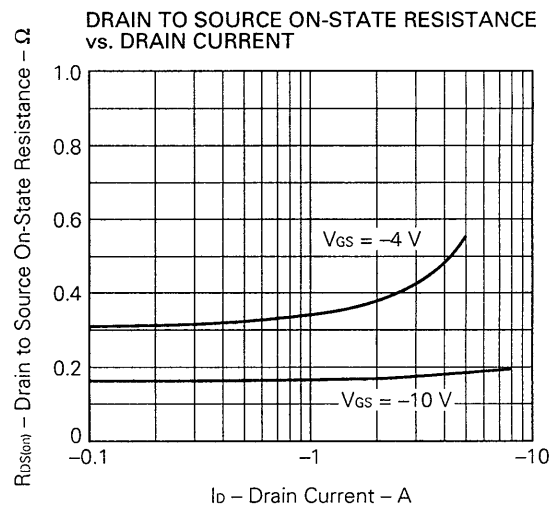
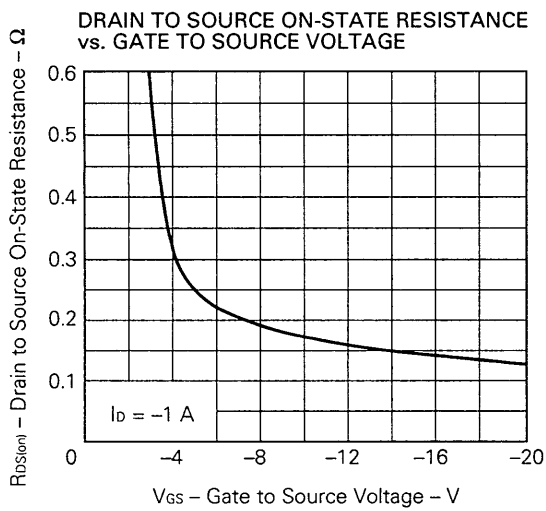
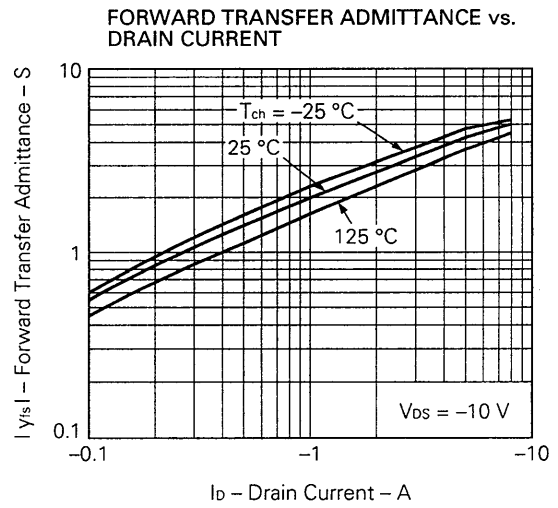
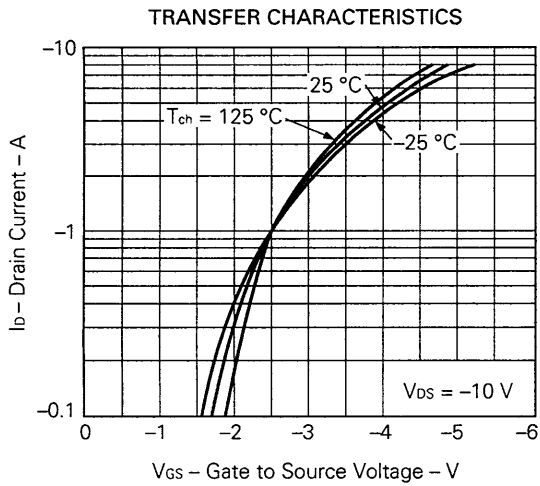


Test Circuit 2: Gate Charge

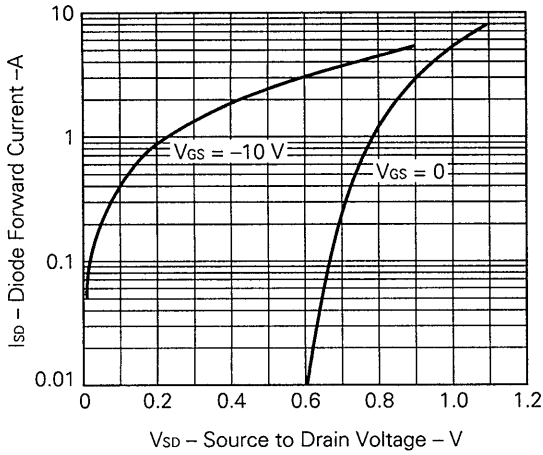


TYPICAL CHARACTERISTICS (T_a = 25 °C)

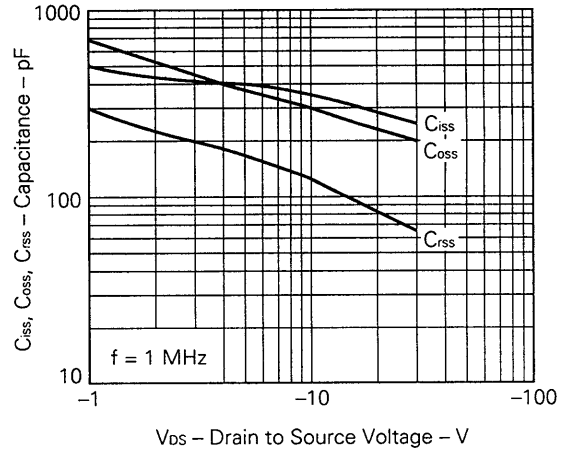




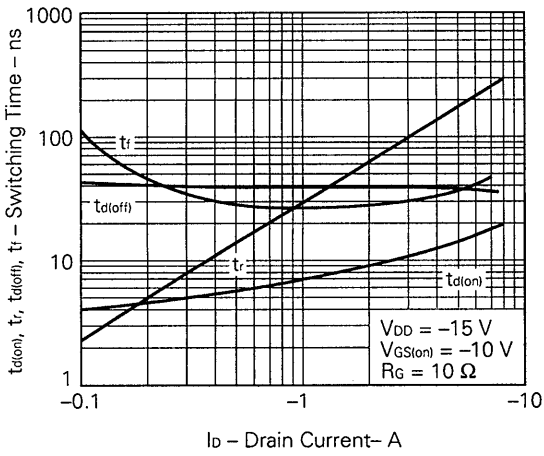
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



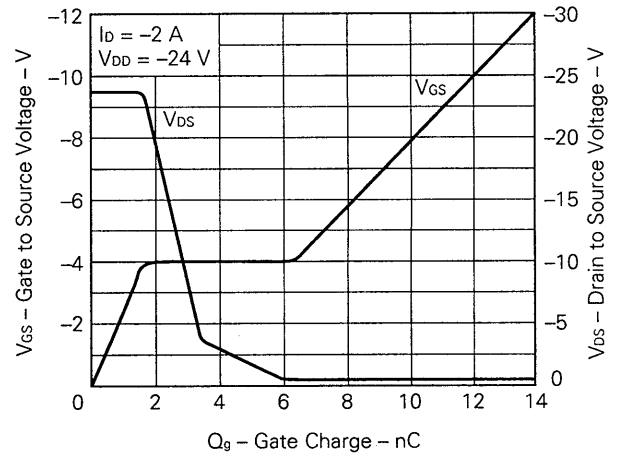
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



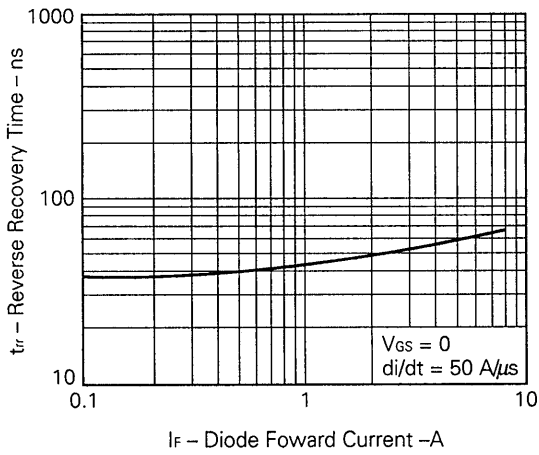
SWITCHING CHARACTERISTICS



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs. REVERSE DRAIN CURRENT



Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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