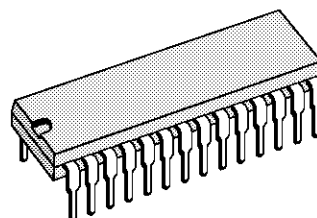


DATA SLICER FOR TELETEXT PROCESSOR

- SEPARATION OF TELETEXT DATA FROM THE COMPOSITE VIDEO SIGNAL
- SEPARATION OF HORIZONTAL AND VERTICAL SYNCHRONIZATION SIGNALS FROM THE COMPOSITE VIDEO SIGNAL
- EXTERNAL OSCILLATOR GENERATING 6MHz SIGNAL SYNCHRONIZED TO A MULTIPLE OF THE LINE FREQUENCY BY PLL
- A 6.9375MHz CLOCK GENERATED FROM AN EXTERNAL QUARTZ CRYSTAL
- "AFTER-HOURS" SYNCHRONIZATION OPTION
- PROGRAMMABLE LEVELS FOR THE INPUT COMPOSITE VIDEO SIGNAL (1V OR 2.5V)
- PROCESSING OF EXTERNAL TELETEXT DATA
- OUTPUT OF POSITIVE OR NEGATIVE SYNCHRONIZING SIGNALS
- 28 PIN DIP PACKAGE
- HDS2P2 TECHNOLOGY

DESCRIPTION

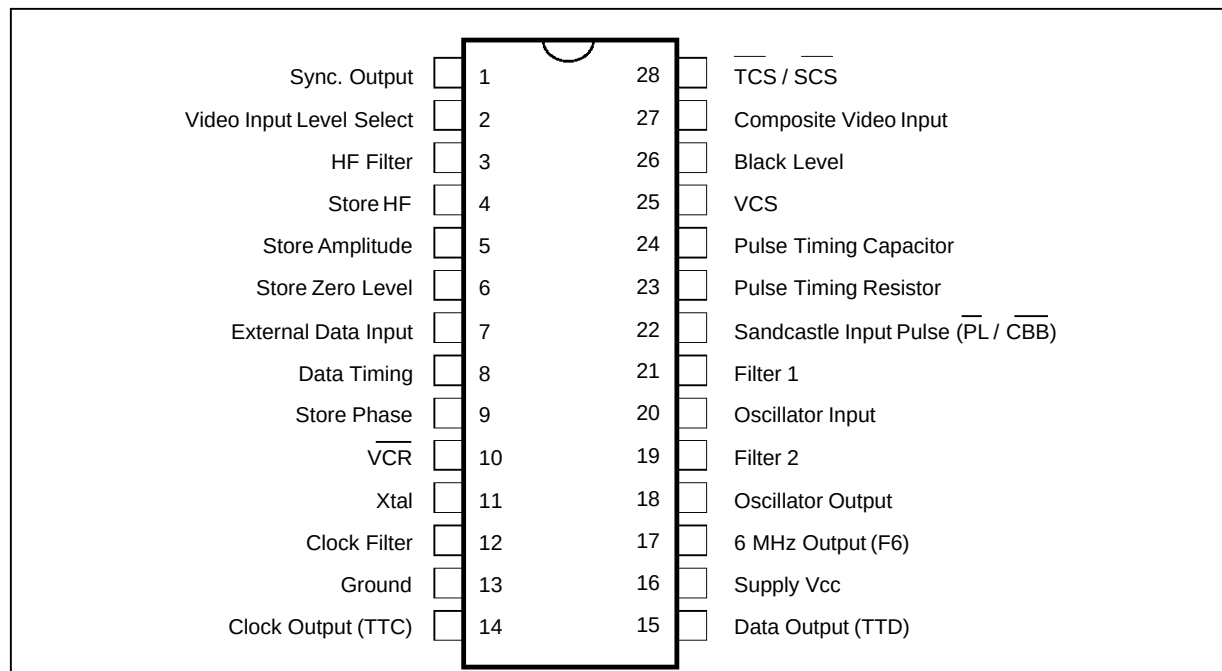
The SAA5231 is a monolithic integrated circuit in 28 Pin DIP package designed to separate Teletext signals from TV signal.



DIP28
(Plastic Package)

ORDER CODE : SAA5231

PIN CONNECTIONS



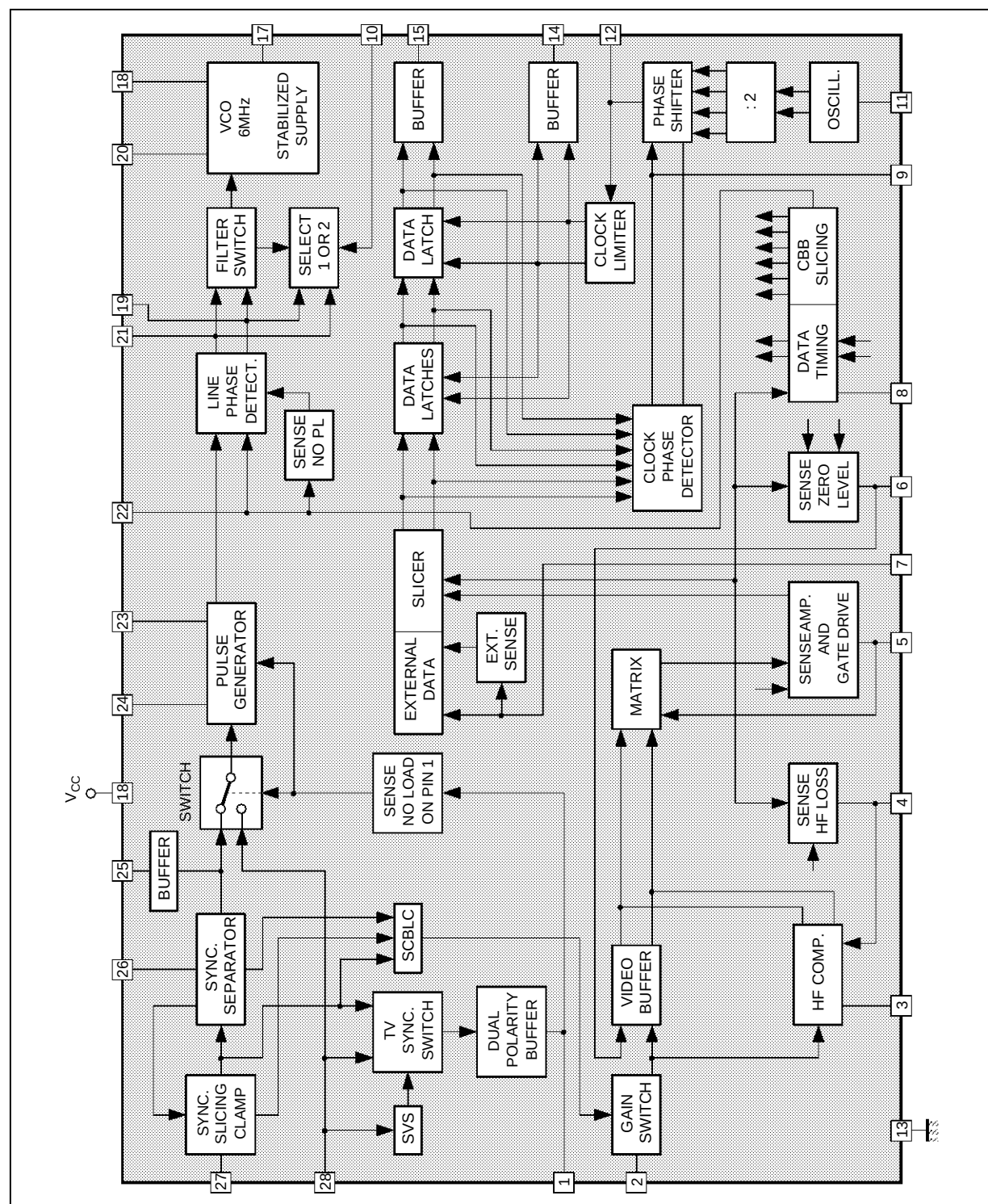
5231-01LEPS

PIN DESCRIPTION

Pin	Function	Description
1	Display Synchronization Outputs	Synchronization signal output available as positive or negative
2	Input video signal level	Input level selected as 1V (Pin 2 low) or 2.5V (Pin 2 not connected)
3	H.F. filter	Video signal filtering using an external capacitor of 15pF
4-5-6	"Store HF" "Store amplitude" "Store zero level"	Three external capacitors used to store : 1/ HF amplitude 2/ Amplitude of adaptative data slicer 3/ Zero level
7	External data input	"Teletext data slice" input from external circuit
8	Data timing	Connection of an external 270pF capacitor for the timing of the adaptative data slicer
9	Store phase	Storage on an external capacitor of the output signal "Clock phase detector"
10	"Video Tape Recorder" mode ($\overline{\text{VCR}}$)	Control signal for the PLL in the low-time constant mode
11	Crystal	External connection for a 13.875MHz crystal. This frequency, divided by 2, yields the 6.9375MHz cloc
12	Clock filter	Filter for 6.9375MHz clock
13	Ground	
14	Teletext clock output	Clock output for the SDA5243
15	Teletext data output	Output of Teletext data for the SDA5243
16	Supply V _{cc}	
17	6MHz clock output	6MHz clock output for the SDA5243
18/20	Oscillator output/input	An external resonant circuit between Pins 18 and 20 is connected to the 6MHz internal V _{CO}
19	Filter 2	Low time constant filter for phase detection of the horizontal signal
21	Filter 1	High time constant filter for phase detection of the horizontal signal
22	"Sandcastle" input pulse	Input of the sandcastle signal produced by the SDA5243 from the PL and CBB signals
23	Pulse timing resistor	External resistor of 68 kohms used to define the current for the pulse generator
24	Pulse timing capacitor	External capacitor of 270pF to define the timing of the pulse generator
25	Composite video synchronizing output (VCS)	Synchronizing output for the SDA5243
26	Black level	Storage of the black level for the adaptive sync. Separator on an external 68nF capacitor
27	Composite video input	Composite video signal input for the adaptive sync. Separator via an external capacitor of 2.2μF
28	Teletext composite sync. input (TCS) or Scan composite sync. input (SCS)	TCS input from the SDA5243 or SCS input from an alternative synchronizing circuit.

5231-01.TBL

BLOCK DIAGRAM



5231-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V ₁₆	Supply Voltage	13.2	V
-I ₂₅	Output Current VCS	5	mA
-I ₁₅	Output Current TTD	10	mA
-I ₁₄	Output Current TTC	10	mA
-I ₁₇	Output Current F6	10	mA
I ₁	Output Current Sync.	5	mA
T _{stg}	Storage Temperature	-40, +150	°C
T _j	Junction	0, +150	°C
T _{amb}	Ambient Temperature	0, +70	°C

5231-02.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th(j-a)}	Thermal Resistance Junction-Ambient Max.	70	°C/W

5231-03.TBL

ELECTRICAL CHARACTERISTICS (V_S = 12 V , T_A = 25°C , unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
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POWER SUPPLY (Pin 16)

V _S	Supply Voltage	10.8	12	13.2	V
I _S	Supply Current		70		mA

CVBS INPUT (Pin 27)

V ₂₇	Input Signal Level Pin 2 to ground Pin 2 open	0.7 1.75	1 2.5	1.4 3.5	v v
V _{27(p-p)}	Synchronism Signal Amplitude	0.1	-	1	V
V _{27(txt)}	Teletext Data Level Pin 2 to ground Pin 2 open	0.3 0.75	0.46 1.15	0.7 1.75	v v
R _{G27}	Generator Resistance			250	Ω

VIDEO INPUT LEVEL SELECT (Pin 2)

V _{2L}	Low Voltage (V ₂₇ = 1V)	0		0.8	V
V _{2H}	High Voltage (V ₂₇ = 2.5V)	2		5.5	V
-I _{2L}	Low Current	0		150	μA
I _{2H}	High Current	0		1.3	mA

TELETEXT DATA(Pin 5)

V _{15(p-p)}	Signal TTD Output	2.5	3.5	4.5	V
t _r , t _f	Transition Times	20	30	45	ns
C ₁₅	Load Capacitance			40	pF
V _{15DC}	DC Voltage at Output		4		V

DATA CLOCK (Pin 14)

V _{14(p-p)}	Signal TTC	2.5	3.5	4.5	V
t _r , t _f	Transition Times	20	30	45	ns
C ₁₄	Load Capacitance			40	pF
t _D	Time Deviation with Respect to TTD	-20	0	20	ns
V _{14DC}	DC Voltage at Output		4		V

SYNC. PULSE SEPARATION VCS (to SDA5243) (Pin 25)

V _{25L}	Low Output Voltage	0		0.4	V
V _{25H}	High Output Voltage	2.1		5.5	V

5231-04.TBL

ELECTRICAL CHARACTERISTICS ($V_S = 12\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified) (continued)

Symbol	Parameter	Min	Typ	Max	Unit
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SYNC. PULSE SEPARATION VCS (to SDA5243) (Pin 25)

I_{25L}	Low Output Current			0.5	mA
$-I_{25H}$	High Output Current			1.5	mA
t_D	Delay with respect to CVBS sync.		0.5		μs

SYNC. OUTPUT DRIVER (to TV set) (Pin 1)

$V_{1(p-p)}$	Output Voltage TCS Operation CVBS Operation		0.45	1	V
V_{1DC}	DC voltage with load resistor to ground (positive synchronous signal)		1.4		V
$-I_1$	Output Current			3	mA
V_{1DC}	DC voltage with load resistor to V_S (negative synchronous signal)		10.1		V
I_1	Output Current			3	mA

6MHz CLOCK F6 (Pin 7)

$V_{17(p-p)}$	F6 Output Signal (negligible harmonic content)	1	2	3	V
t_r, t_f	Transition Times	20		40	ns
C_{17}	Load Capacitance			40	pF
V_{17DC}	DC Voltage	4		8.5	V

SYNCHRONIZATION SELECTION (Pin 28)

$-I_{28}$	Input Current TCS Operation ($V_{28} = 0$ to 7 V)	40	70	100	μA
I_{28}	Input Current CVBS Operation ($V_{28} = 10$ to V_S)	-5	0	5	μA
V_{28L}	Low Input voltage (TCS operation) (load resistor at Pin 1)	0		0.8	V
V_{28H}	High Input voltage (TCS operation) (load resistor at Pin 1)	2		6.1	V
V_{28L}	Low Input Voltage (SCS operation) (Pin 1 open)	0		1.5	V
V_{28H}	High Input Voltage (SCS operation) (Pin 1 open)	3.5		6.1	V
t_p	Line Synchronous Pulse Width TCS Operation SCS Operation		2 3		μs μs

VCR OPERATION (Pin 10)

V_{10L}	Low Input Voltage VCR Operation	0		0.8	V
V_{10H}	High Input Voltage Standard Operation	2		V_S	V
I_{10}	Input Current	-10	0	10	A

SANDCASTLE PULSE INPUT (Pin 22)

V_{22L}	Phase Locked Mode Input Low Voltage PL	0		3	V
V_{22H}	Phase Locked Mode Input High Voltage PL	3.9		5.5	V
t_{pl}	PL - low time for free-wheeling oscillator	100			ms
V_{22L}	Reset Pulse for Data Separation Input Low Voltage CBB	0		0.5	V
V_{22H}	Reset Pulse for Data Separation Input High Voltage CBB	1		5.5	V
I_{22}	Input Current	-10		10	μA

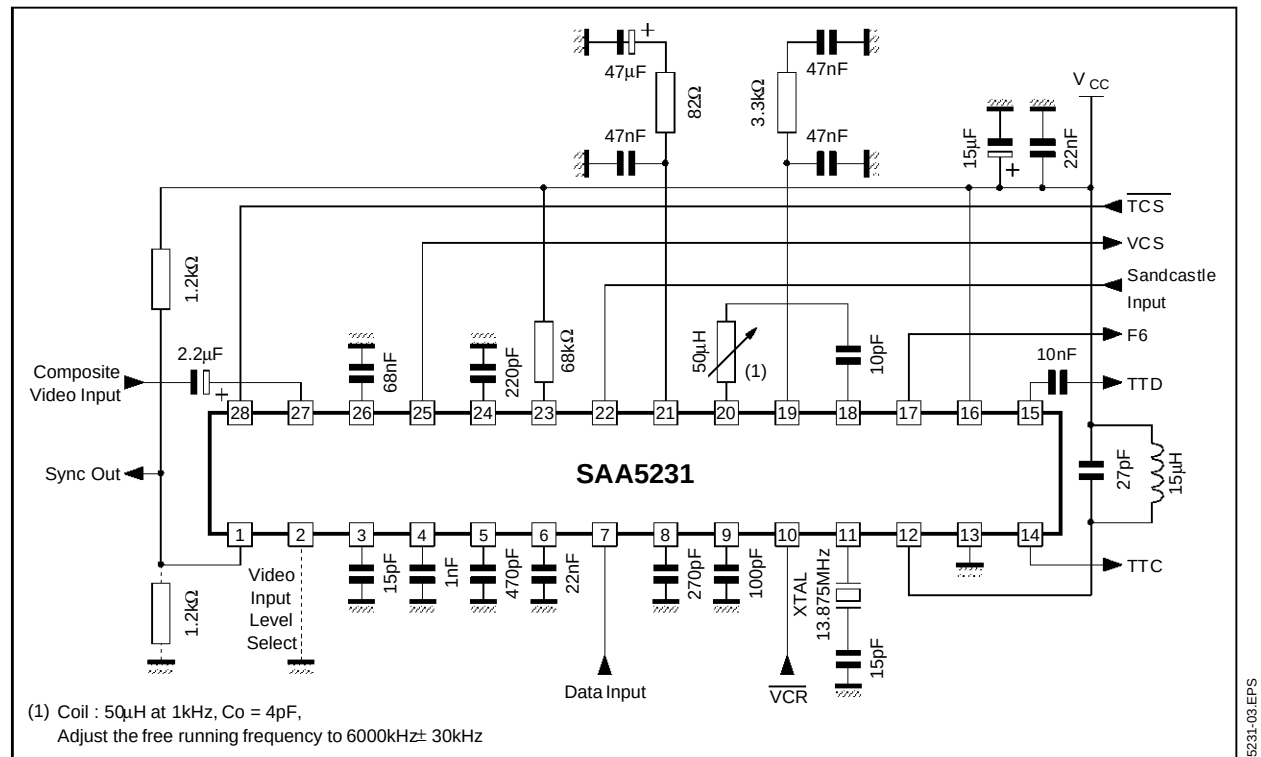
EXTERNAL DATA INPUT (CURRENT SOURCE DRIVING) (Pin 7)

Internal Data Processing Input					
I_7	Current	-10	0	100	μA
V_7	Voltage ($I_7 = -10$ to $100\mu\text{A}$)		10		V
External Data Processing Input					
I_{7L}	Current for low Level	-175	-40	-25	μA
I_{7H}	Current for High Level	-1000	-500	-325	μA
V_7	Voltage ($I_7 = -1000$ to $-25\mu\text{A}$)	7	8		V

5231-05.TBL

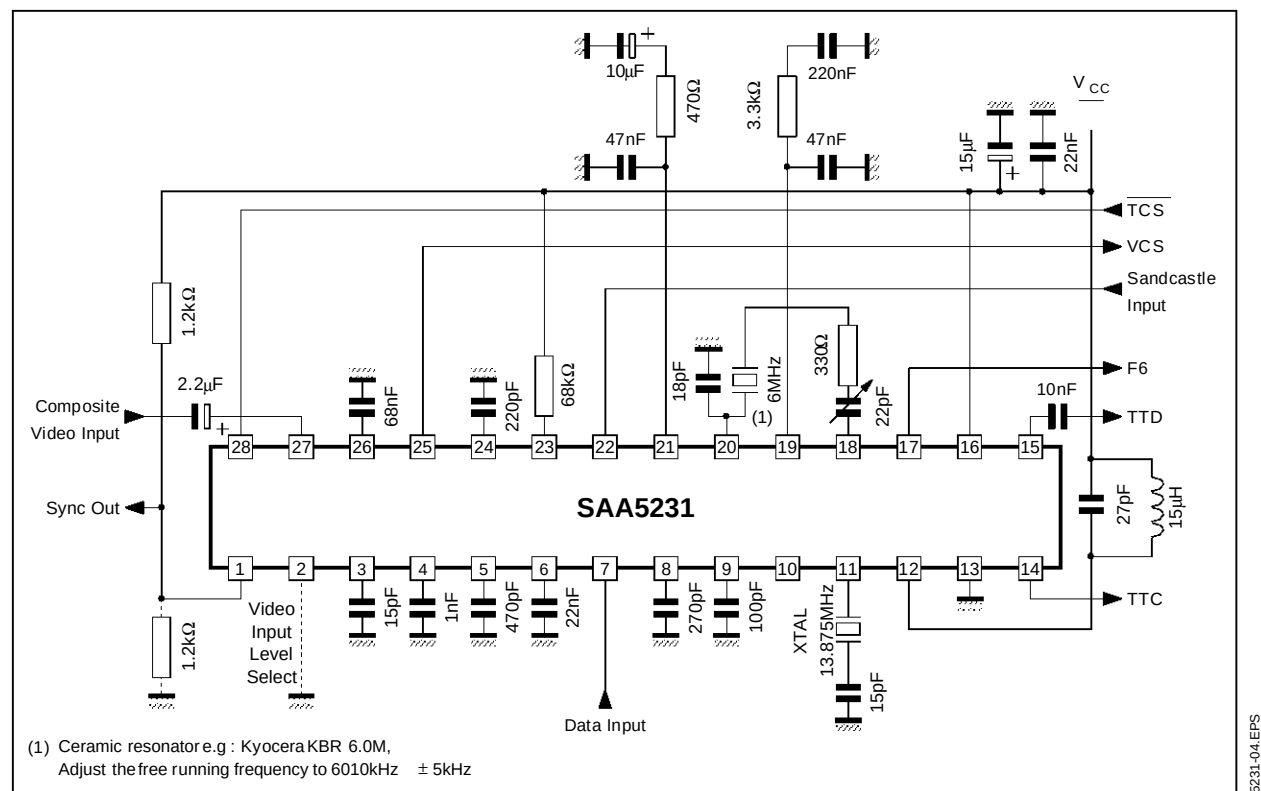
APPLICATION DIAGRAMS

Figure 1a : Application Diagram with LC Circuit in 6MHz PLL



5231-03.EPS

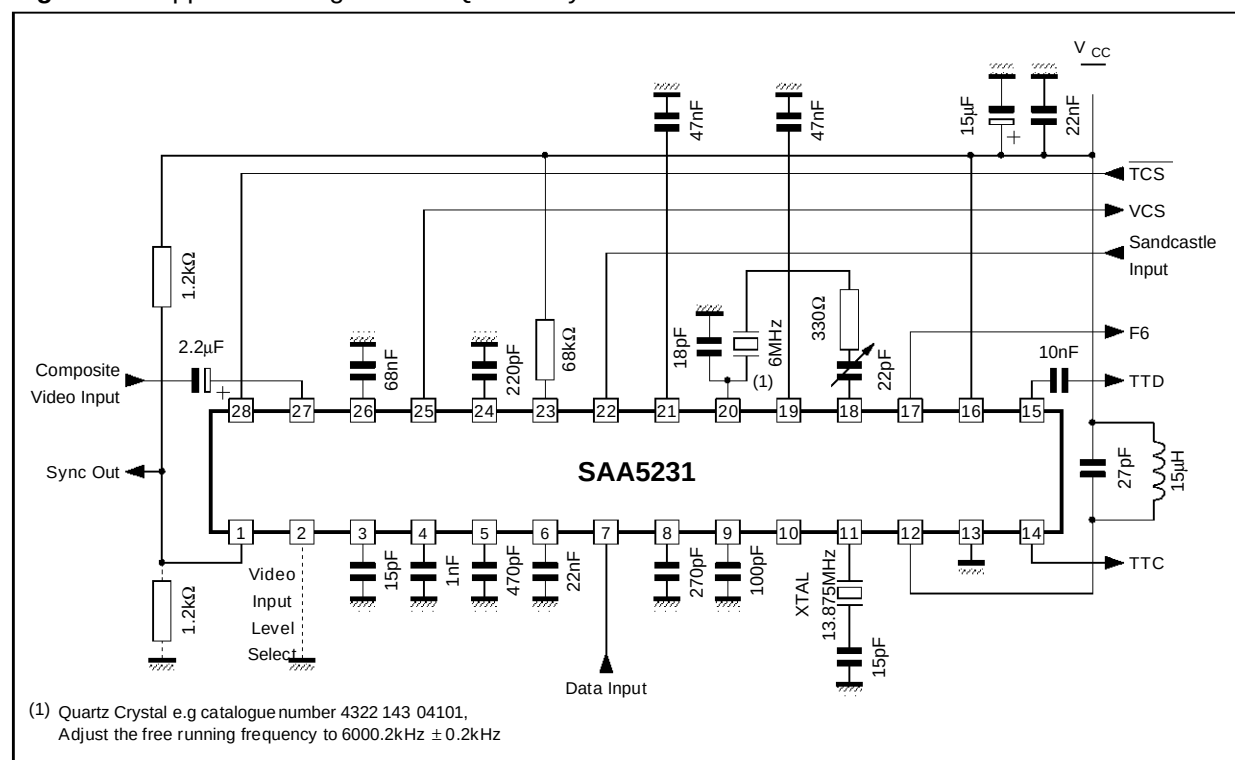
Figure 1b : Application Diagram with Ceramic Resonator in 6MHz PLL



5231-04.EPS

APPLICATION DIAGRAMS (continued)

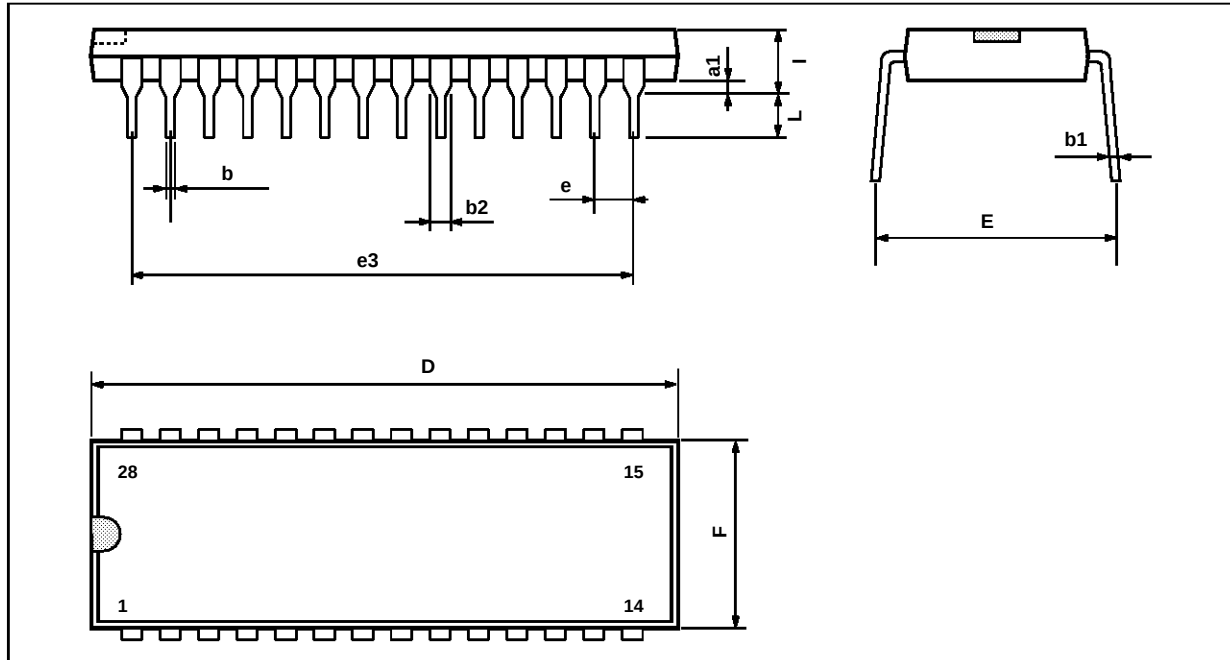
Figure 1c : Application Diagram with Quartz Crystal in 6MHz PLL



5231-05 EPS

PACKAGE MECHANICAL DATA

28 PINS - PLASTIC DIP



PM-DIP28.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.4			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

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