AN3313, AN3313S

Head Amplifier Circuits for VTR (2-Head Type)

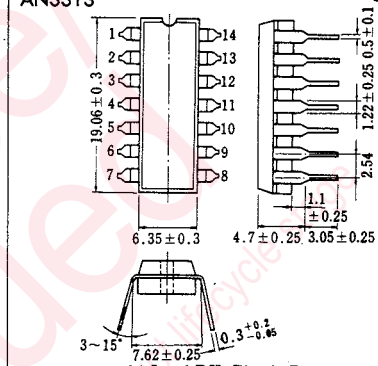
■ Outline

The AN3313 and the AN3313S are integrated circuits designed for head amplifier circuits for VTR (2-head type).

■ Features

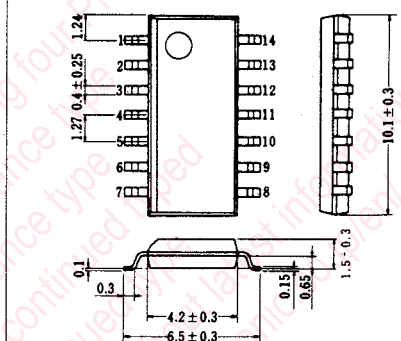
- Supply voltage : V_{CC}=5V
- Built-in peaking amplifier circuit
- Less noise voltage to input (1 μ Vrms)

AN3313 Unit : mm



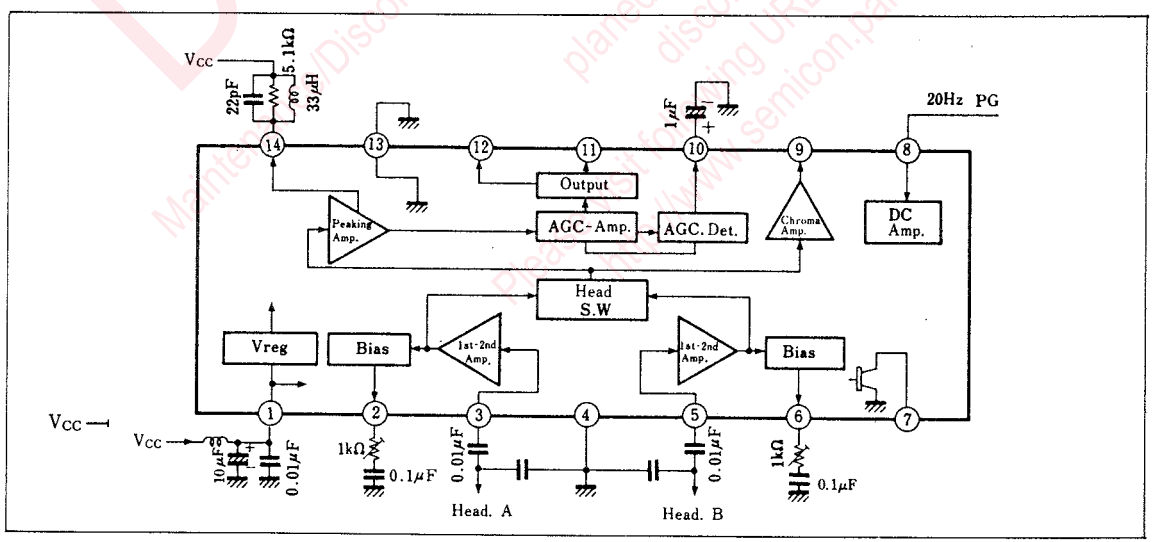
14-Lead DIL Plastic Package

AN3313S Unit : mm



14-Lead PANAFLAT Package (SO-14D)

■ Block Diagram



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	8	PG Pulse Input
2	CH1 Damping Adjustment	9	Chroma Signal Output
3	CH1 Input	10	AGC Level Detection
4	GND	11	AGC Output B
5	CH2 Input	12	AGC Output A
6	CH2 Damping Adjustment	13	GND
7	ON Switch at PB	14	Peaking

■ Absolute Maximum Ratings (Ta=25℃)

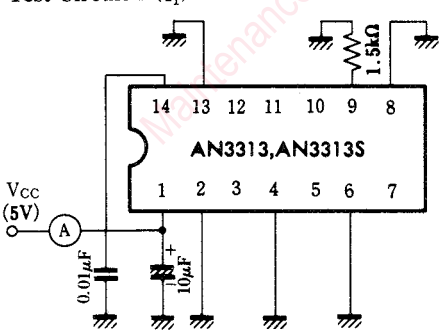
Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	6.0	V
Power Dissipation(Ta=70℃)	P_D	130	mW
Operating Ambient Temperature	T_{opr}	−20~+70	℃
Storage Temperature	T_{stg}	−55~+150	℃

■ Electrical Characteristics (V_{CC}=5V, Ta=25℃)

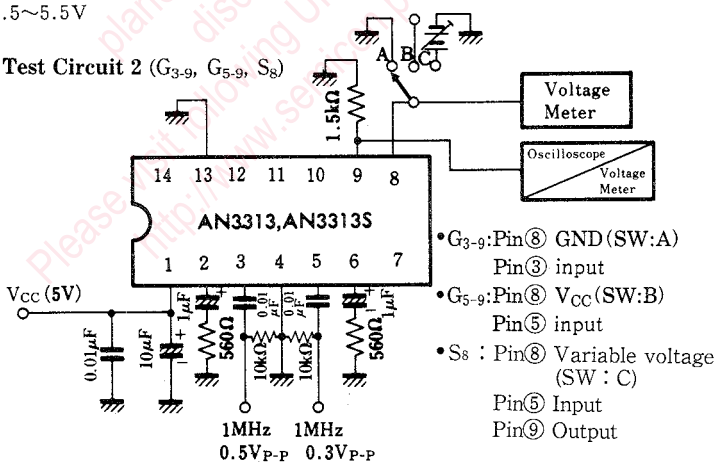
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit Current	I_1	1	②, ⑥, ⑧ GND. ⑨ 1.5×Ω GND. ⑭ V_{CC}	10		24	mA
Ch1 Gain	$G_{3\text{-}9}$	2	③ 1MHz, 0.5mV_{P-P}. ⑨ Out	52.5		62.5	dB
Ch2 Gain	$G_{5\text{-}9}$	2	⑤ 1MHz, 0.5mV_{P-P}. ⑨ Out	52.5		62.5	dB
AGC Output Amplitude	v_{12}	3	③ 4MHz, 0.3mV_{P-P}. ⑫ Out	154		286	mV_{P-P}
AGC Control Sensitivity	Δv_{12}	3	③ 4MHz, 0.3mV_{P-P}. ⑫ Out			3	dB
PG Switch Changeover Sensitivity	S_8	2	③ 1MHz, 0.5mV_{P-P}. ⑥ GND ⑧ Varible voltage⑨out			3.5	V
Noise Voltage Referred to Input(1)	V_{ni1}	4	⑧ GND ⑨ Out 1MHz BPF added			1	μV_{rms}
Noise Voltage Referred to Input(2)	V_{ni2}	4	⑧ V_{CC} ⑨ Out 1MHz BPF added			1	μV_{rms}

Note : Operating supply voltage range $V_{CC(opr)}$=4.5~5.5V

Test Circuit 1 (I_1)



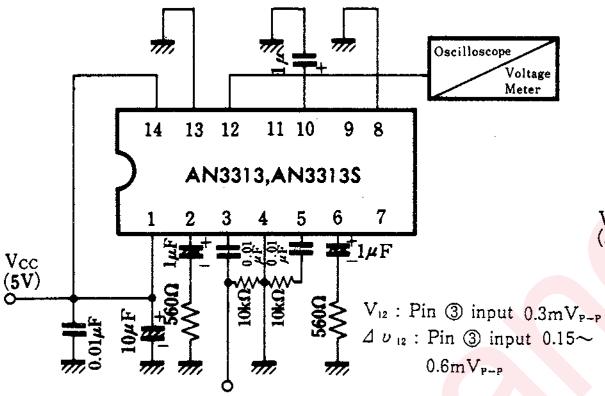
Test Circuit 2 ($G_{3\text{-}9}$, $G_{5\text{-}9}$, S_8)



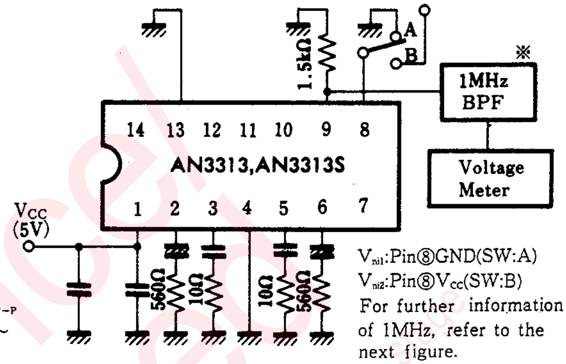
- $G_{3\text{-}9}$: Pin⑧ GND (SW:A) Pin③ input
- $G_{5\text{-}9}$: Pin⑧ V_{CC} (SW:B) Pin⑤ input
- S_8 : Pin⑧ Variable voltage (SW : C) Pin⑤ Input Pin⑨ Output

Increasing the electric potential of Pin ⑧ from 0V, measure the electric potential of Pin ⑧ when Pin ⑨ output appears.

Test Circuit 3 (v_{12}, Δv_{12})

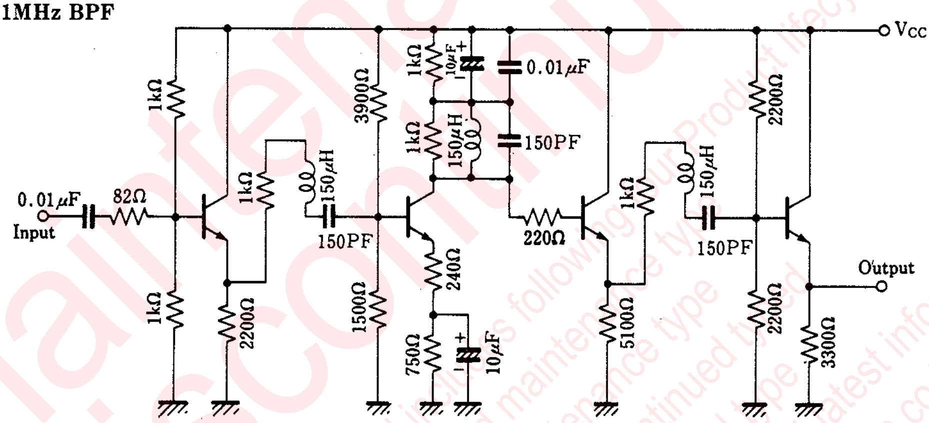


Test Circuit 4 (V_{ni1}, V_{ni2})

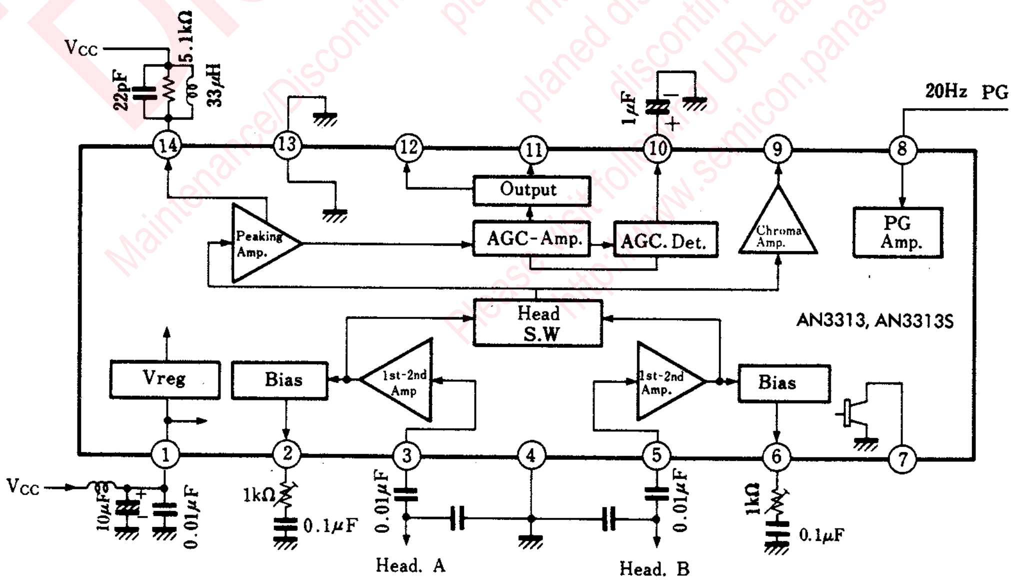


V_{ni1}:Pin⑧GND(SW:A)
V_{ni2}:Pin⑧V_{cc}(SW:B)
For further information of 1MHz, refer to the next figure.

※ 1MHz BPF



■ Application Circuit



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