

AN3320K, AN3320S

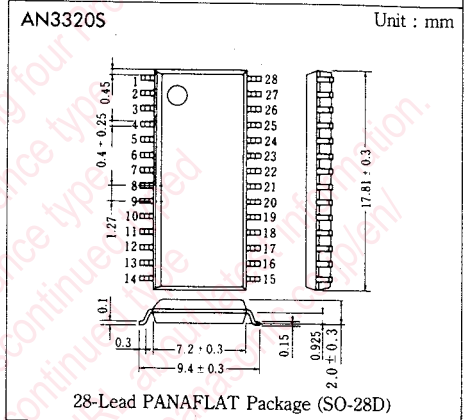
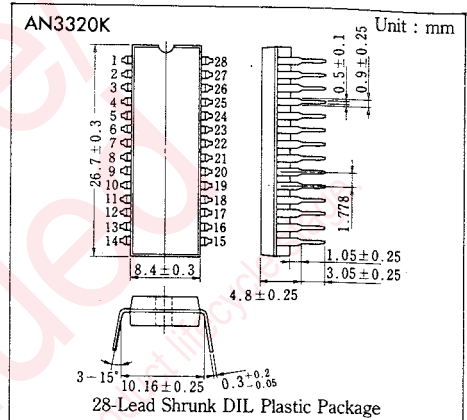
VTR Playback Video Signal Processing Circuits

■ Outline

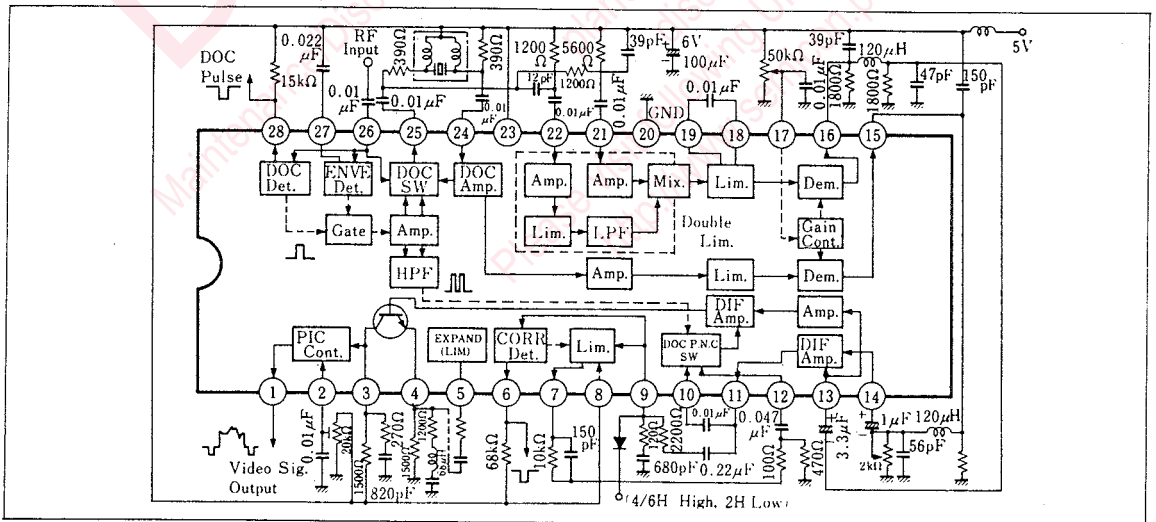
The AN3320K and the AN3320S are integrated circuits designed for VTR playback video signal processing circuits.

■ Features

- Built-in line noise canceler
- Built-in picture control circuit
- Supply voltage : $V_{cc}=5V$



■ Block Diagram



■ Absolute Maximum Ratings (Ta=25°C)

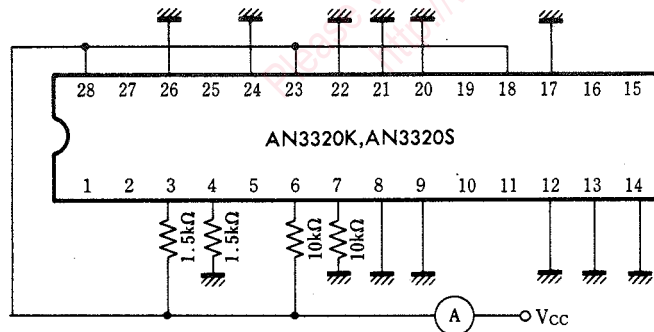
Item	Symbol	Rating	Unit
Supply Voltage	V _{CC}	6.0	V
Power Dissipation(Ta=70°C)	P _D	200	mW
Operating Ambient Temperature	T _{opr}	-20~+70	°C
Storage Temperature	T _{stg}	-55~+150	°C

■ Electrical Characteristics (V_{CC}=5V, Ta=25°C)

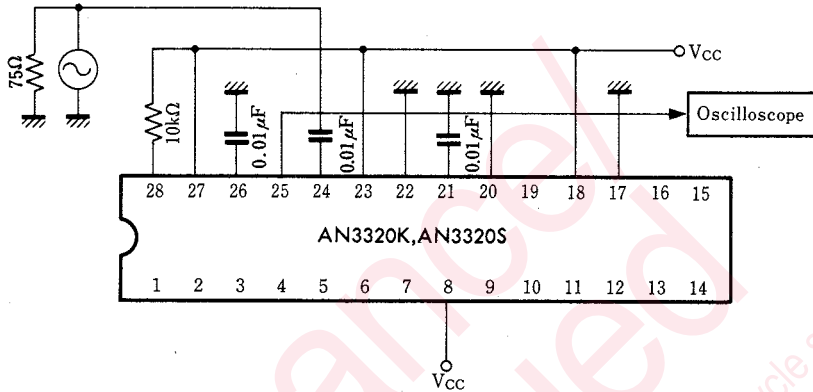
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit Current	I ₂₃	1		17		30	mA
DOC Ampl. Gain	G ₂₅	2	Pin ⑭ Input (60mV _{P-P} , 4MHz)	13		16	dB
DOC Sensitivity ON	S ₂₈	3	Pin ⑮ Input (4MHz), 0 dB=350mV _{P-P}	-15		-11.5	dB
DOC Sensitivity OFF(Hysteresis)	ΔS ₂₈	3	Pin ⑮ Input (4MHz), 0 dB=350mV _{P-P}	-5		-0.5	dB
Sub FM Demodulation Det. Sensitivity	S ₁₅	4	Pin ⑭ Input (50mV _{P-P}) ⑰ 3.5V F ₁₁ is multiplied by Gain(0dB=250mV)	2.5			dB
Sub FM Demodulation Det. Limitation	L _{f15}	4	Pin ⑭ Input (100mV _{P-P}) Pin ⑰ 3.5V	7			MHz
Main FM Demodulation Det. Sensitivity	S ₁₆	5	Pin ⑰ Input (150mV _{P-P}) ⑰ 3.5V F ₁₁ is multiplied by Gain(0dB=250mV)	2.5			dB
Main FM Demodulation Det. Limitation	L _{f16}	5	Pin ⑰ Input (100mV _{P-P}) ⑰ 3.5V	7			MHz
Difference Det. Amp. Gain A	G ₁₁₋₁	6	Pin ⑬ Input (100mV _{P-P} , 1MHz)	13.5		16.5	dB
Difference Det. Amp. Gain B	G ₁₁₋₂	6	Pin ⑬ Input (100mV _{P-P} , 1MHz)	12		15	dB
Differential + MIX Amp. Gain	G ₄₋₁	7	Same as above	7		10	dB
MIX Amp. Ratio	G ₄₋₂	7	Pin ⑫ Input (500mV _{P-P} , 1MHz)	-5.5		-2.5	dB
Line Noise Canceler Switch Changeover Level Difference	Δv ₄	8	Pin ⑩ Control Pulse	-5		5	mV
Line Noise Canceler Switch Crosstalk	CT ₄	9	500mV _{P-P} , 1MHz ④ Output ratio of ⑩ and ⑫			-40	dB
Line Noise Canceler Limiter Gain	G ₇	10	Pin ⑨ Input (40mV _{P-P} , 1MHz)	15.5		19	dB
Line Noise Canceler Correlative Det. Sensitivity ON	S ₆	11	Pin ⑨ Input (4MHz), 0dB=60mV _{P-P}	1.5		4.5	dB
Line Noise Canceler Correlative Det. Sensitivity OFF(Hysteresis)	ΔS ₆	11	Pin ⑨ Input (4MHz), 0dB=60mV _{P-P}	-4		-0.1	dB
Picture Control Gain	G ₁	12	Pin ③ Input (250mV _{P-P} , 1MHz) Output ratio of Pin②0V and 2.5V	-1.5		0.5	dB
Picture Control Frequency Characteristics A	f ₁₋₁	12	Pin ③ Input (250mV _{P-P} , 1MHz)			-3	dB
Picture Control Frequency Characteristics B	f ₁₋₂	12	Pin ③ Input (250mV _{P-P} , 1MHz) Output ratio of Pin⑤5V and 2.5V	5			dB

Note : Operating Supply Voltage Range : V_{CC(oper)} = 4.5~5.5V

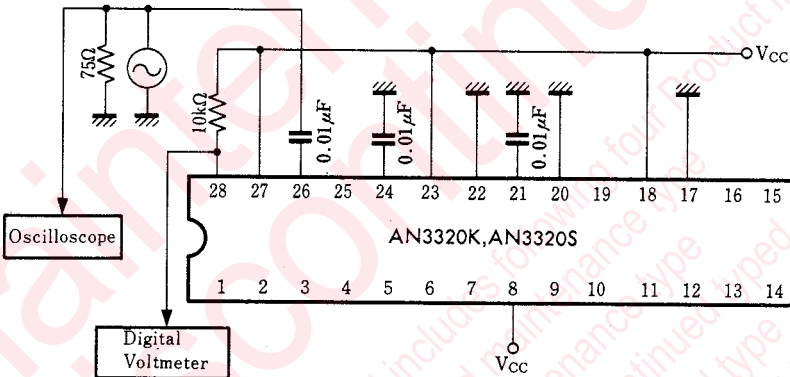
Test Circuit 1 (I₂₃)



Test Circuit 2 (G_{25})

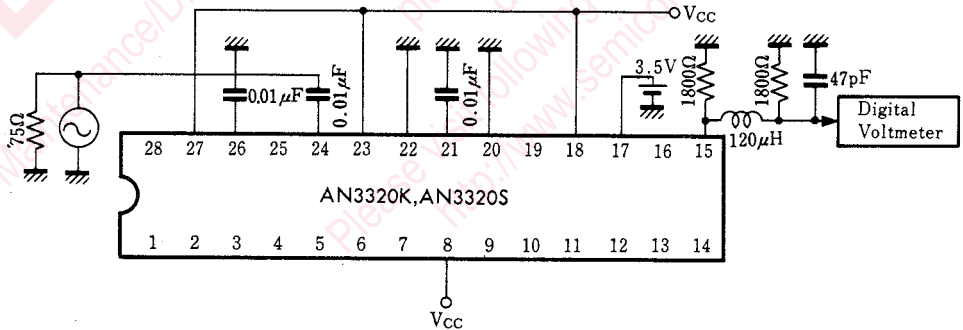


Test Circuit 3 (S_{28} , ΔS_{28})



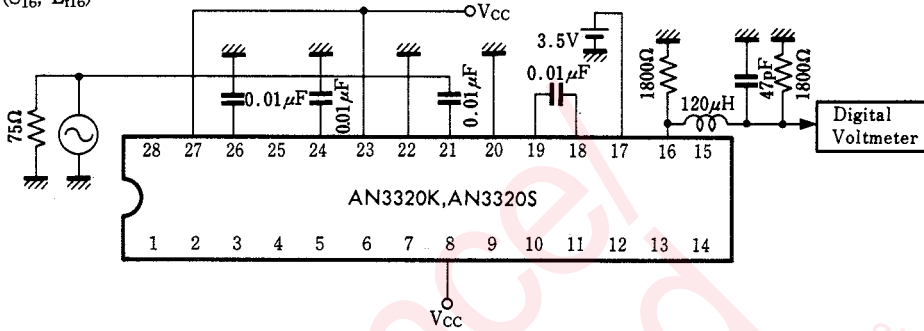
- S_{28-1} : Input level when Pin 28 output goes to Low
- S_{28-2} : Difference between input level and S_{28-1} when Pin 28 output goes to High

Test Circuit 4 (S_{15} , L_{15})



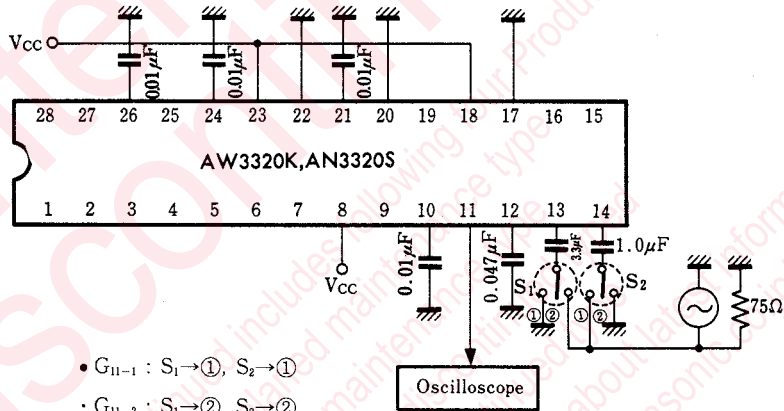
- S_{15} : Pin 15 output difference of input frequency 3.5MHz and 4.5MHz for Pin 24 is multiplied by F_{11} differential + Mix. Amp. gain.
- L_{15} : Pin 24 input frequency when Pin 15 output changes

Test Circuit 5 (S_{16} , L_{116})



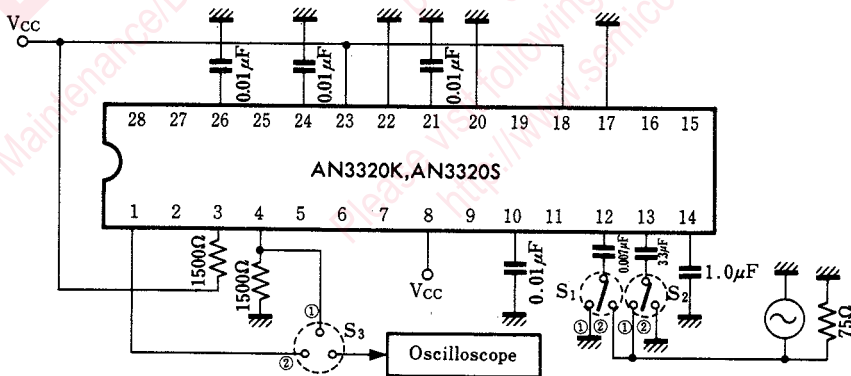
- S_{16} : Pin ⑮ output difference of input frequency 3.5MHz and 4.5MHz for Pin ⑳ is multiplied by F_{11} differential + Mix. Amp. gain.
- L_{116} : Pin ㉑ input frequency when Pin ⑮ output changes

Test Circuit 6 (G_{11-1} , G_{11-2})



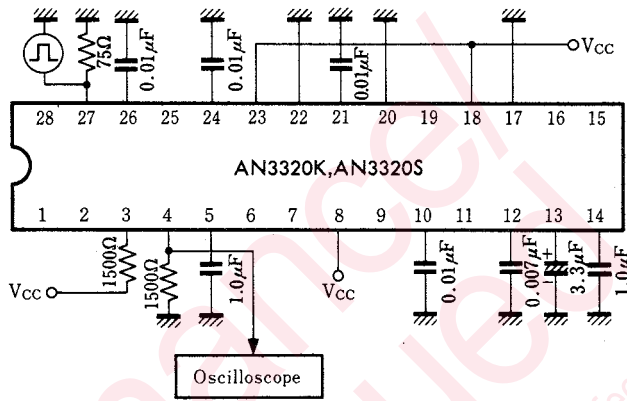
- G_{11-1} : $S_1 \rightarrow ①$, $S_2 \rightarrow ①$
- G_{11-2} : $S_1 \rightarrow ②$, $S_2 \rightarrow ②$

Test Circuit 7 (G_{4-1} , G_{4-2})

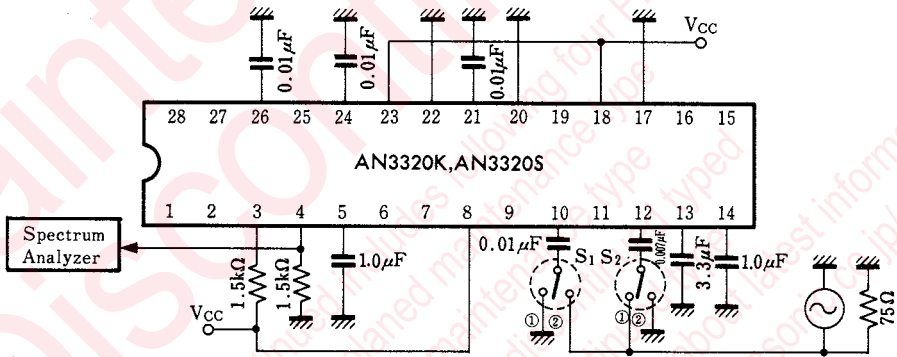


- G_{4-1} : $S_1 \rightarrow ①$, $S_2 \rightarrow ①$, $S_3 \rightarrow ②$
- G_{4-2} : $S_1 \rightarrow ②$, $S_2 \rightarrow ②$, $S_3 \rightarrow ①$

Test Circuit 8 (Δv_4)

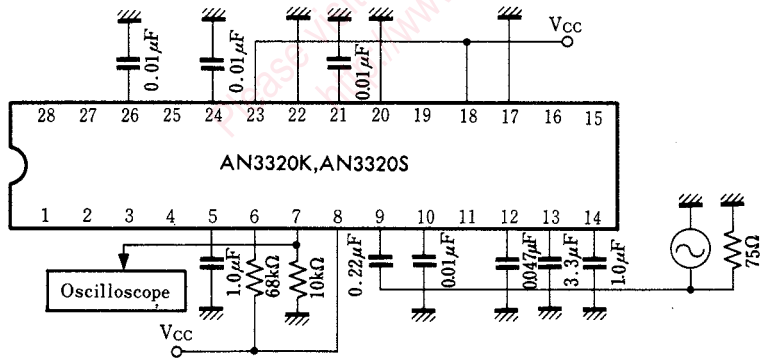


Test Circuit 9 (CT₄)

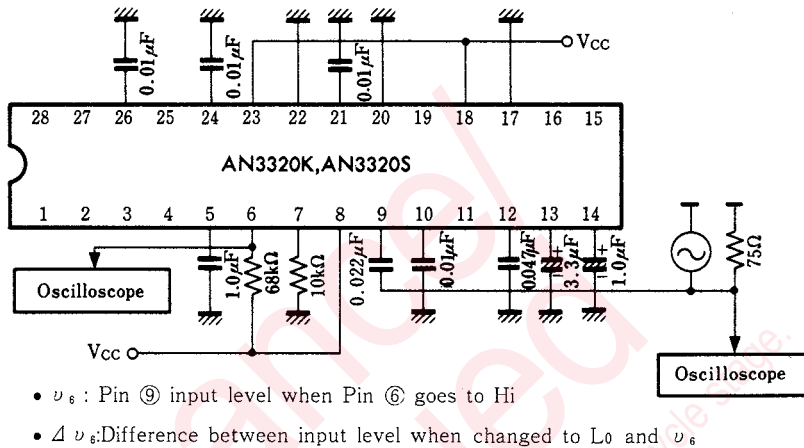


• CT₄: Pin ④ output for Pin ⑫ and element ratio for Pin ⑩ input corresponding to element

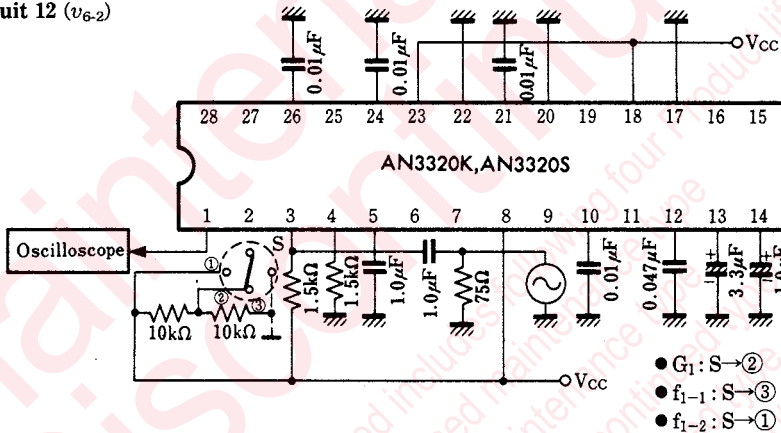
Test Circuit 10 (G₇)



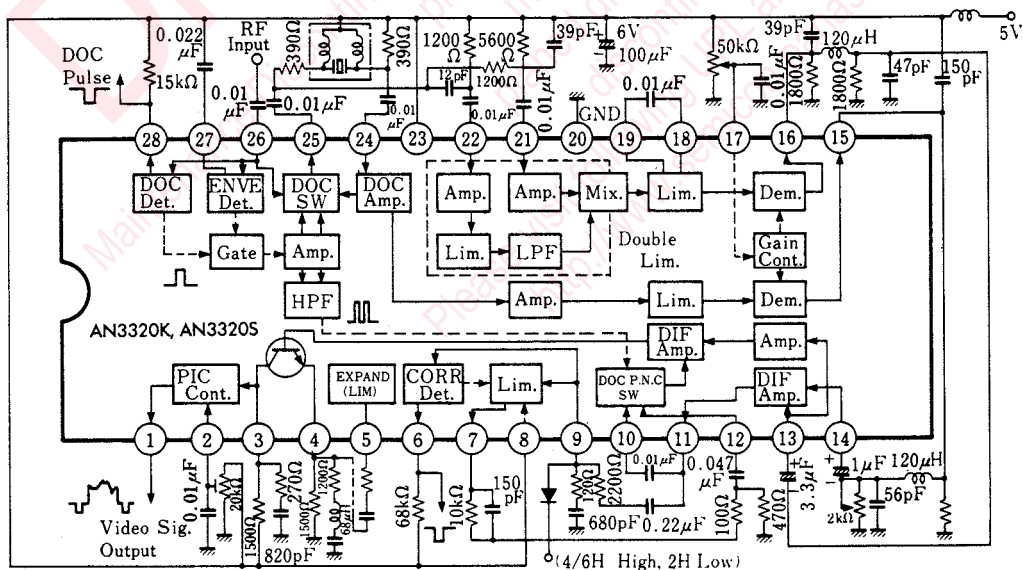
Test Circuit 11 (v_{6-1} , v_{6-2})



Test Circuit 12 (v_{6-2})



Application Circuit



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	Video Output	15	DEM(1H DL)Output
2	Picture Control	16	DEM Output
3	De-emphasis	17	DEM Gain Control
4	Peaking	18	LIM
5	Extension	19	LIM
6	Relative Detecting Pulse Output	20	GND
7	Line N.C. LIM. Output	21	Double LIM LPF Input
8	To Except Rec V _{cc}	22	Double LIM HPF Input
9	Line N.C. LIM. Input	23	V _{cc}
10	Diff. Sig. Input	24	1H Delay RF Input
11	Diff. Sig. Output	25	RF Output
12	Limited Sig. Input	26	RF Input
13	Video Input	27	Envelop DET
14	Video(1H DL)Input	28	DOC Pulse Output

Notes for Use

- Pin ⑧ shall be always used in connection with Pin ⑭
- Power supply to be supplied to the variable resistor added to Pins ② and ⑰ shall be used the same as that supplied to this integrated circuit.
- Since deterioration or destory of characteristics due to flow of overcurrent caused by reverse current, careful attention should be taken to handling.

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