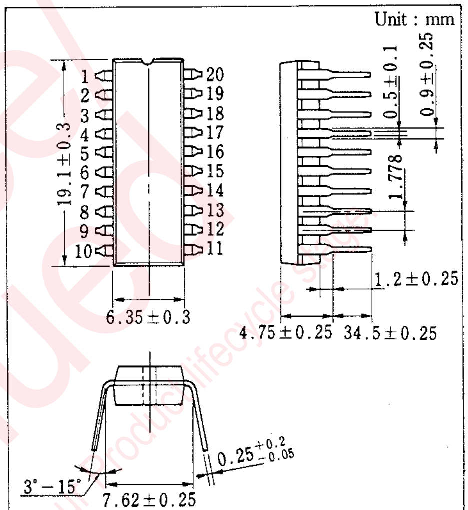
AN3920K

RF Amplifier Circuit for FM Audio of VTRs

■ Outline

The AN3920K is an integrated circuit designed as an RF amplifier for an FM audio of a VTR.

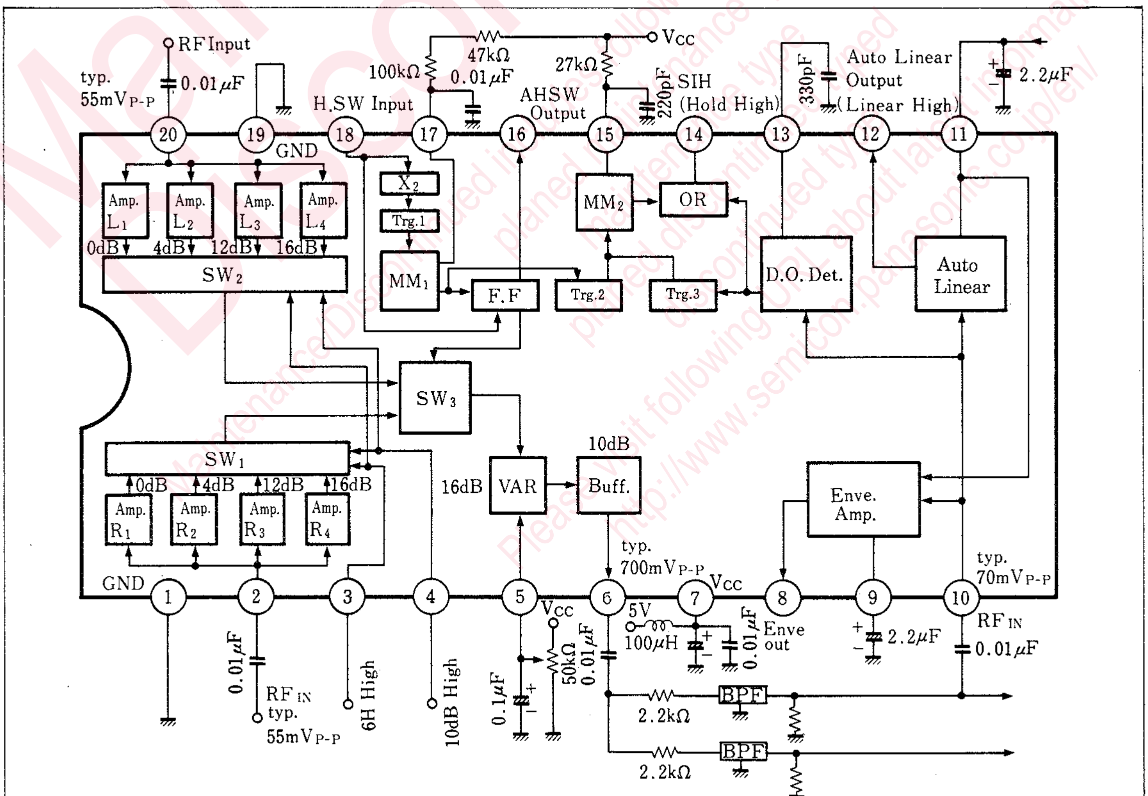


20-Lead Shrunk DIL Plastic Package

■ Features

- Operated by low power supply voltage : Vcc=5V
- Built-in audio-head switch
- Built-in variable amplifier circuit
- Built-in envelope output circuit

■ Block Diagram



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	GND	11	Auto Linear Detection Terminal
2	RF (R-ch) Input Terminal	12	Linear High Output Terminal
3	6H High Input Terminal	13	D.O. Detection Terminal
4	+12dB High Input Terminal	14	S/H Output Terminal
5	Variable Amplifier Control Terminal	15	M.M. 2
6	RF Output Terminal	16	A.H. SW Output Terminal
7	V_{cc}	17	M.M. 1
8	Envelope Output Terminal	18	H. SW Input Terminal
9	Envelope Detection Terminal	19	GND
10	RF Input Terminal	20	RF (L-ch) Input Terminal

■ Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	6.0	V
Power Dissipation(Ta=70℃)	P_D	230	mW
Operating Ambient Temperature	T_{opr}	−20～+70	℃
Storage Temperature	T_{stg}	−55～+150	℃

■ Electrical Characteristics (Vcc=5V, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Supply Current	I_{CC}	1		13		32	mA
Amp. R3 Gain (Max.)	G_{R3}	2	Pin ③…Low, Pin ④…High Input 28mV_{P-P}, f= 1.3MHz	28			dB
Amp. R4 Gain Difference	ΔG_{R4}	2	Pin ③ and Pin ④…High Input 18mV_{P-P}, f=1.3MHz	1.7		6.3	dB
Amp. R2 Gain Difference	ΔG_{R2}	2	Pin ③…High, Pin ④…Low Input 70mV_{P-P}, f=1.3MHz	−11		−5	dB
Amp. R1 Gain Difference	ΔG_{R1}	2	Pin ③ and Pin ④…Low Input 110mV_{P-P}, f=1.3MHz	−15		−9	dB
R1/L1 Gain Difference	ΔG_1	2	Pin ③ and Pin ④…Low Input 110mV_{P-P}, f=1.3MHz	−2		2	dB
R2/L2 Gain Difference	ΔG_2	2	Pin ③…High, Pin ④…Low Input 70mV_{P-P}, f=1.3MHz	−2		2	dB
R3/L3 Gain Difference	ΔG_3	2	Pin ③…Low, Pin ④…High Input 28mV_{P-P}, f=1.3MHz	−2		2	dB
R4/L4 Gain Difference	ΔG_4	2	Pin ③ and Pin ④…High Input 18mV_{P-P}, f=1.3MHz	−2		2	dB
Amp. R3 Gain (Min.)	G_{R3M}	2	Pin ③…Low, Pin ④…High Input 28mV_{P-P}, f=1.3MHz			16	dB
6H High Threshold Level	V_{TH3}	2		3		3.8	V
Pin 4 High Threshold Level	V_{TH4}	2		2.2		3	V
Dropout Detection Sensitivity	$S_{10\text{-}14}$	3	Pin ⑩ Input f=1.3MHz Let 70mV_{P-P}=0dB	−19		−13	dB
S/H Output High Level	V_{14}	3	I_{OUT}=−0.1mA	3.11			V

Note) Range of the Operating Supply Voltage : $V_{CC(opr)}$=4.5 to 5.5V

■ Electrical Characteristics (Cont'd)(Ta=25℃)

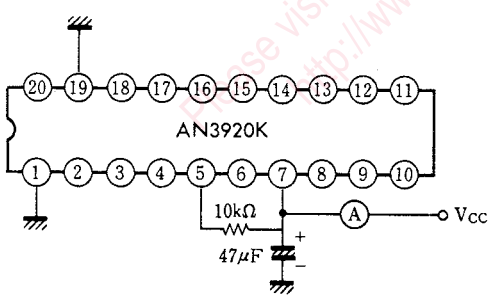
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Linear Switching Sensitivity	$S_{10\text{-}12}$	3	Pin ⑩ Input f=1.3MHz Let 70mV_{P-P}=0dB.	−13		−7	dB
Linear Output High Level	V_{12}	3	I_{OUT}=−1mA	3.5			V
Envelope Output Halt Level	V_{11}	3		3.7			V
HSW Input Voltage High Level	V_{18H}	4		3			V
HSW Input Voltage Low Level	V_{18L}	4				0.8	V
A.H. SW Output High Level	V_{16H}	4	I_{OUT}=−1mA	3.5			V
A.H. SW Output Low Level	V_{16L}	4	I_{OUT}=−1mA			1.5	V
Supply Current	I_{CC}*1	1			23		mA
Amp. R3 Gain	G_{R3T}*1,2	5	Pin ③…Low, Pin ④…High Input 55mV_{P-P}, f=1.3MHz		22		dB
Amp. R4 Gain Difference	ΔG_{R4T}*1,2	5	Pin ③ and Pin ④…High Input 34.7mV_{P-P}, f=1.3MHz		4		dB
Amp. R2 Gain Difference	ΔG_{R2T}*1,2	5	Pin ③…High, Pin ④… Low Input 138mV_{P-P}, f=1.3MHz		−8		dB
Amp. R1 Gain Difference	ΔG_{R1T}*1,2	5	Pins ③ and ④…Low Input 219mV_{P-P}, f=1.3MHz		−12		dB
6H High Threshold Level	V_{TH3}*1	2			3.5		V
Pin 4 High Threshold Level	V_{TH4}*1	2			2.6		V
Dropout Detection Sensitivity	$S_{10\text{-}14}$*1	3	Pin ⑩ Input f= 1.3MHz Let 70mV_{P-P}=0dB		−16		dB
Dropout Hysteresis	$\Delta S_{10\text{-}14}$*1	3	Pin ⑩ Input f=1.3MHz Let 70mV_{P-P}=0dB.	1	3	5	dB
Linear Switching Detection Sensitivity	$S_{10\text{-}12}$*1	3	Pin ⑩Input f=1.3MHz Let 70mV_{P-P}=0dB.		−10		dB
Linear Switching Hysteresis	$\Delta S_{10\text{-}12}$*1	3	Pin ⑩ Input f=1.3MHz Let 70mV_{P-P}=0dB.	1	3	5	dB
Envelope Output Level	V_8*1	3	Pin ⑩ Input f=1.3MHz 70mV_{P-P}	2.3	2.75	3.2	V

Note) Range of the Operating Supply Voltage : $V_{CC(opr)}$=4.5 to 5.5V

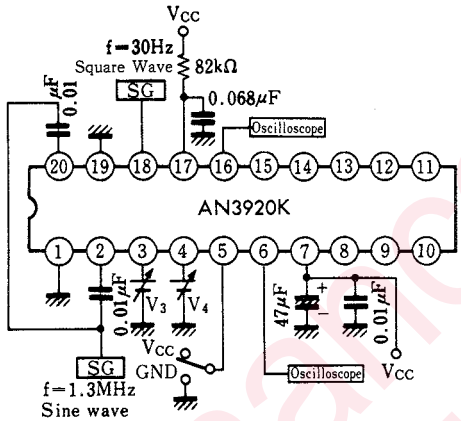
*1. There are reference values for designing and not a guaranteed ones.

*2. Pin ⑤ voltage are regulated so that the Amp. R3 gain of Pin ⑥ to Pin ② will be 22dB.

Test Circuit 1 (I_{CC})



Test Circuit 2 (G_{R3}, ΔG_{R4}, ΔG_{R2}, ΔG_{R1}, ΔG_1, ΔG_2, ΔG_3, ΔG_4, G_{R3M}, V_{TH3}, V_{TH4})



Gain	Input Pin	Input Level	Pin③	Pin④	Pin⑤	Measurement
G_{R4}	Pin②	$18mV_{P-P}$	High	High	GND	Pin⑥ Output Level in the Case Where Pin⑯ is High
G_{R3}	Pin②	$28mV_{P-P}$	Low	High	GND	Pin⑥ Output Level in the Case Where Pin⑯ is High
G_{R2}	Pin②	$70mV_{P-P}$	High	Low	GND	Pin⑥ Output Level in the Case Where Pin⑯ is High
G_{R1}	Pin②	$110mV_{P-P}$	Low	Low	GND	Pin⑥ Output Level in the Case Where Pin⑯ is High
G_{L4}	Pin⑳	$18mV_{P-P}$	High	High	GND	Pin⑥ Output Level in the Case Where Pin⑯ is Low
G_{L3}	Pin⑳	$28mV_{P-P}$	High	High	GND	Pin⑥ Output Level in the Case Where Pin⑯ is Low
G_{L2}	Pin⑳	$70mV_{P-P}$	Low	Low	GND	Pin⑥ Output Level in the Case Where Pin⑯ is Low
G_{L1}	Pin⑳	$110mV_{P-P}$	Low	Low	GND	Pin⑥ Output Level in the Case Where Pin⑯ is Low
G_{R3M}	Pin②	$28mV_{P-P}$	High	High	Vcc	Pin⑥ Output Level in the Case Where Pin⑯ is High

*A Square wave (f=30Hz, 0→5V) is input Pin ⑱.

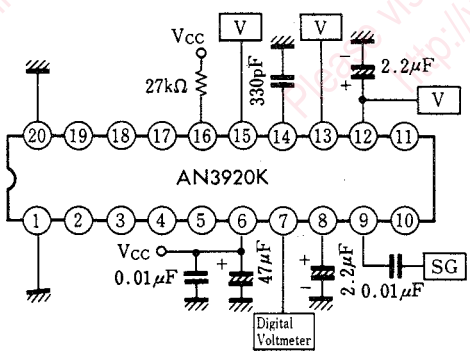
duty 50 : 50

$\Delta G_{R4} = G_{R4} - G_{R4}$
$\Delta G_{R2} = G_{R3} - G_{R3}$
$\Delta G_{R1} = G_{R1} - G_{R3}$

$\Delta G_4 = G_{R4} - G_{L4}$
$\Delta G_3 = G_{R3} - G_{L3}$
$\Delta G_2 = G_{R2} - G_{L2}$
$\Delta G_1 = G_{R1} - G_{L1}$

- The 6H High threshold level is an electric potential at which the Pin⑥ output rises approximately 4dB(1.5dB to 6.5dB) by increasing the Pin③ electric potential from 0V under the G_{R3} measuring conditions.

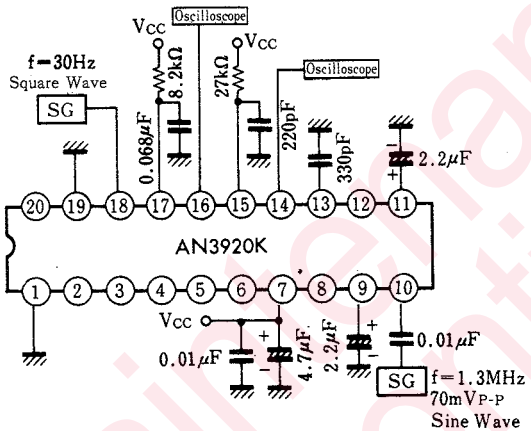
Test Circuit 3 (S_{10-14}, V_{14}, S_{10-12}, V_{12}, V_{11})



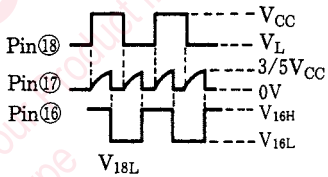
f=1.3MHz, $70mV_{P-P}$→Sine Wave at 0dB

- Drop out detection sensitivity (S_{10-14}): The input level at which Pin⑭ will be High by lowering the Pin⑩ input level below 70mV_{p-p}(0dB).
- S/H output High level (V_{14}): The above Pin⑭ voltage in the case where it is High.
- Linear switching sensitivity (S_{10-12}): The input level at which Pin⑫ will be High by lowering the Pin⑩ input level below 70mV_{p-p}(0dB).
- Linear output High level (V_{12}): The above Pin⑫ voltage in the case where it is High.
- Envelope output halt level (V_{11}): The Pin⑪ electric potential at which the Pin⑧ electric potential is 0.5V or less by increasing the Pin⑪ electric potential when the Pin⑩ input level is 70mV_{p-p}.

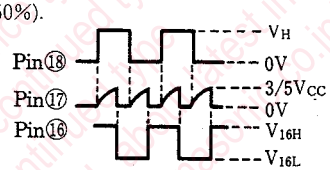
Test Circuit 4 (V_{18H}, V_{18L}, V_{16H}, V_{16L})



- HSW input voltage High level V_{18H}
  The V_H level at which waveforms as shown in the below figure are output to Pin⑯ and Pin⑰ when a square wave (f=30Hz, 0V) is input to Pin⑱ (duty is 50%).

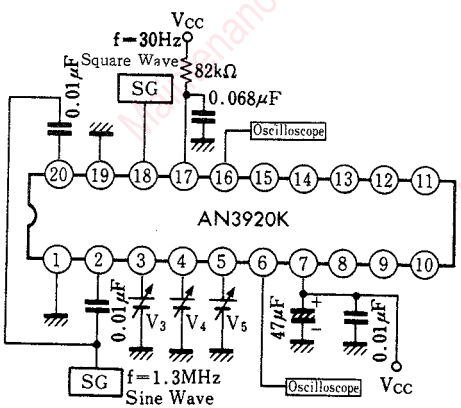


- HSW input voltage low level V_{18L}
  The V_L level at which waveforms as shown in the below figure are output to Pin⑯ and Pin⑰ when a square wave (f=30Hz, Vcc) is input to Pin⑱ (Duty=50%).



- A.H.SW output High level V_{16H}
  The Pin⑯ level in the above figure in the case where it is High
- A.H.SW output Low level V_{16L}
  The Pin⑯ level in the above figure in the case where it is Low

Test Circuit 5 (ΔG_{R3T}, ΔG_{R4T}, ΔG_{R2T}, Δ_{R1T})

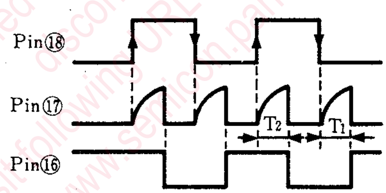


- V_5 is regulated so that the Amp.R3 gain will be 22dB.
  (The conditions in **Test Circuit 2** apply to this case except for the input level.)

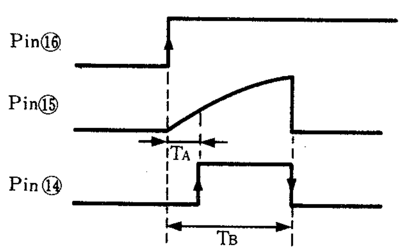
[Reference Material for Designing]
Waveforms of Pins

Pin No.	Function	Waveform (Condition)	Impedance	Pin No.	Function	Waveform (Condition)	Impedance
1	GND	————	———	11	Linear Det	————	———
2	RF_{IN} (R-ch)	55mV_{P-P} 1.3MHz+1.7MHz	15kΩ	12	Auto Linear OUT	High at typ. −10dB (V_{OUT}≧3.5V)	E.F.
3	6H High IN	The total gain is risen by 4dB at High. Vth≒3.5V	Base Input	13	D.O.det	————	———
4	+12dB High IN	The total gain is risen by 12dB at High. Vth≒2.5V	Base Input	14	S/H OUT	(V_{OUT}≒3.5V)	E.F.
5	VAR (Variable Amplifier Control)	The total gain is changed by more than ±6dB. (2V～3.5V)	Base Input	15	M.M.2 (7μsec)	3V	———
6	RF OUT	700mV_{P-P} 1.3MHz+1.7MHz	E.F.	16	A.H.SW OUT	V_{CC}−D 0V	———
7	V_{CC}	5.0V	———	17	M.M.1 (60°shift)	3V	———
8	Enve. OUT	When typ. is Input 2 2.8V	E.F.	18	H.SW IN	30Hz duty50:50	More than 39kΩ
9	Enve. Det	————	———	19	GND	————	———
10	RF IN	70mV_{P-P} 1.3MHz	10kΩ	20	RF IN (L-ch)	55mV_{P-P} 1.3MHz+1.7MHz	15kΩ

(1) M.M.1 Delay Time
If C=0.068μF and R=82kΩ, then T_1≒5.4ms (≒CR ln2.6). [R≧15kΩ]

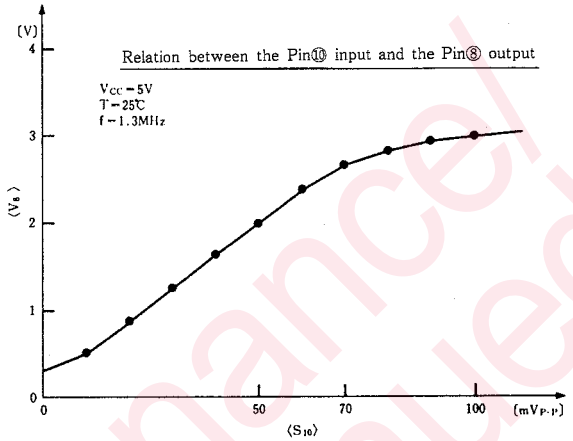


(2) M.M.2 Delay Time
If C=220pF and R=27kΩ, then T_A≒1.3μs (≒0.3μs+CR ln1.2). T_B≒6.8μs (≒1.2μs+CR ln2.6). [R≧15kΩ]



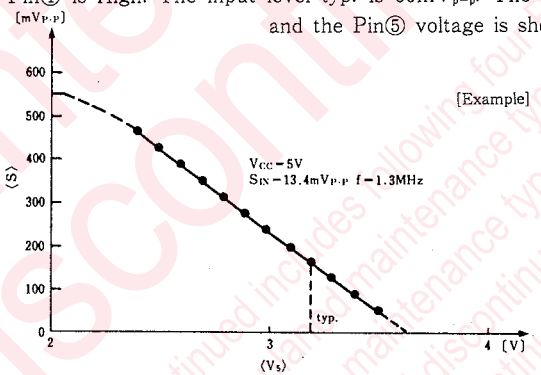
(3) The Pin⑥ load resistance must be that of 470Ω or over.

(4) The relation between the Pin⑩ input and the Pin⑧ output is shown below.



Note) The left values are reference values for designing in the case where Vcc is 5V and T is 25℃.

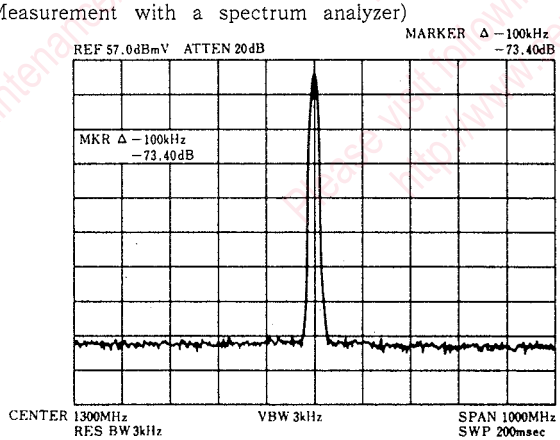
(5) Regulate the normal Pin⑤ voltage so that the gain between Pin② or Pin⑳ and Pin⑥ will be 22dB when Pin③ is Low and Pin④ is High. The input level typ. is 55mV$_{p-p}$. The relation between the Pin⑥ output and the Pin⑤ voltage is shown below.



[Example]

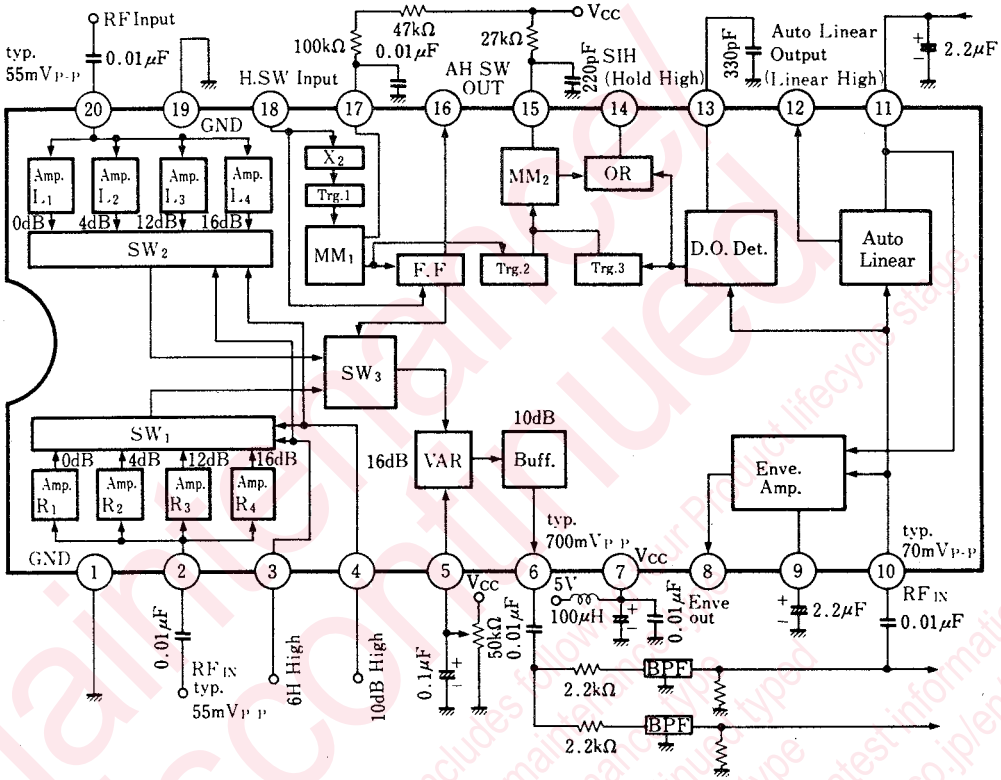
(6) Input Impedance in the case where Vcc is OFF Pin③→50kΩ Pin⑱→39kΩ
(Do not apply voltage to Pin⑪ when Vcc is OFF.)

(7) The signal level and the noise level of the Pin⑥ output are shown below.
(Measurement with a spectrum analyzer)



Note) The above values are reference ones for designing and not guaranteed ones.

■ Application Circuit



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