

AN5650

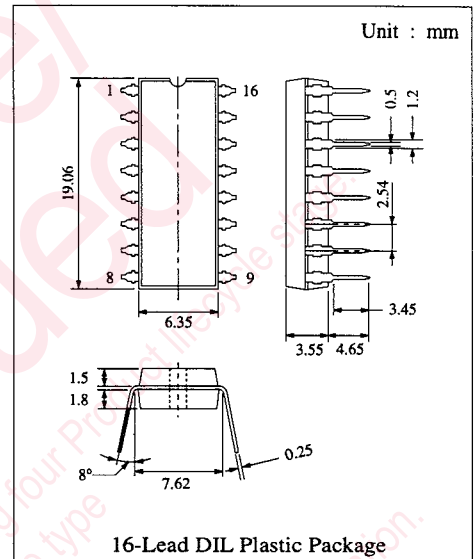
Colour TV Synchronization Signal Processing Circuit

■ Description

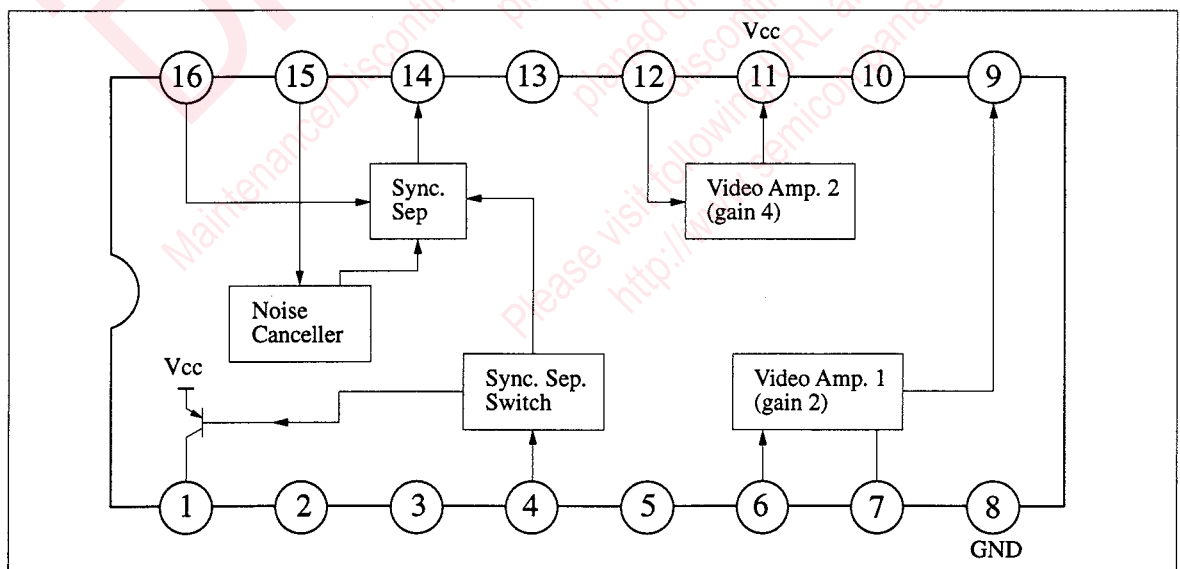
The AN5650 is an integrated circuit designed for colour TV synchronizing signal processing circuit.

■ Features

- Built-in video signal amplifier circuit
- A synchronizing separation circuit highly stable against noise
- Built-in synchronization signal output switching circuit



■ Block Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit		
Voltage	Supply Voltage	V ₁₃₋₈	14.4	V	
	Circuit Voltage	V ₁₋₈	0	V ₁₃₋₈	V
		V ₄₋₈	0	V ₁₃₋₈	V
		V ₆₋₈	0	V ₁₃₋₈	V
		V ₇₋₈	0	V ₁₃₋₈	V
		V ₁₂₋₈	0	V ₁₃₋₈	V
		V ₁₄₋₈	0	V ₁₃₋₈	V
		V ₁₅₋₈	0	6	V
V ₁₆₋₈	-3	2	V		
Current	Supply Current	I ₁₃	40	mA	
	Circuit Current	I ₁	-2	0	mA
		I ₇	-3	0	mA
		I ₉	-5	0	mA
		I ₁₁	-5	0	mA
		I ₁₄	0	10	mA
		I ₁₆	-1	1	mA
Power Dissipation	P _D	560	mW		
Operating Ambient Temperature	Topr	-20 ~ +70°C	°C		
Storage Temperature	Tstg	-55 ~ +150°C	°C		

■ Electrical Characteristics (Ta=25°C)

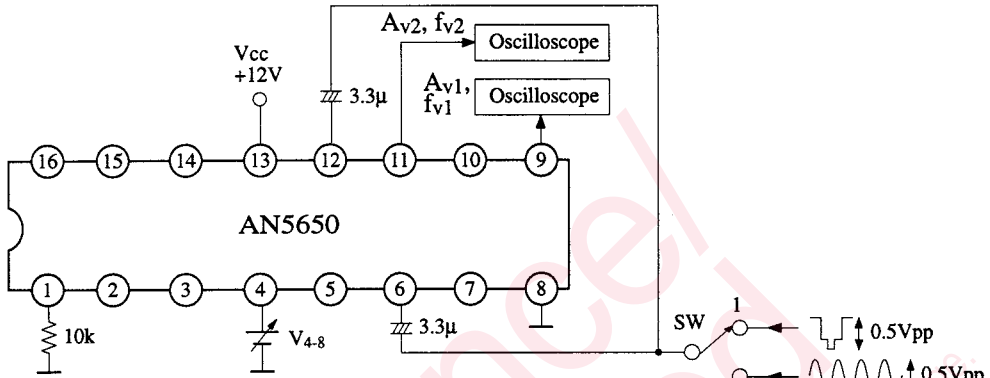
Item	Symbol	Test Cct	Condition	min.	typ.	max.	Unit
Voltage Gain (Video Amp. 1)	A _{v1}	1	Video signal input 0.5Vpp SW1	1.5	1.9	2.3	times
Voltage Gain (Video Amp. 2)	A _{v2}	1	Video signal input 0.5Vpp SW2	3.4	3.9	4.3	times
Frequency Characteristics (Video Amp. 1)	f _{v1}	1	Sine wave input 0.5Vpp SW2 input frequency when A _{v1} becomes -3dB	5			MHz
Frequency Characteristics (Video Amp. 2)	f _{v2}	1	Sine wave input 0.5Vpp SW2 input frequency when A _{v2} becomes -3dB	5			MHz
Switch Operating Voltage	V ₄₋₈	1	Switch input voltage when switch output becomes 0.7V or more	1.5			V
Max. Allowable Input (Video Amp. 1)	V _{in(max).1}	1	APL = 50%			1.9	Vpp
Max. Allowable Input (Video Amp. 2)	V _{in(max).2}	1	APL = 50%			1.4	Vpp
Sync. Sep. Input*	V _{in3}	2	V _{cc} = 12V, APL = 50%	1.0		2.5	Vpp

* Design reference value

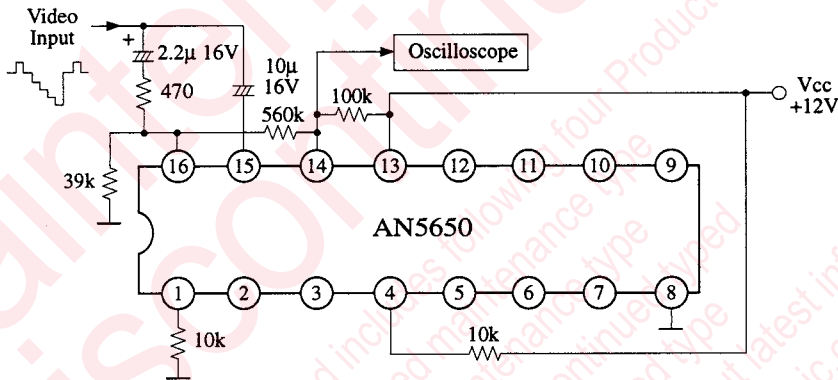
■ Pin Description

Pin No	Pin Name	Pin No	Pin Name
1	Switch Output	9	Video Signal Output 1
2	NC	10	NC
3	NC	11	Video Signal Output 2
4	Sync. Sep. Switch Input	12	Video Signal Input 2
5	NC	13	V _{cc}
6	Video Signal Input 1	14	Sync. Sep. Output
7	Gain Control	15	Noise Det. Input
8	GND	16	Video Signal Input 3

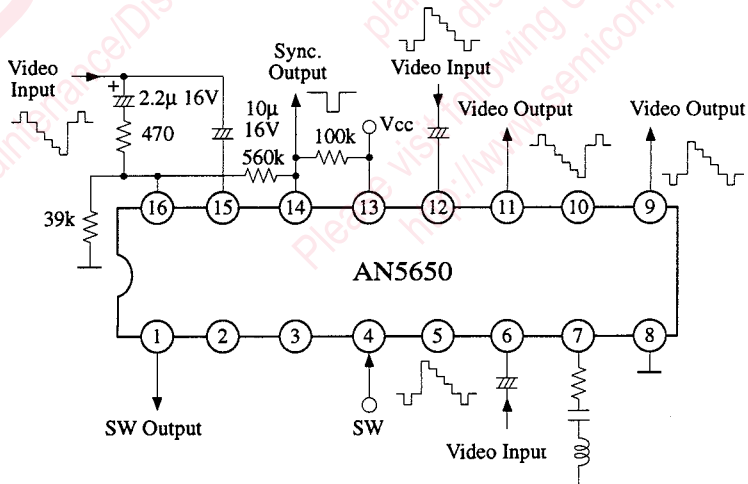
Test Circuit 1 (A_{v1} , A_{v2} , f_{v1} , f_{v2} , V_{4-8} , $V_{in(max.)1}$, $V_{in(max.)2}$)



Test Circuit 2 (V_{in3})



■ Application Circuit



(When input is high, Sync. Sep. and SW Output Operates.)

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