AN5733

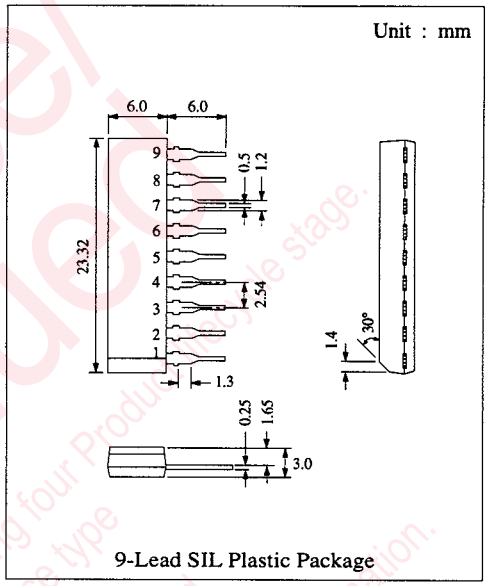
TV Volume Control Circuit

■ Description

The AN5733 is an integrated circuit designed for TV volume control circuit.

■ Features

- Dual attenuator
- 9-lead SIL plastic package

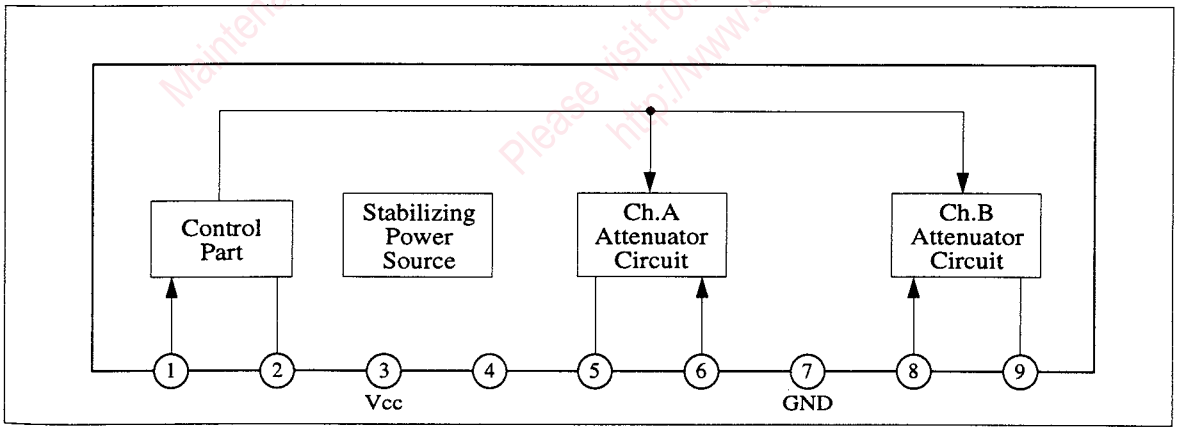


9-Lead SIL Plastic Package

■ Pin Descriptions

Pin No.	Pin Name
1	Control Voltage Input
2	Control Reference Voltage Output
3	Power Source (Vcc)
4	Decoupling
5	Ch.A Output Signal
6	Ch.A Input Signal
7	GND
8	Ch.B Input Signal
9	Ch.B Output Signal

■ Block Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	14.4	V
Supply Current	I_3	13.7	mA
Power Dissipation (Ta = 70°C)	P_D	197	mW
Operating Ambient Temperature	Topr	-40 ~ +150	°C
Storage Temperature	Tstg	-20 ~ +70	°C

■ Electrical Characteristics (Ta=25°C)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Supply Voltage	I_3		Table 1 (V_{CC}=12V)	9.5	11.3	13.5	mA
Terminal Voltage	$V_{2\text{-}7}$		Table 1 (V_{CC}=12V)	3.8	4.1	4.45	V
Terminal Voltage	$V_{4\text{-}7}$		Table 1 (V_{CC}=12V)	2.9	3.2	3.5	V
Terminal Voltage	$V_{6\text{-}7,\ 8\text{-}7}$		Table 1 (V_{CC}=12V)	2.0	2.4	2.8	V
Terminal Voltage	$V_{5\text{-}7,\ 9\text{-}7}$		Table 1 (V_{CC}=12V)	2.9	3.4	3.9	V
Circuit Gain (1) (VR=10kΩ)	$G_{V⑤\text{-}1}$	1	f=1kHz, V_L=500mVrms	4	6	7.6	dB
Circuit Gain (1) Ch. Relative Gain	$\Delta G_{\text{-}1}$	1	f=1kHz, V_L=500mVrms	-1.5		1.5	dB
Circuit Gain (1) O/P Dist. Factor	THD	1	f=1kHz, V_L=500mVrms		0.2		%
Circuit Gain (2) (VR=5kΩ)	$G_{V⑤\text{-}2}$	1	f=1kHz, V_L=500mVrms	-2	0	2.2	dB
Circuit Gain (2) Ch. Relative Gain	$\Delta G_{\text{-}2}$	1	f=1kHz, V_L=500mVrms	-2		2	dB
Circuit Gain (2) O/P Dist. Factor	THD	1	f=1kHz, V_L=500mVrms		0.2		%
Circuit Gain (3) (VR=1kΩ)	$G_{V⑤\text{-}3}$	1	f=1kHz, V_L=500mVrms	-20	-16	-12	dB
Circuit Gain (3) Ch. Relative Gain	$\Delta G_{\text{-}3}$	1	f=1kHz, V_L=500mVrms	-2.5		2.5	dB
Maximum Attenuation (VR=0)	Att	1	f=1kHz, V_L=500mVrms	75			dB
Channel Separation	Sep	2	f=1kHz, V_L=500mVrms	70			dB
Input Impedance	R_{in}	3	f=1kHz		25		kΩ
Output Impedance	R_{out}	4	f=1kHz		1.7		kΩ
Hum Rejection	Hr		Table 1	34			dB
Noise Output Voltage	N_O	1				180	μVrms
DC Output Voltage Fluctuation	$\Delta V_{5\text{-}7,\ 9\text{-}7}$		Table 1 (V_{CC}=12V)	-0.2		0.3	V

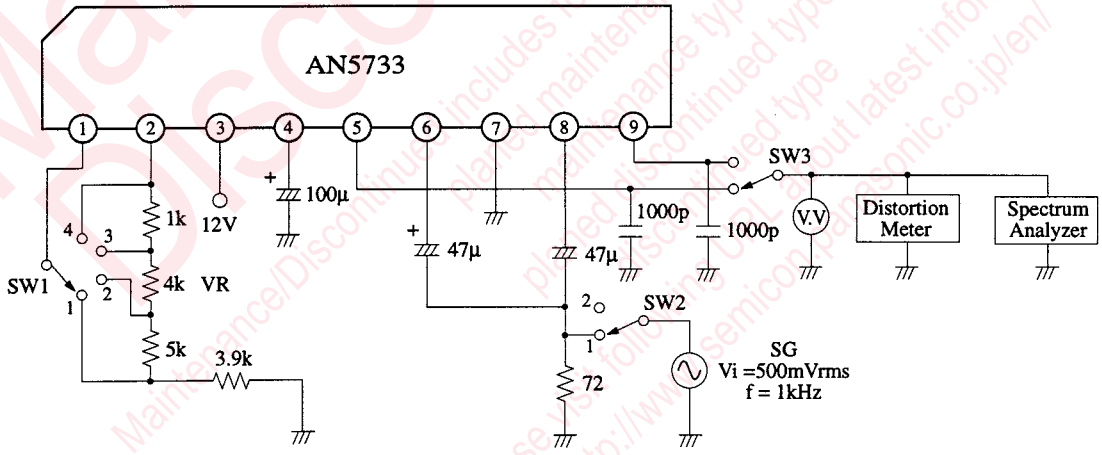
Table 1

Item	Symbol	Measuring Pin No.	Pin No. 1	2	3	4	5	6	7	8	9	Note
Supply Voltage	I_3	3	8.9kΩ 0V	5kΩ CON①	12V				0V			
Terminal Voltage	$V_{2\text{-}7}$	2	8.9kΩ 0V	5kΩ CON①	12V				0V			
Terminal Voltage	$V_{4\text{-}7}$	4	8.9kΩ 0V	5kΩ CON①	12V				0V			
Terminal Voltage	$V_{6\text{-}7}$	6	8.9kΩ 0V	5kΩ CON①	12V				0V			
Terminal Voltage	$V_{8\text{-}7}$	8	8.9kΩ 0V	5kΩ CON①	12V				0V			
Terminal Voltage	$V_{5\text{-}7}$	5	8.9kΩ 0V	5kΩ CON①	12V				0V			
Terminal Voltage	$V_{9\text{-}7}$	9	8.9kΩ 0V	5kΩ CON①	12V				0V			
Hum Rejection	Hr_5	5	8.9kΩ 0V	5kΩ CON①	14V				0V			1
Hum Rejection	ΔHr_5	5	8.9kΩ 0V	5kΩ CON①	10V				0V			1
Hum Rejection	Hr_g	9	8.9kΩ 0V	5kΩ CON①	14V				0V			2
Hum Rejection	ΔHr_g	9	8.9kΩ 0V	5kΩ CON①	10V				0V			2
DC Output Voltage	$V_{5\text{-}7,\ 9\text{-}7}$	5, 9	3.9kΩ 0V	10kΩ CON①	12V				0V			3,4
DC Output Voltage Fluctuation	$\Delta V_{5\text{-}7,\ 9\text{-}7}$	5, 9	CON②	13.9kΩ 0V	12V				0V			3,4

Obtain Hr of Pin No.5 by taking ratio of difference between changes of DC voltage of pin No. 5, i.e. Hr_5 and ΔHr_5 against change in supply voltage (4V). Similarly, obtain Hr of Pin No.9.

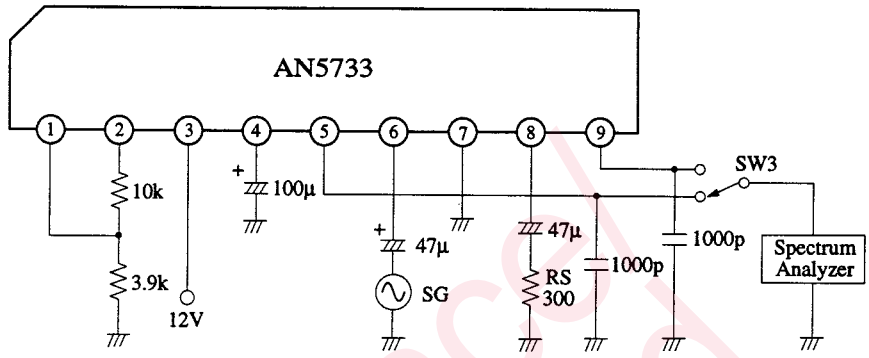
Note) 1. (18-2) - (18-1) : H_5 3. (20 upper) - (5 upper) : $V_{5\text{-}7}$
2. (18-4) - (18-3) : H_9 4. (20 below) - (5 below) : $V_{9\text{-}7}$

Test Circuit 1



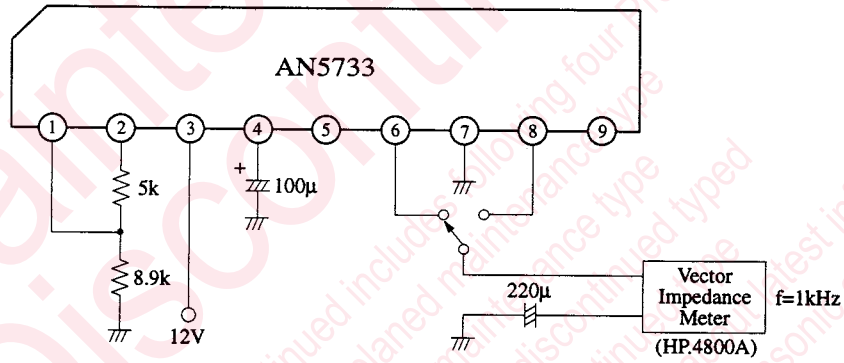
Item	Symbol	SW1	SW2
Circuit Gain (1) Ch. Relative Gain	$\Delta G_{\text{-}1}$	1	1
Circuit Gain (1) O/P Dist. Factor	THD	1	1
Circuit Gain (2) (VR=5kΩ)	$Gv_{⑤\text{-}2}$	1	1
Circuit Gain (2) Ch. Relative Gain	$\Delta G_{\text{-}2}$	2	1
Circuit Gain (2) O/P Dist. Factor	THD	2	1
Circuit Gain (3) (VR=1kΩ)	$Gv_{⑤\text{-}3}$	2	1
Circuit Gain (3) Ch. Relative Gain	$\Delta G_{\text{-}3}$	3	1
Maximum Attenuation (VR=0)	Att	3	1
Channel Separation	Sep	4	1
Input Impedance	R_{in}	2	2

Test Circuit 2

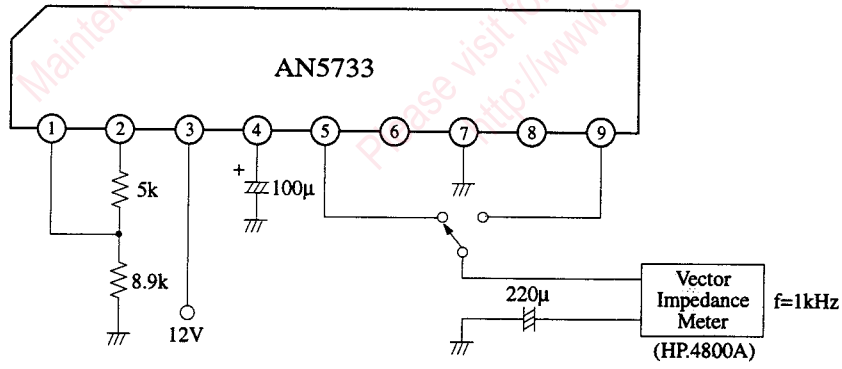


Note) Read level difference between Pin No.5 and Pin No.9 on the Spectrum Analyzer.
Read level difference of Pin No.5 and Pin No.9, similarly after changing SG and RS.

Test Circuit 3



Test Circuit 4



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