

High-Power PNP Silicon Transistors

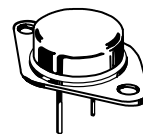
... designed for use in industrial–military power amplifier and switching circuit applications.

- High Collector–Emitter Sustaining Voltage —
 $V_{CEO(sus)} = 100 \text{ Vdc (Min)} \text{ — } 2N6437$
 $= 120 \text{ Vdc (Min)} \text{ — } 2N6438$
- High DC Current Gain —
 $h_{FE} = 20\text{--}80 @ I_C = 10 \text{ Adc}$
 $= 12 \text{ (Min)} @ I_C = 25 \text{ Adc}$
- Low Collector–Emitter Saturation Voltage —
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max)} @ I_C = 10 \text{ Adc}$
- Fast Switching Times @ $I_C = 10 \text{ Adc}$
 $t_r = 0.3 \mu\text{s (Max)}$
 $t_s = 1.0 \mu\text{s (Max)}$
 $t_f = 0.25 \mu\text{s (Max)}$
- Complement to NPN 2N6339 thru 2N6341

2N6437 2N6438*

*ON Semiconductor Preferred Device

**25 AMPERE
POWER TRANSISTORS
PNP SILICON
100, 120 VOLTS
200 WATTS**



**CASE 1-07
TO-204AA
(TO-3)**

MAXIMUM RATINGS (1)

Rating	Symbol	2N6437	2N6438	Unit
Collector–Base Voltage	V_{CB}	120	140	Vdc
Collector–Emitter Voltage	V_{CEO}	100	120	Vdc
Emitter–Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous Peak	I_C	25 50		Adc
Base Current	I_B	10		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	200 1.14		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	$^\circ\text{C/W}$

(1) Indicates JEDEC Registered Data.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

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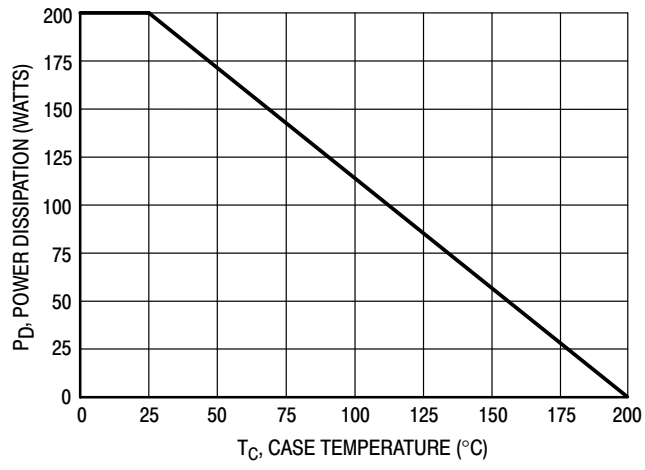


Figure 1. Power Derating

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*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) ($I_C = 50\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	100 120	— —	Vdc
Collector Cutoff Current ($V_{CE} = 50\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 60\text{ Vdc}$, $I_B = 0$)	I_{CEO}	— —	50 50	μA
Collector Cutoff Current ($V_{CE} = 110\text{ Vdc}$, $V_{BE(off)} = -1.5\text{ Vdc}$) ($V_{CE} = 130\text{ Vdc}$, $V_{BE(off)} = -1.5\text{ Vdc}$) ($V_{CE} = 100\text{ Vdc}$, $V_{BE(off)} = -1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 120\text{ Vdc}$, $V_{BE(off)} = -1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	— — — —	10 10 1.0 1.0	μA mA
Collector Cutoff Current ($V_{CB} = 120\text{ Vdc}$, $I_E = 0$) ($V_{CB} = 140\text{ Vdc}$, $I_E = 0$)	I_{CBO}	— —	10 10	μA
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	100	μA

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 0.5\text{ A}$, $V_{CE} = 2.0\text{ Vdc}$) ($I_C = 10\text{ A}$, $V_{CE} = 2.0\text{ Vdc}$) ($I_C = 25\text{ A}$, $V_{CE} = 2.0\text{ Vdc}$)	h_{FE}	30 20 12	— 120 —	—
Collector–Emitter Saturation Voltage (1) ($I_C = 10\text{ A}$, $I_B = 1.0\text{ A}$) ($I_C = 25\text{ A}$, $I_B = 2.5\text{ A}$)	$V_{CE(sat)}$	— —	1.0 1.8	Vdc
Base–Emitter Saturation Voltage (1) ($I_C = 10\text{ A}$, $I_B = 1.0\text{ A}$) ($I_C = 25\text{ A}$, $I_B = 2.5\text{ A}$)	$V_{BE(sat)}$	— —	1.8 2.5	Vdc

DYNAMIC CHARACTERISTICS

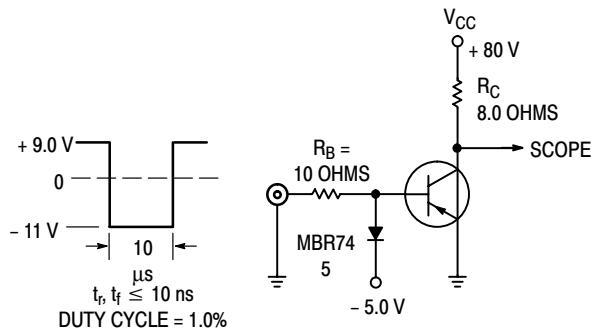
Current–Gain — Bandwidth Product ($I_C = 1.0\text{ A}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 10\text{ MHz}$)	f_T	40	—	MHz
Output Capacitance ($V_{CE} = 10\text{ Vdc}$, $I_E = 0$, $f = 100\text{ kHz}$)	C_{ob}	—	700	pF

SWITCHING CHARACTERISTICS

Rise Time ($V_{CC} = 80\text{ Vdc}$, $I_C = 10\text{ A}$, $V_{BE(off)} = 6.0\text{ Vdc}$, $I_{B1} = 1.0\text{ A}$)	t_r	—	0.3	μs
Storage ($V_{CC} = 80\text{ Vdc}$, $I_C = 10\text{ A}$, $V_{BE(off)} = 6.0\text{ Vdc}$, $I_{B1} = I_{B2} = 1.0\text{ A}$)	t_s	—	1.0	μs
Fall Time ($V_{CC} = 80\text{ Vdc}$, $I_C = 10\text{ A}$, $V_{BE(off)} = 6.0\text{ Vdc}$, $I_{B1} = I_{B2} = 1.0\text{ A}$)	t_f	—	0.25	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$; Duty Cycle $\leq 2.0\%$.



NOTE: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

Figure 2. Switching Time Test Circuit

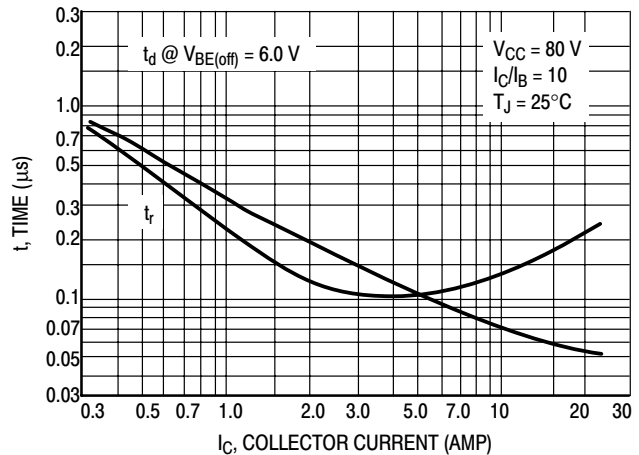


Figure 3. Turn–On Time

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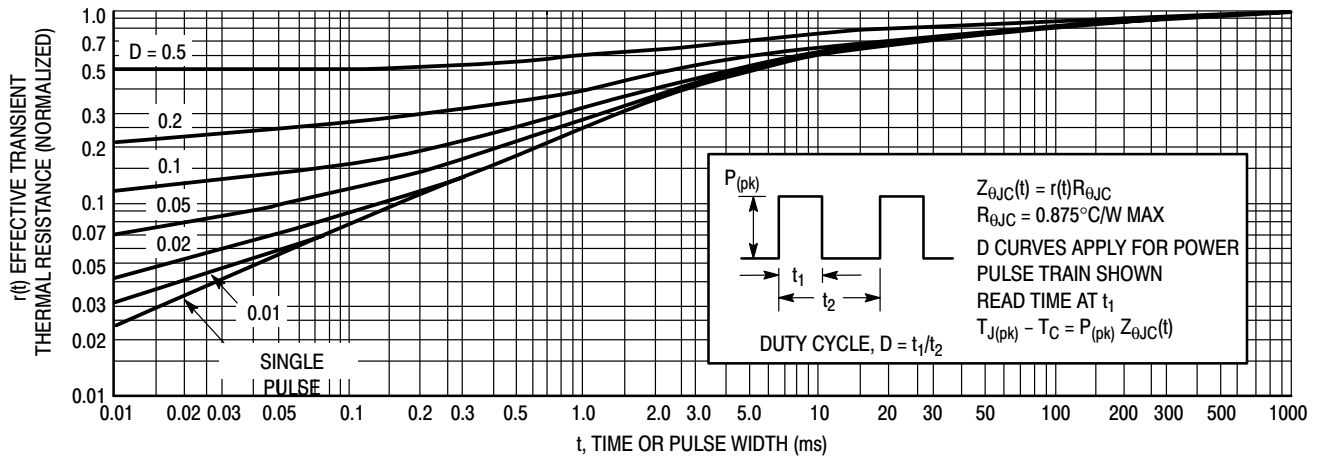


Figure 4. Thermal Response

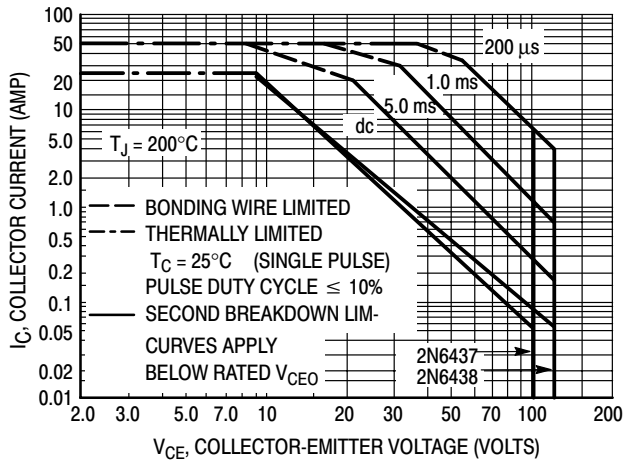


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

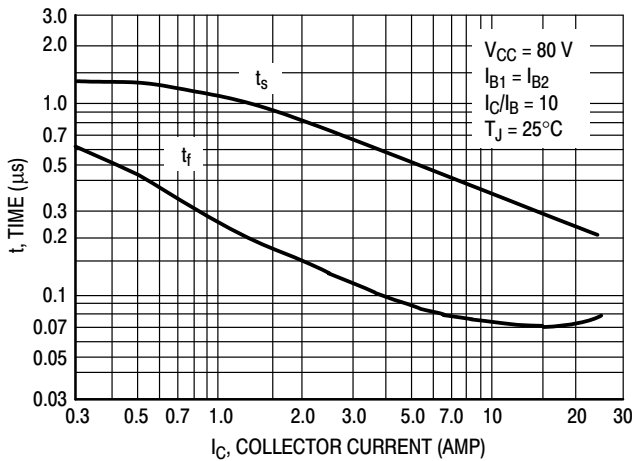


Figure 6. Turn-Off Time

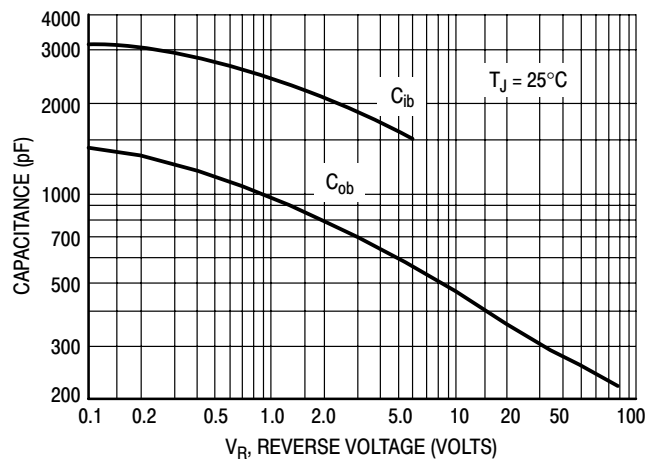


Figure 7. Capacitance

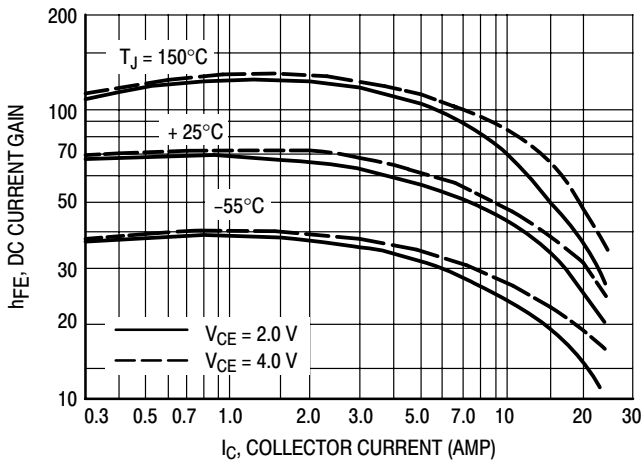


Figure 8. DC Current Gain

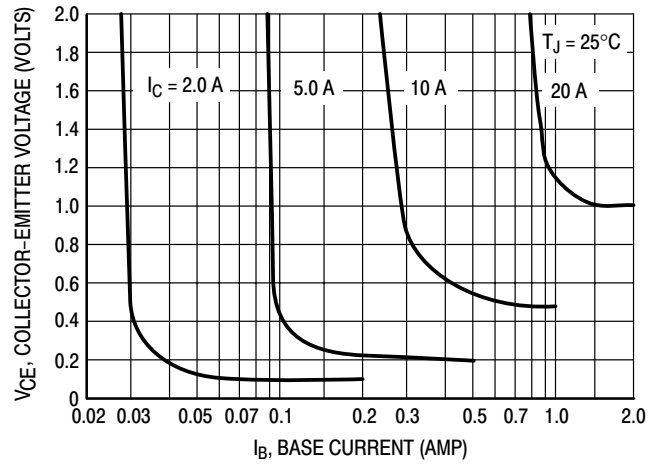


Figure 9. Collector Saturation Region

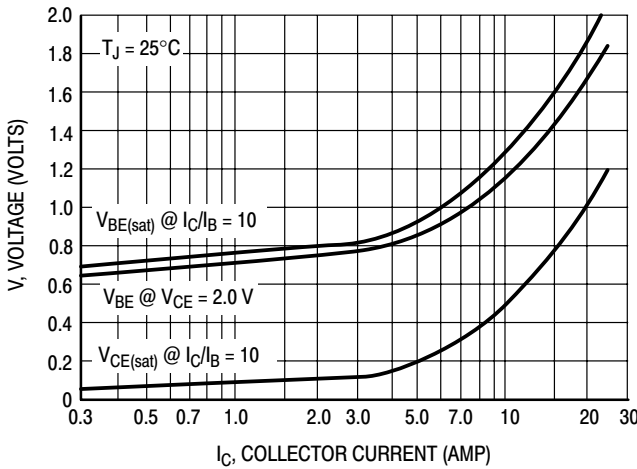


Figure 10. "On" Voltages

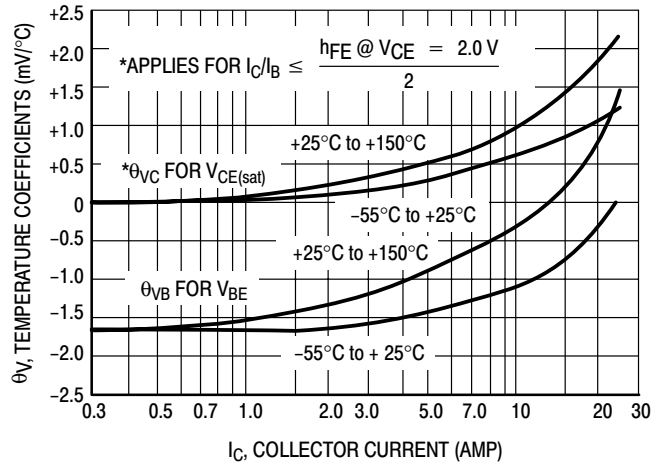


Figure 11. Temperature Coefficients

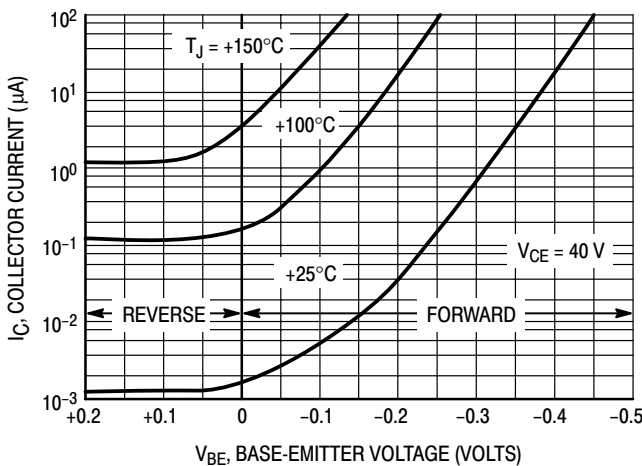


Figure 12. Collector Cut-Off Region

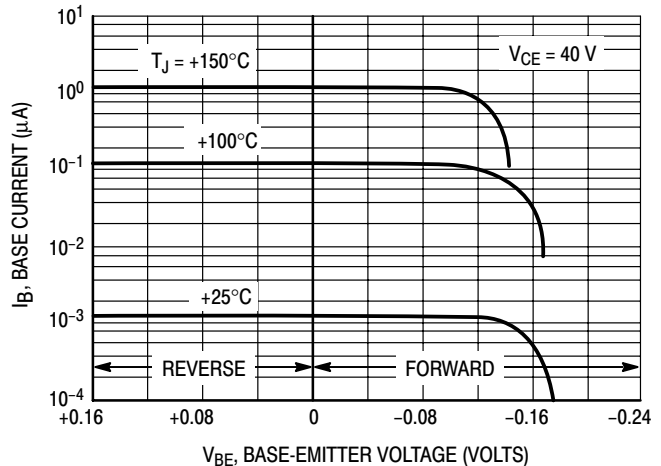
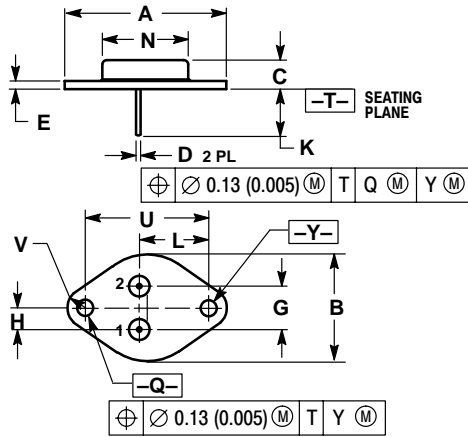


Figure 13. Base Cutoff Region

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PACKAGE DIMENSIONS

CASE 1-07 TO-204AA (TO-3) ISSUE Z



NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:

1. PIN 1. BASE
 2. EMITTER
- CASE: COLLECTOR

Notes

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