

# Plastic Darlington Complementary Silicon Power Transistors

... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —  
 $h_{FE} = 2000$  (Typ) @  $I_C = 2.0$  Adc
- Collector-Emitter Sustaining Voltage — @ 100 mA dc  
 $V_{CEO(sus)} = 60$  Vdc (Min) — 2N6035, 2N6038 = 80 Vdc (Min) — 2N6036, 2N6039
- Forward Biased Second Breakdown Current Capability  
 $I_{S/b} = 1.5$  Adc @ 25 Vdc
- Monolithic Construction with Built-In Base-Emitter Resistors to Limit Leakage Multiplication
- Space-Saving High Performance-to-Cost Ratio TO-225AA Plastic Package

## MAXIMUM RATINGS (1)

Rating	Symbol	2N6035 2N6038	2N6036 2N6039	Unit
Collector-Emitter Voltage	$V_{CEO}$	60	80	Vdc
Collector-Base Voltage	$V_{CB}$	60	80	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current — Continuous Peak	$I_C$	4.0 8.0		Adc
Base Current	$I_B$	100		mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 0.32		Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.5 0.012		Watts
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150		$^\circ\text{C}$

## THERMAL CHARACTERISTICS

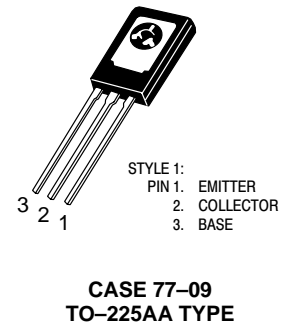
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	3.12	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	83.3	$^\circ\text{C/W}$

(1) Indicates JEDEC Registered Data.

**PNP  
2N6035**  
**2N6036\***  
**NPN  
2N6038**  
**2N6039\***

\*ON Semiconductor Preferred Device

**DARLINGTON  
4-AMPERE  
COMPLEMENTARY  
SILICON  
POWER TRANSISTORS  
60, 80 VOLTS  
40 WATTS**



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

2N6035 2N6036 2N6038 2N6039

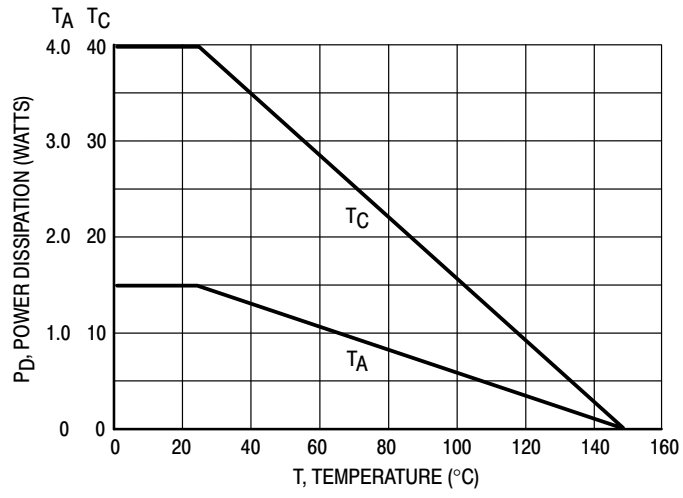


Figure 1. Power Derating

# 2N6035 2N6036 2N6038 2N6039

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Sustaining Voltage (I <sub>C</sub> = 100 mAdc, I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	60 80	— —	Vdc
Collector-Cutoff Current (V <sub>CE</sub> = 60 Vdc, I <sub>B</sub> = 0) (V <sub>CE</sub> = 80 Vdc, I <sub>B</sub> = 0)	I <sub>CEO</sub>	— —	100 100	μA
Collector-Cutoff Current (V <sub>CE</sub> = 60 Vdc, V <sub>BE(off)</sub> = 1.5 Vdc) (V <sub>CE</sub> = 80 Vdc, V <sub>BE(off)</sub> = 1.5 Vdc) (V <sub>CE</sub> = 60 Vdc, V <sub>BE(off)</sub> = 1.5 Vdc, T <sub>C</sub> = 125°C) (V <sub>CE</sub> = 80 Vdc, V <sub>BE(off)</sub> = 1.5 Vdc, T <sub>C</sub> = 125°C)	I <sub>CEX</sub>	— — — —	100 100 500 500	μA
Collector-Cutoff Current (V <sub>CB</sub> = 60 Vdc, I <sub>E</sub> = 0) (V <sub>CB</sub> = 80 Vdc, I <sub>E</sub> = 0)	I <sub>CBO</sub>	— —	0.5 0.5	mAdc
Emitter-Cutoff Current (V <sub>BE</sub> = 5.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	—	2.0	mAdc

## ON CHARACTERISTICS

DC Current Gain (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 3.0 Vdc) (I <sub>C</sub> = 2.0 Adc, V <sub>CE</sub> = 3.0 Vdc) (I <sub>C</sub> = 4.0 Adc, V <sub>CE</sub> = 3.0 Vdc)	h <sub>FE</sub>	500 750 100	— 15,000 —	—
Collector-Emitter Saturation Voltage (I <sub>C</sub> = 2.0 Adc, I <sub>B</sub> = 8.0 mAdc) (I <sub>C</sub> = 4.0 Adc, I <sub>B</sub> = 40 mAdc)	V <sub>CE(sat)</sub>	— —	2.0 3.0	Vdc
Base-Emitter Saturation Voltage (I <sub>C</sub> = 4.0 Adc, I <sub>B</sub> = 40 mAdc)	V <sub>BE(sat)</sub>	—	4.0	Vdc
Base-Emitter On Voltage (I <sub>C</sub> = 2.0 Adc, V <sub>CE</sub> = 3.0 Vdc)	V <sub>BE(on)</sub>	—	2.8	Vdc

## DYNAMIC CHARACTERISTICS

Small-Signal Current-Gain (I <sub>C</sub> = 0.75 Adc, V <sub>CE</sub> = 10 Vdc, f = 1.0 MHz)	h <sub>fe</sub>	25	—	—
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 0.1 MHz)	C <sub>ob</sub>	— —	200 100	pF

\*Indicates JEDEC Registered Data.

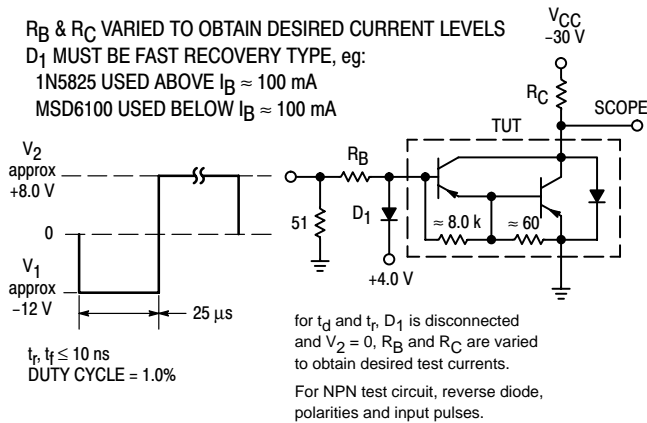


Figure 2. Switching Times Test Circuit

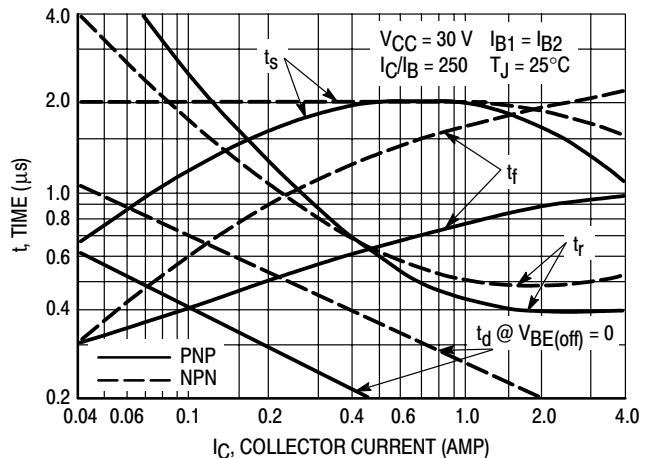


Figure 3. Switching Times

2N6035 2N6036 2N6038 2N6039

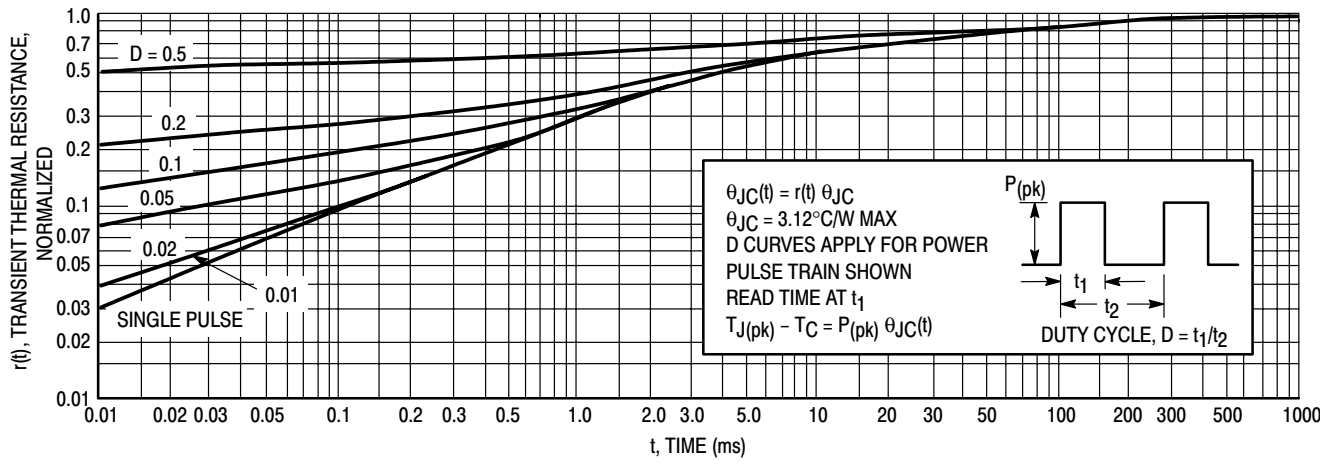


Figure 4. Thermal Response

ACTIVE-REGION SAFE-OPERATING AREA

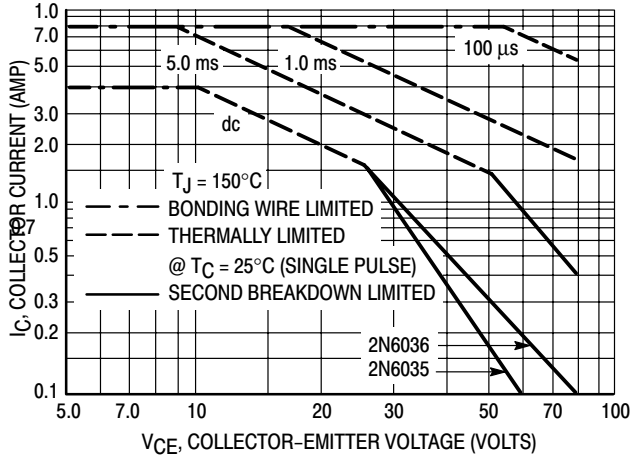


Figure 5. 2N6035, 2N6036

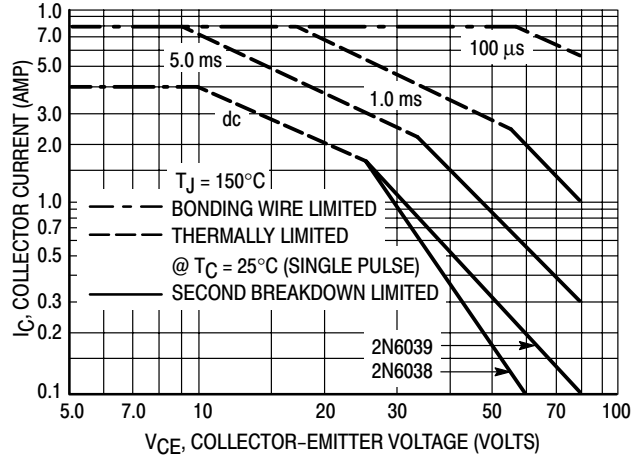


Figure 6. 2N6038, 2N6039

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

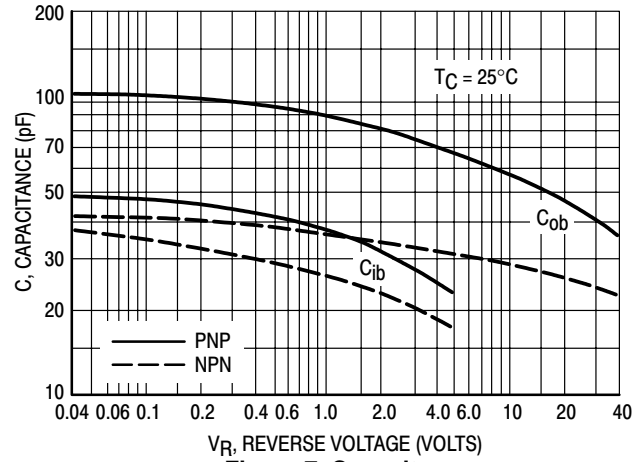


Figure 7. Capacitance

2N6035 2N6036 2N6038 2N6039

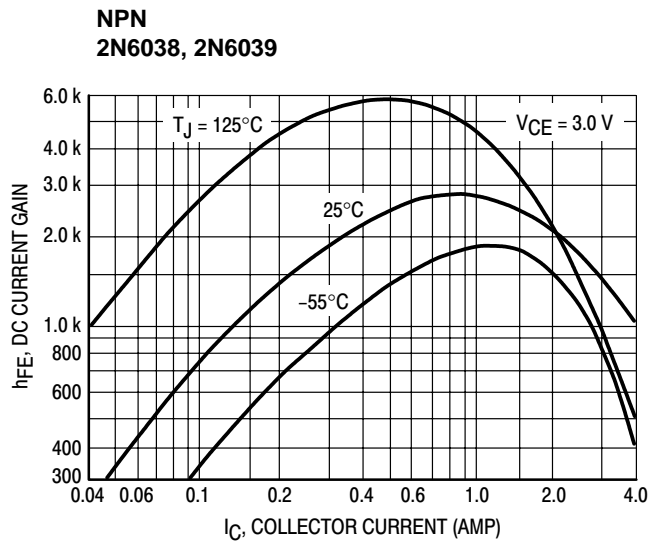
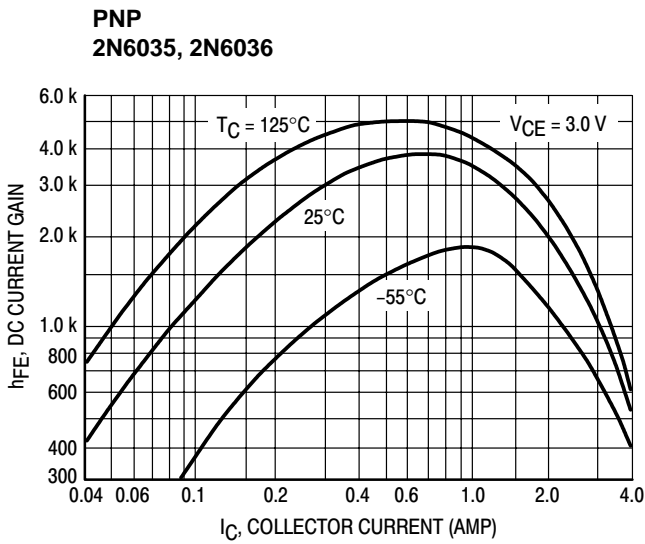


Figure 8. DC Current Gain

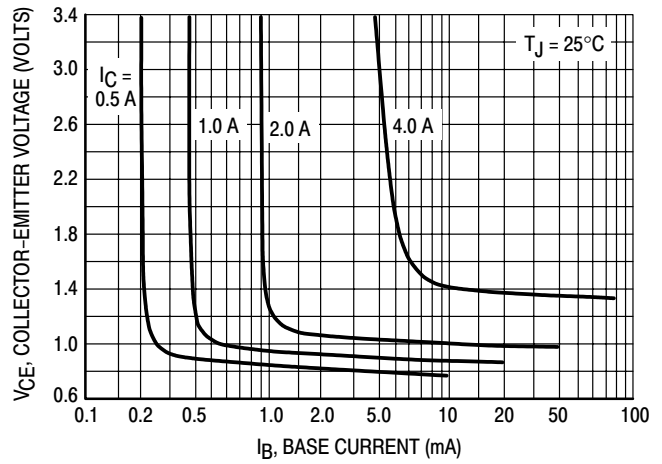
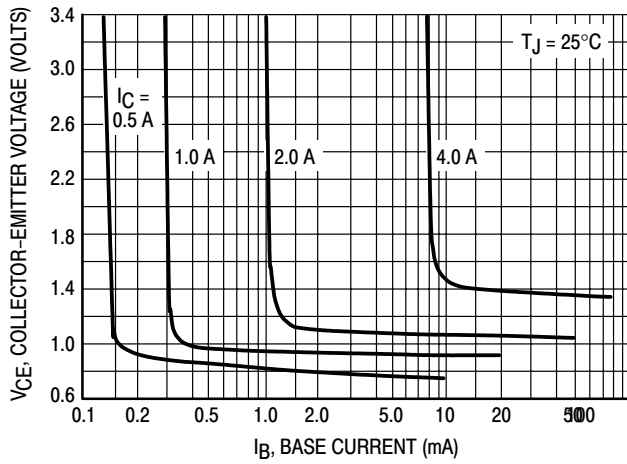


Figure 9. Collector Saturation Region

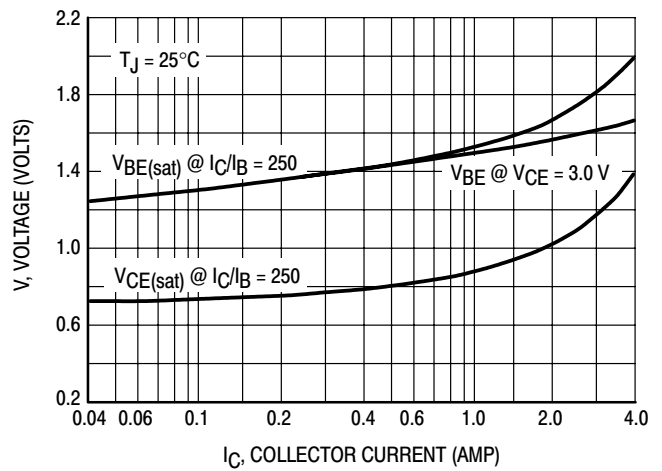
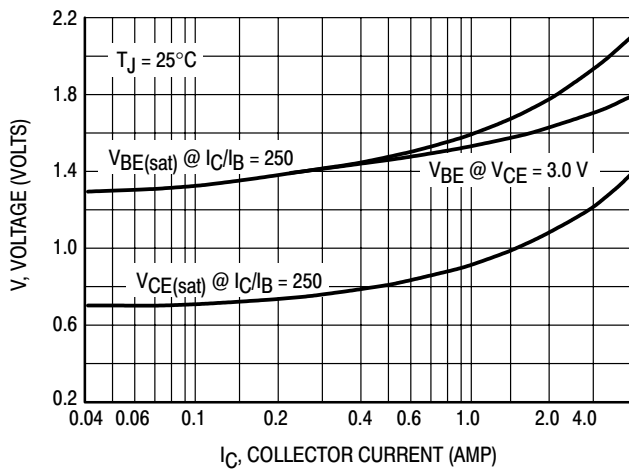
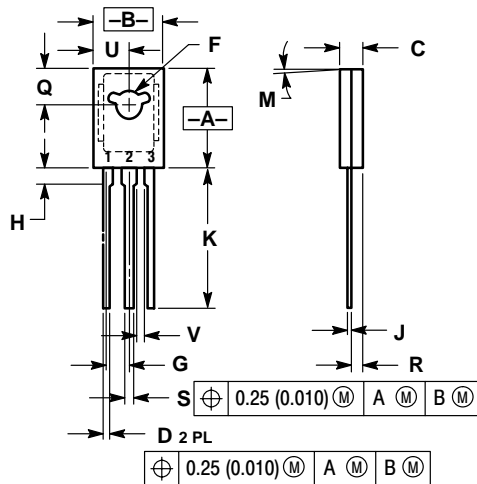


Figure 10. "On" Voltages

2N6035 2N6036 2N6038 2N6039

PACKAGE DIMENSIONS


TO-225AA  
CASE 77-09  
ISSUE W



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	---	1.02	---

- STYLE 1:  
PIN 1. EMITTER  
2. COLLECTOR  
3. BASE

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