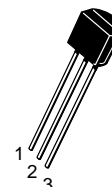
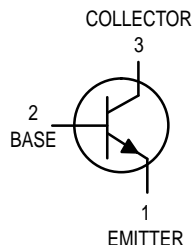


# General Purpose Transistor

## NPN Silicon

**2N4264**



CASE 29-04, STYLE 1  
TO-92 (TO-226AA)

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	15	Vdc
Collector–Base Voltage	$V_{CBO}$	30	Vdc
Emitter–Base Voltage	$V_{EBO}$	6.0	Vdc
Collector Current — Continuous	$I_C$	200	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	350 2.8	mW mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.0 8.0	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	357	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	$^\circ\text{C}/\text{W}$

### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Breakdown Voltage ( $I_C = 1.0$ mAdc, $I_B = 0$ )	$V_{(BR)CEO}$	15	—	Vdc
Collector–Base Breakdown Voltage ( $I_C = 10$ $\mu$ Adc, $I_E = 0$ )	$V_{(BR)CBO}$	30	—	Vdc
Emitter–Base Breakdown Voltage ( $I_E = 10$ $\mu$ Adc, $I_C = 0$ )	$V_{(BR)EBO}$	6.0	—	Vdc
Base Cutoff Current ( $V_{CE} = 12$ Vdc, $V_{EB(off)} = 0.25$ Vdc) ( $V_{CE} = 12$ Vdc, $V_{EB(off)} = 0.25$ Vdc, $T_A = 100^\circ\text{C}$ )	$I_{BEV}$	— —	0.1 10	$\mu$ Adc
Collector Cutoff Current ( $V_{CE} = 12$ Vdc, $V_{EB(off)} = 0.25$ Vdc)	$I_{CEX}$	—	100	nAdc

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Max	Unit
<b>ON CHARACTERISTICS</b>				
DC Current Gain ( $I_C = 1.0\text{ mAdc}$ , $V_{CE} = 1.0\text{ Vdc}$ ) ( $I_C = 10\text{ mAdc}$ , $V_{CE} = 1.0\text{ Vdc}$ ) ( $I_C = 10\text{ mAdc}$ , $V_{CE} = 1.0\text{ Vdc}$ , $T_A = -55^\circ\text{C}$ ) ( $I_C = 30\text{ mAdc}$ , $V_{CE} = 1.0\text{ Vdc}$ ) ( $I_C = 100\text{ mAdc}$ , $V_{CE} = 1.0\text{ Vdc}$ )(1) ( $I_C = 200\text{ mAdc}$ , $V_{CE} = 1.0\text{ Vdc}$ )(1)	$h_{FE}$	25 40 20 40 30 20	— 160 — — — —	—
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ mAdc}$ , $I_B = 1.0\text{ mAdc}$ ) ( $I_C = 100\text{ mAdc}$ , $I_B = 10\text{ mAdc}$ )(1)	$V_{CE(sat)}$	— —	0.22 0.35	Vdc
Base–Emitter Saturation Voltage ( $I_C = 10\text{ mAdc}$ , $I_B = 1.0\text{ mAdc}$ ) ( $I_C = 100\text{ mAdc}$ , $I_B = 10\text{ mAdc}$ )(1)	$V_{BE(sat)}$	0.65 0.75	0.8 0.95	Vdc

**SMALL–SIGNAL CHARACTERISTICS**

Current–Gain — Bandwidth Product ( $I_C = 10\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 100\text{ MHz}$ )	$f_T$	300	—	MHz
Input Capacitance ( $V_{EB} = 0.5\text{ Vdc}$ , $I_C = 0$ , $f = 1.0\text{ MHz}$ )	$C_{ibo}$	—	8.0	pF
Output Capacitance ( $V_{CB} = 5.0\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ , $I_E = 0$ )	$C_{obo}$	—	4.0	pF

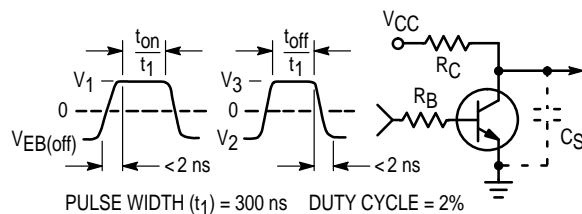
**SWITCHING CHARACTERISTICS**

Delay Time	$(V_{CC} = 10\text{ Vdc}$ , $V_{EB(off)} = 2.0\text{ Vdc}$ , $I_C = 100\text{ mAdc}$ , $I_{B1} = 10\text{ mAdc}$ ) (Fig. 1, Test Condition C)	$t_d$	—	8.0	ns
Rise Time		$t_r$	—	15	ns
Storage Time	$V_{CC} = 10\text{ Vdc}$ , ( $I_C = 10\text{ mAdc}$ , for $t_s$ ) ( $I_C = 100\text{ mA}$ for $t_f$ ) ( $I_{B1} = -10\text{ mA}$ ) ( $I_{B2} = 10\text{ mA}$ ) (Fig. 1, Test Condition C)	$t_s$	—	20	ns
Fall Time		$t_f$	—	15	ns
Turn–On Time	$(V_{CC} = 3.0\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $I_C = 10\text{ mAdc}$ , $I_{B1} = 3.0\text{ mAdc}$ ) (Fig. 1, Test Condition A)	$t_{on}$	—	25	ns
Turn–Off Time	$(V_{CC} = 3.0\text{ Vdc}$ , $I_C = 10\text{ mAdc}$ , $I_{B1} = 3.0\text{ mAdc}$ , $I_{B2} = 1.5\text{ mAdc}$ ) (Fig. 1, Test Condition A)	$t_{off}$	—	35	ns
Storage Time	$(V_{CC} = 10\text{ Vdc}$ , $I_C = 10\text{ mA}$ , $I_{B1} = I_{B2} = 10\text{ mAdc}$ ) (Fig. 1, Test Condition B)	$t_s$	—	20	ns
Total Control Charge	$(V_{CC} = 3.0\text{ Vdc}$ , $I_C = 10\text{ mAdc}$ , $I_B = \text{mAdc}$ ) (Fig. 3, Test Condition A)	$Q_T$	—	80	pC

1. Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle = 2.0%.

**Figure 1. Switching Time Equivalent Test Circuit**

Test Condition	$I_C$	$V_{CC}$	$R_S$	$R_C$	$C_S(\text{max})$	$V_{BE(off)}$	$V_1$	$V_2$	$V_3$
	mA	V	$\Omega$	$\Omega$	pF	V	V	V	V
<b>A</b>	10	3	3300	270	4	-1.5	10.55	-4.15	10.70
<b>B</b>	10	10	560	960	4	—	—	-4.65	6.55
<b>C</b>	100	10	560	96	12	-2.0	6.35	-4.65	6.55



CURRENT GAIN CHARACTERISTICS

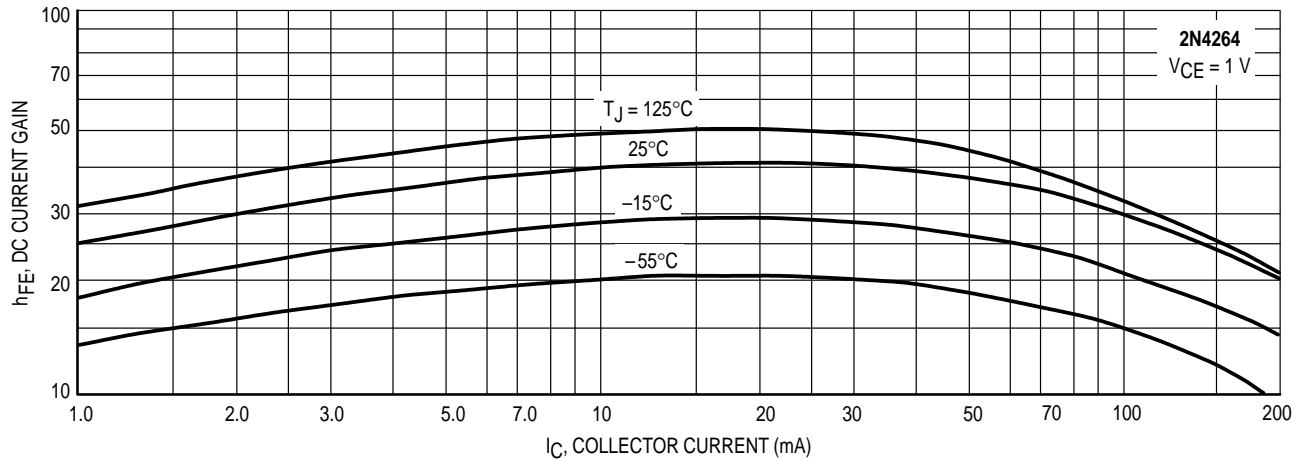


Figure 2. Minimum Current Gain

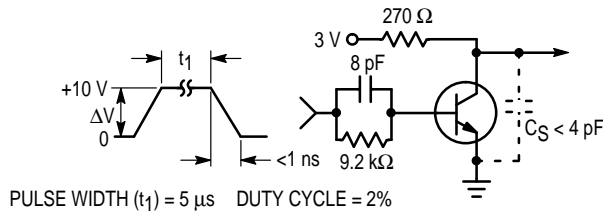


Figure 3.  $Q_T$  Test Circuit

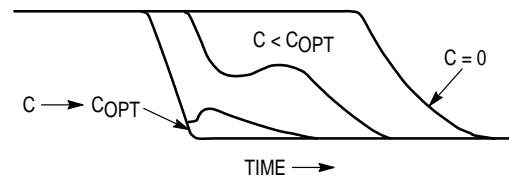


Figure 4. Turn-Off Waveform

NOTE 1

When a transistor is held in a conductive state by a base current,  $I_B$ , a charge,  $Q_S$ , is developed or "stored" in the transistor.  $Q_S$  may be written:  $Q_S = Q_1 + Q_V + Q_X$ .

$Q_1$  is the charge required to develop the required collector current. This charge is primarily a function of alpha cutoff frequency.  $Q_V$  is the charge required to charge the collector-base feedback capacity.  $Q_X$  is excess charge resulting from overdrive, i.e., operation in saturation.

The charge required to turn a transistor "on" to the edge of saturation is the sum of  $Q_1$  and  $Q_V$  which is defined as the active region charge,  $Q_A$ .  $Q_A = I_{B1}t_1$  when the transistor is driven by a constant current step

$$(I_{B1}) \text{ and } I_{B1} < < \frac{I_C}{h_{FE}}$$

If  $I_B$  were suddenly removed, the transistor would continue to conduct until  $Q_S$  is removed from the active regions through an external path or through internal recombination. Since the internal recombination time is long compared to the ultimate capability of a transistor, a charge,  $Q_T$ , of opposite polarity, equal in magnitude, can be stored on an external capacitor,  $C$ , to neutralize the internal charge and considerably reduce the turn-off time of the transistor. Figure 3 shows the test circuit and Figure 4 the turn-off waveform. Given  $Q_T$  from Figure 13, the external  $C$  for worst-case turn-off in any circuit is:  $C = Q_T/\Delta V$ , where  $\Delta V$  is defined in Figure 3.

“ON” CONDITION CHARACTERISTICS

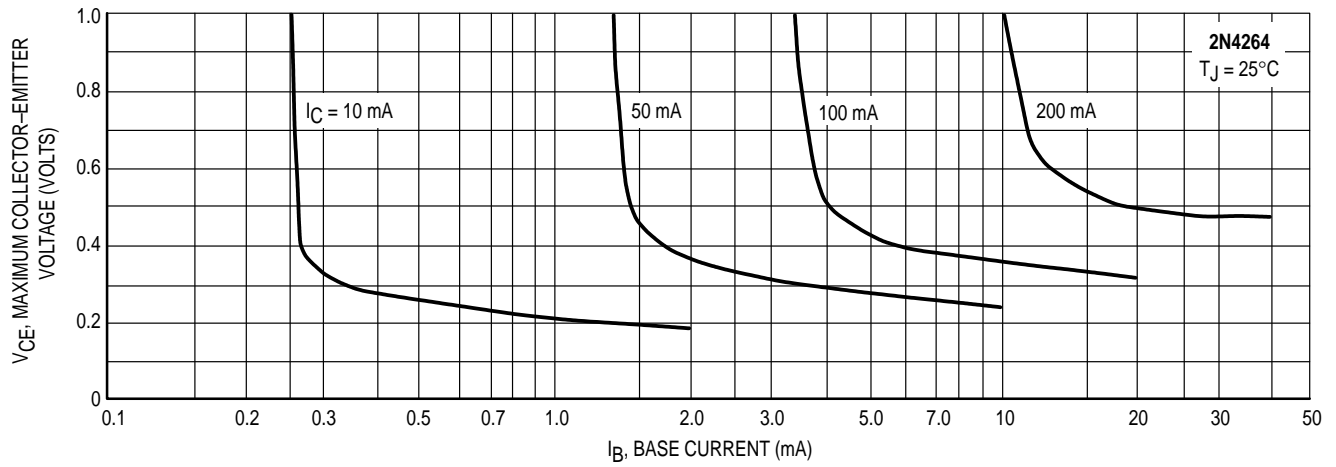


Figure 5. Collector Saturation Region

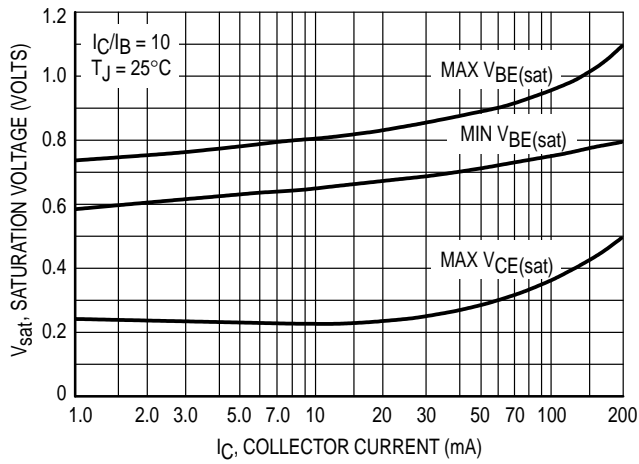


Figure 6. Saturation Voltage Limits

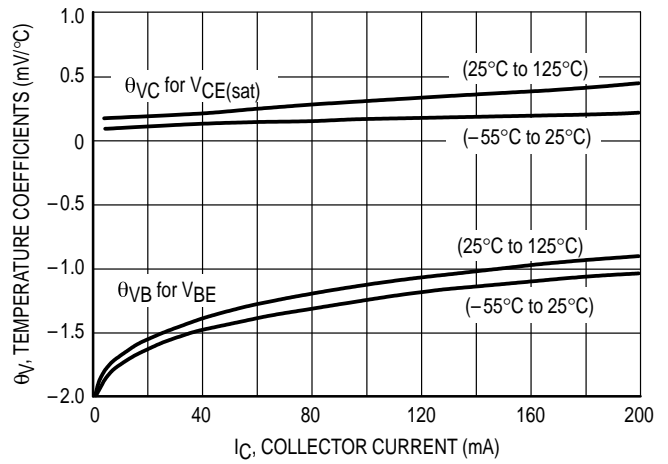


Figure 7. Temperature Coefficients

DYNAMIC CHARACTERISTICS

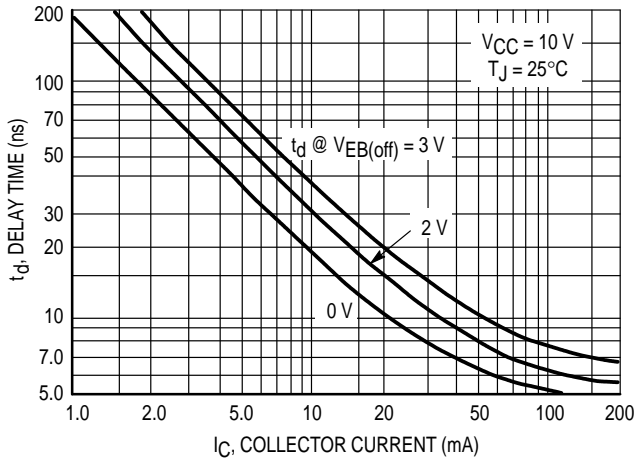


Figure 8. Delay Time

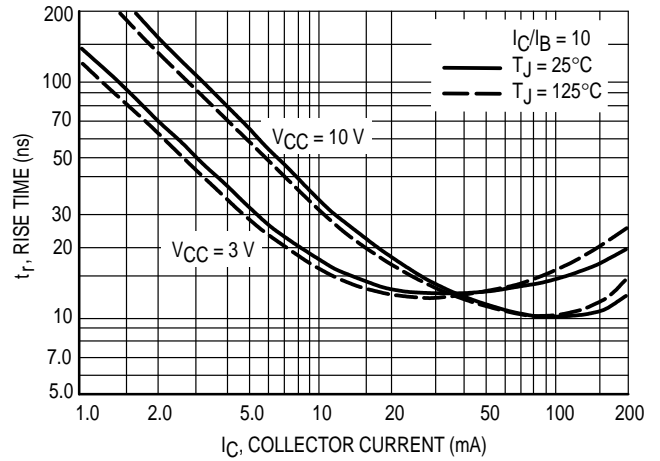


Figure 9. Rise Time

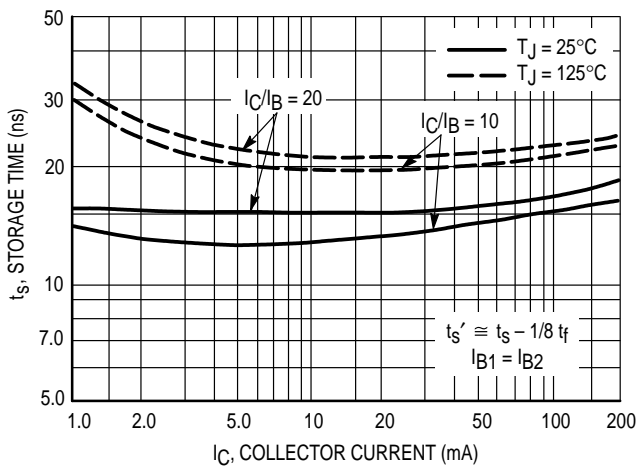


Figure 10. Storage Time

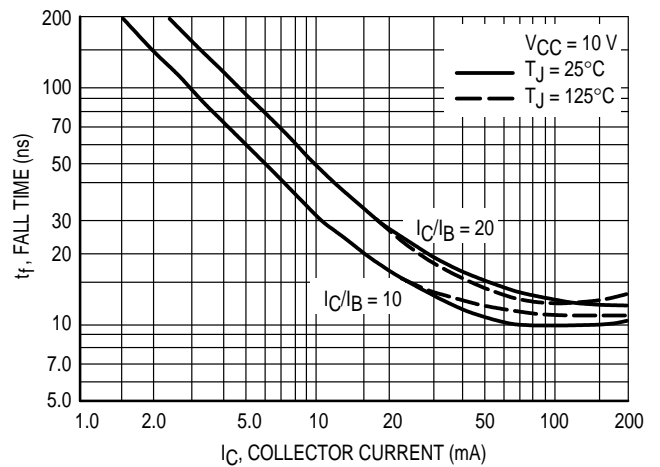


Figure 11. Fall Time

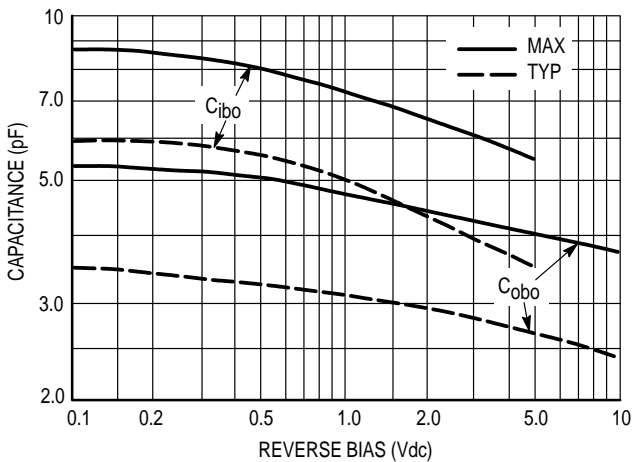


Figure 12. Junction Capacitance

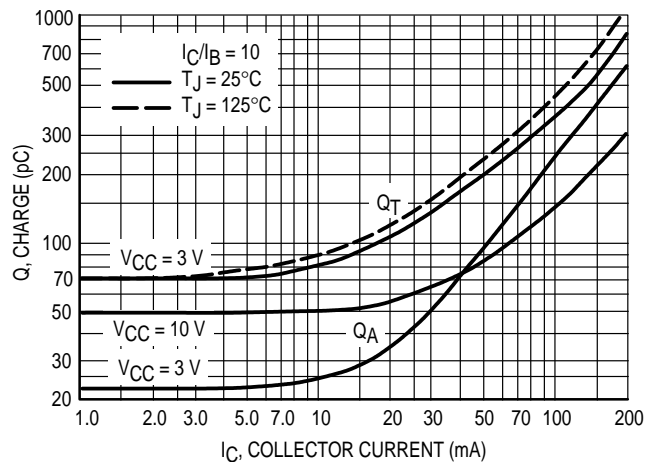
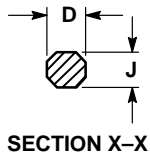
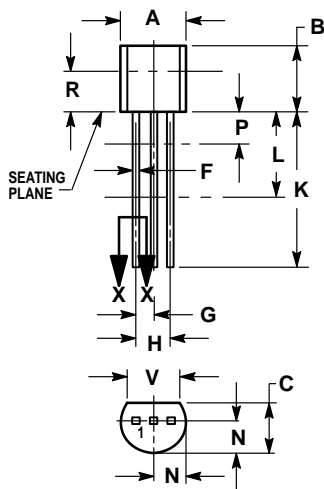


Figure 13. Maximum Charge Data

PACKAGE DIMENSIONS



CASE 029-04  
(TO-226AA)  
ISSUE AD

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
  4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K. MINIMUM LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

- STYLE 1:
1. EMITTER
  2. BASE
  3. COLLECTOR

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