

SANYO

No. 3353A

LA7956**Video Switch for TV / VCR Use****Features**

- 4 inputs, 1 output, 75Ω termination, driver on-chip
- 6dB amp on-chip
- Excellent crosstalk characteristic
- Wide band

Maximum Ratings at Ta = 25°C

			unit
Maximum Supply Voltage	V7 max	14	V
Maximum Input Supply Voltage (1)	V4 max, V6 max V8 max, V9 max,	8	V
Maximum Input Supply Voltage (2)	V2 max, V3 max	14	V
Maximum Output Current	I1 max	10	mA
Allowable Power Dissipation	Pd max	540	mW
Operating Temperature	Topr	-20 to +65	°C
Storage Temperature	Tstg	-55 to +150	°C

 $V_{CC} = 14V$ $T_a \leq 65^\circ C$ **Operating Conditions at Ta = 25°C**

			unit
Operating Voltage Range	$V_{CC\ op}$	10.5 to 13.5	V
Recommended Supply Voltage	V_{CC}	12	V

Operating Characteristics at Ta = 25°C, $V_{CC} = 12V$

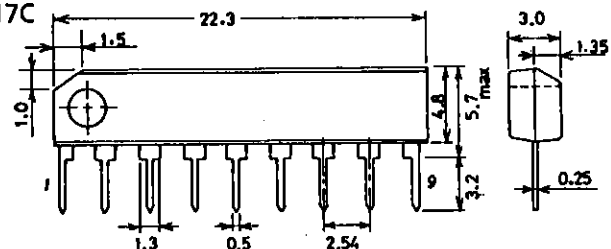
		min	typ	max	unit
Quiescent Current	I_{CC}	15	21	30	mA
Input Bias Voltage	V4, V6, V8, V9	3.5	3.8	4.1	V
Output Bias Voltage	V1	4.6	6.1	7.6	V
Output DC Offset Voltage	V_{OS} (Note 1)	-50	0	+50	mV
Control Threshold Voltage	V2H, V3H, V2L, V3L	2.3		0.7	V
Control Input Current	I2, I3	-20	-6		μA
Voltage Gain	GV	5.6	6.1	6.4	dB

 $f = 1MHz, V_{IN} = 2V_{pp}$ (Note 1)

Continued on next page.

Package Dimensions
(unit : mm)

3017C



SANYO : SIP9

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Frequency Characteristic	GV-f	[0dB at $f=100\text{kHz}$ (Note 1) $f=10\text{MHz}, V_{IN}=1\text{Vpp}$	min -3	typ 0	max	unit dB
Output Dynamic Range	V_{DR}	$f=15\text{kHz}, V_{IN}=1.5\text{p-p}$ (Note 1)	1.4	1.5		Vpp
Crosstalk (Note 2)	CT	$V_{IN}=1\text{Vp-p}, f=3\text{MHz}$ (Note 1)	50 (48)	58 (55)		dB
		$V_{IN}=1\text{Vp-p}, f=5\text{MHz}$ (Note 1)	45 (45)	55 (52)		dB

※ The current flowing into the IC is defined as positive and current from the IC is defined as negative.

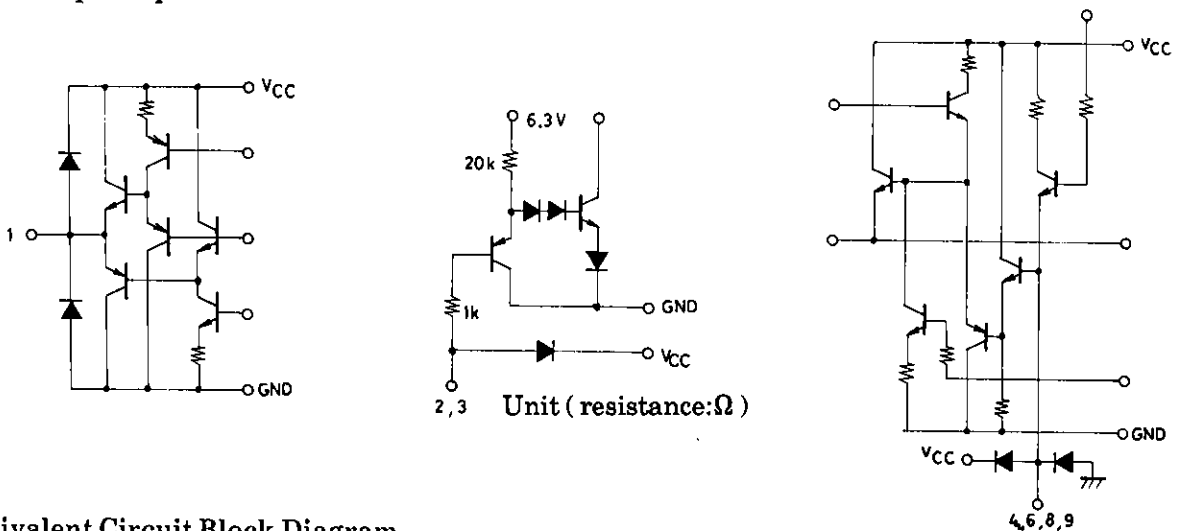
Video Switch Truth Table

S2 (Pin 2)	S3 (Pin 3)	V_{IN1} (Pin 4)	V_{IN2} (Pin 6)	V_{IN3} (Pin 8)	V_{IN4} (Pin 9)
H	H	ON	OFF	OFF	OFF
L	H	OFF	ON	OFF	OFF
H	L	OFF	OFF	ON	OFF
L	L	OFF	OFF	OFF	ON

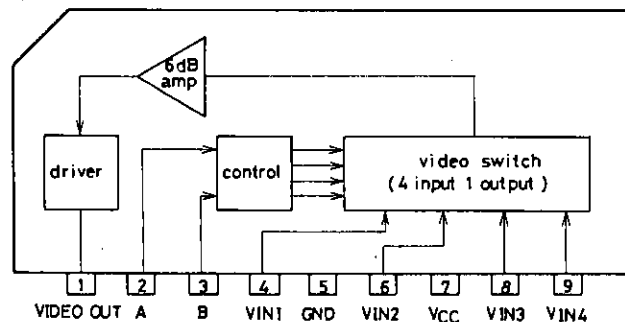
Note 1 : Refer to this Truth Table and make measurements by switching S2, S3.

Note 2 : () : Crosstalk between pins 8 and 9

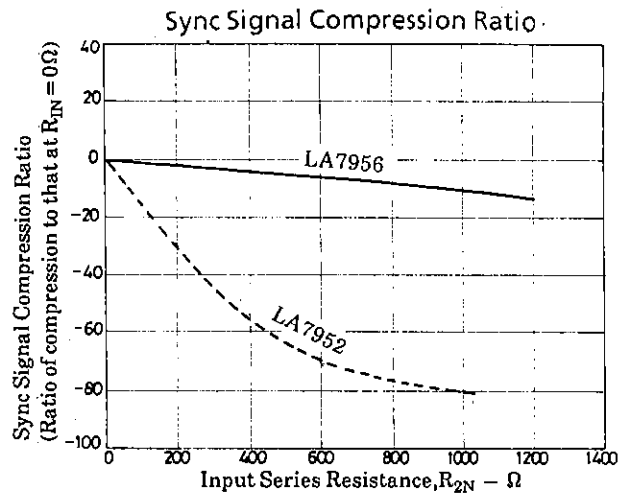
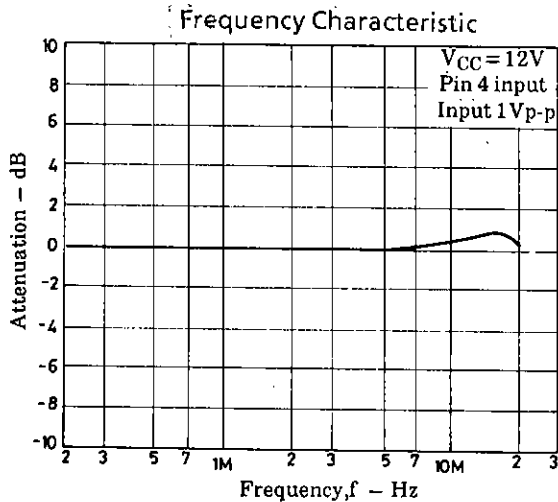
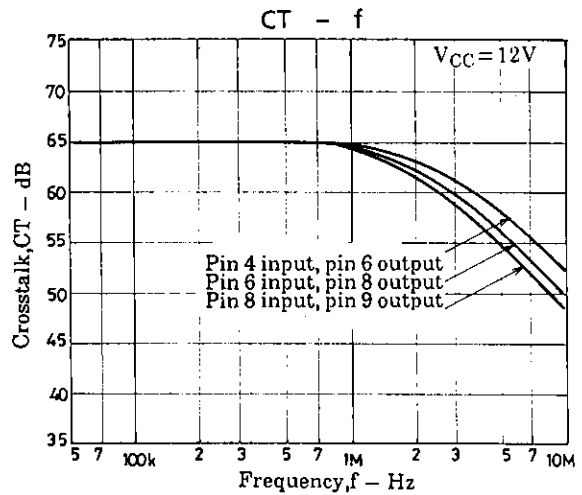
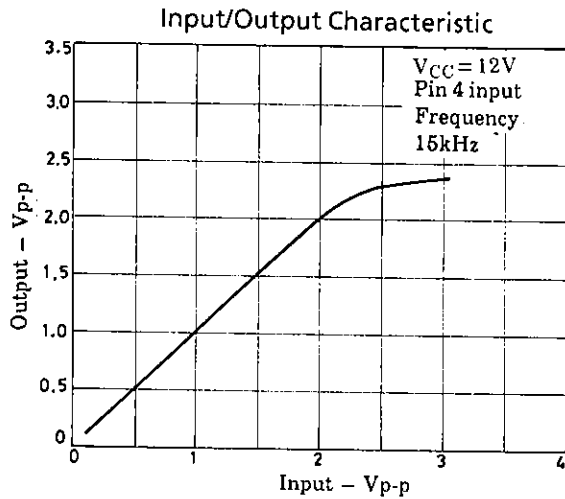
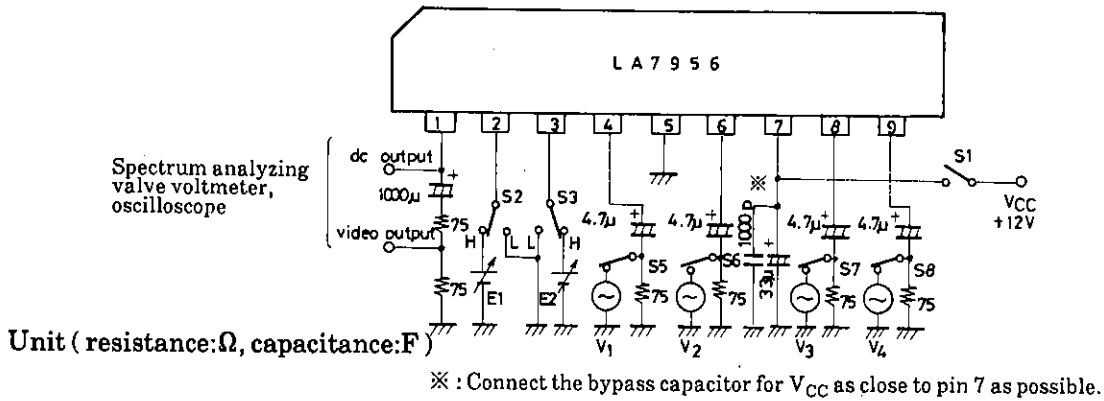
Input/Output Equivalent Circuit



Equivalent Circuit Block Diagram



Test Circuit



Design Notes

An improvement in the DC clamp circuit has improved the sync signal compression attributable to the signal source impedance, but the response time of the DC clamp is made longer accordingly than that of the LA7952. Make adjustments by connecting a high resistance (several hundred kΩ) across input pin and GND (decreasing the resistance makes the sync signal compression larger).

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