M51978P,FP

SWITCHING REGULATOR CONTROL

DESCRIPTION

Mitsubish IC type M51978P, FP are primary swiching regulator controller which are especially designed to get the regulated DC voltage from AC power supply.
These IC can directly drive the MOS-FET with fast rise and fast fall output pulse and with a large-capacity totem pole output.
Type M51978P, FP have the functions of not only high frequency OSC and fast output drive but also current limit with fast response and high sensibility so the true "fast switching regulator" can be realized.

FEATURES

- 500kHz operation to MOS-FET
  - Output current ..... ±1A
  - Output rise time 60ns, fall time 40ns
  - Modified totempole output method with small through current
- Compact and light-weight power supply
  - Small start-up current ..... 100μA typ.
  - Big difference between "start-up voltage" and "stop voltage" makes the smoothing capacitor of the power input section small.
    Start-up threshold 16V, stop voltage 10V
- Packages with high power dissipation are used to withstand the heat generated by the gate-drive current of MOS FET.
  14-pin DIP, 16-pin SOP 1.5W (at 25℃)
- Simplified peripheral circuit with protection circuit and built-in large-capacity totempole output
  - High-speed current limiting circuit using pulse-by-pulse method (CLM + terminal)
  - Over-voltage protection circuit with a single signal input (OVP)
  - Output error prevention circuit at low supply voltage (UVLO)
- High-performance and highly functional power supply
  - Triangular wave oscillator for easy dead time setting
  - Soft start function by expanding period

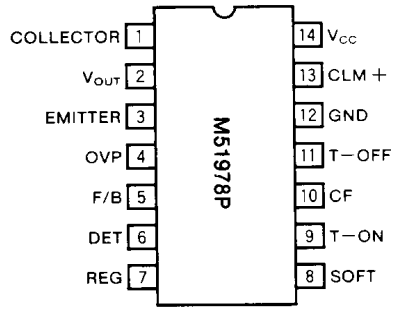
APPLICATION

Feed forward regulator, Fly-back regulator

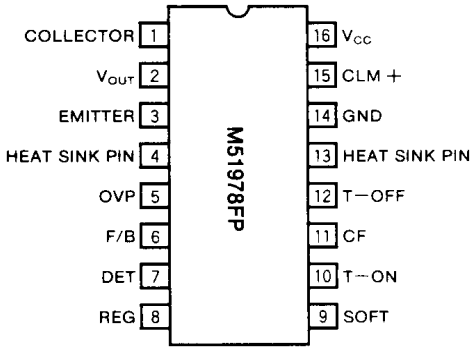
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... 12~30V
Operating frequency ..... less than 500kHz
Oscillator frequency setting resistance
- T—ON pin resistance R_{ON} ..... 10k~75kΩ
- T—OFF pin resistance R_{OFF} ..... 2k~30kΩ

PIN CONFIGURATION (TOP VIEW)



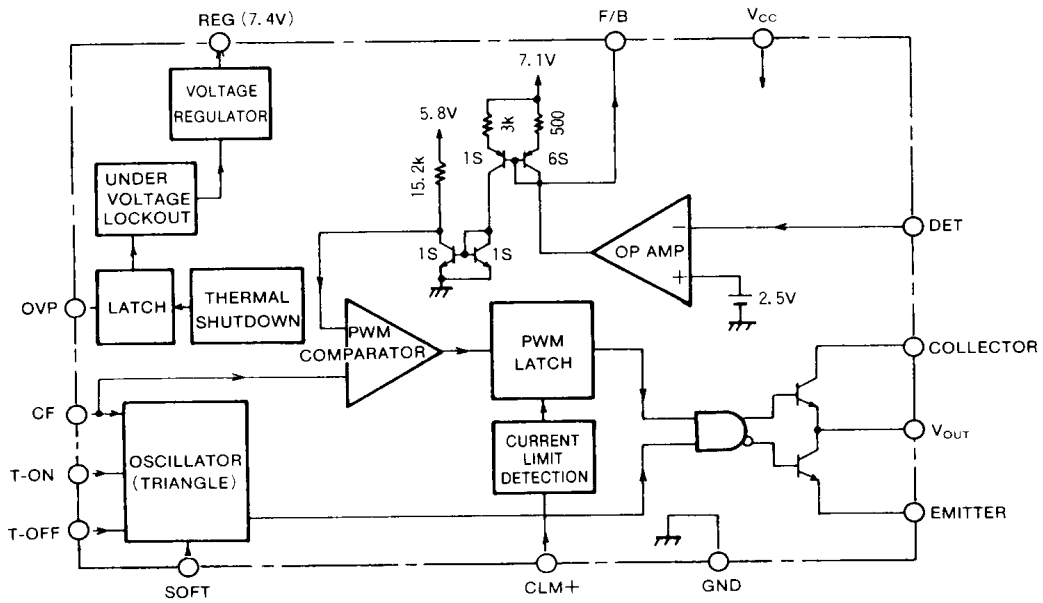
Outline 14P4



Outline 16P2N

Connect the heat sink pin to GND.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		31	V
V_C	Collector voltage		31	V
I_O	Output current	Peak	±1	A
		Continuous	±0.15	
I_{VREG}	VREG terminal output current		−6	mA
V_{SOFT}	SOFT terminal voltage		VREG+0.2	V
V_{CLM+}	CLM+ terminal voltage		−0.3~3	V
V_{DET}	DET terminal voltage		6	V
V_{OVP}	OVP terminal voltage		V_{CC}	V
$I_{F/B}$	F/B terminal current		−10	mA
I_{TON}	T-ON terminal input current		−1	mA
I_{TOFF}	T-OFF terminal input current		−2	mA
P_d	Power dissipation	T_a=25℃	1.5	W
$K\theta$	Thermal derating	T_a>25℃	12	mW/℃
T_{opr}	Operating temperature		−30~+85	℃
T_{stg}	Storage temperature		−40~125	℃

Note : "+" sign shows the direction of current flowing into the IC and "−" sign shows the current flowing out from the IC.

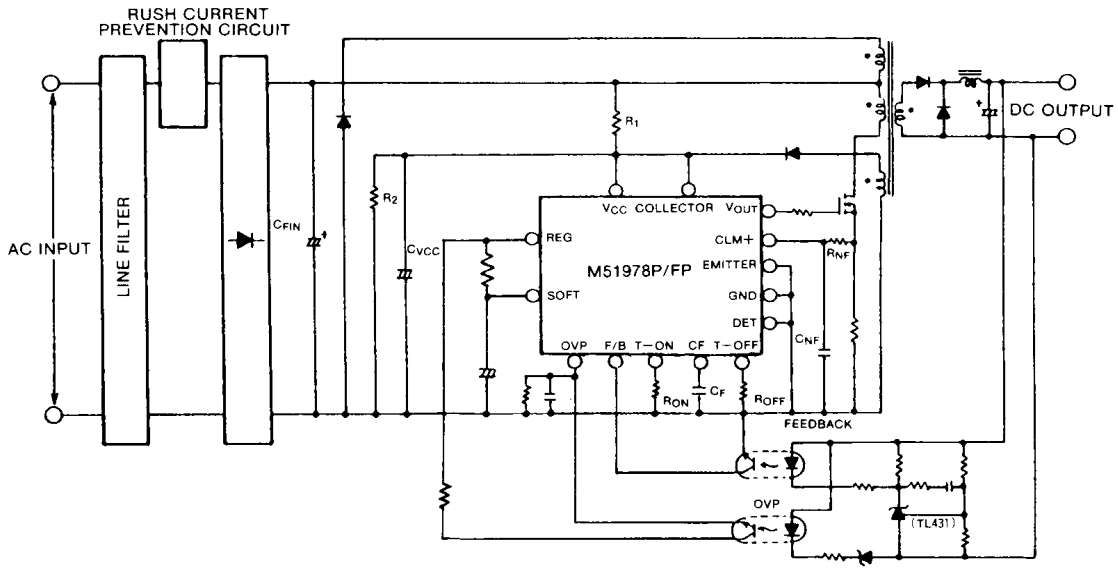
ELECTRICAL CHARACTERISTICS (V_{CC}=18V, T_a=25℃, unless otherwise noted)

Block	Symbol	Parameter	Test Conditions	Limits			Unit
				Min	Typ	Max	
Supply voltage/circuit current	V_{CC}	Operating supply voltage range		V_{CC} (STOP)	—	30	V
	$V_{CC(START)}$	Operation start up voltage		15.2	16.2	17.2	V
	$V_{CC(STOP)}$	Operation stop voltage		9.0	9.9	10.9	V
	ΔV_{CC}	$V_{CC(START)}$, $V_{CC(STOP)}$ difference	$\Delta V_{CC}=V_{CC(START)}-V_{CC(STOP)}$	5.0	6.3	7.6	V
	I_{CCL}	Stand-by current	V_{CC}=14.5V T_a=25℃	65	100	150	μA
			V_{CC}=14.5V −30℃≤T_a≤85℃	50	100	200	
	I_{CCO}	Operating circuit current	V_{CC}=15V, f=188kHz	7.3	11	17	mA
			V_{CC}=30V, f=188kHz	8	12	19	
	I_{CCOVP}	Circuit current in OVP state	V_{CC}=25V	1.3	2.0	3.0	mA
			V_{CC}=9.5V	140	210	320	μA
F/B	I_{FBMIND}	Current at 0% duty	F/B terminal input current	−2.1	−1.5	−1.0	mA
	I_{FBMAXD}	Current at maximum duty	F/B terminal input current	−0.9	−0.6	−0.4	mA
	ΔI_{FB}	Current difference between max and 0% duty	$\Delta I_{FB}=I_{FBMIND}-I_{FBMAXD}$	−1.35	−0.99	−0.70	mA
	V_{FB}	F/B terminal voltage	F/B terminal input current=0.95mA	4.9	5.9	7.1	V
	R_{FB}	OVP terminal resistance		420	600	780	Ω
OVP	V_{THOVP}	OVP terminal threshold voltage		1.00	1.40	1.80	V
	I_{INOVP}	OVP terminal input current		—	1.0	4.0	μA
	V_{CCOVPC}	OVP reset supply voltage		7.5	8.5	9.5	V
	$V_{CC(STOP)}-V_{CCOVPC}$	Difference voltage between operation stop and OVP reset		0.65	1.30	—	V
CLM+	V_{THCLM+}	CLM+ terminal threshold voltage		180	200	220	mV
	I_{INCLM+}	CLM+ terminal current	V_{CLM+}=0V	−280	−200	−140	μA
	T_{PDCLM+}	Delay time from CLM+ to V_{OUT}		—	150	—	ns
Oscillator	f_{OSC}	Oscillating frequency	R_{ON}=20kΩ C_F=220pF	170	188	207	kHz
	T_{DUTY}	Maximum ON duty	R_{OFF}=17kΩ, −5≤T_a≤85℃	47	50	53	%
	V_{OSCH}	Upper limit voltage of oscillation waveform	R_{ON}=20kΩ, R_{OFF}=17kΩ C_F=220pF	3.97	4.37	4.77	V
	V_{OSCL}	Lower limit voltage of oscillation waveform		1.76	1.96	2.16	V
	ΔV_{OSC}	Voltage difference between upper limit and lower limit of OSC waveform		2.11	2.41	2.71	V
	V_{T-ON}	T−ON terminal voltage	R_{ON}=20kΩ	3.8	4.5	5.4	V
	V_{T-OFF}	T−OFF terminal voltage	R_{OFF}=17kΩ	2.9	3.5	4.2	V
SOFT	$f_{OSCSOFT}$	Oscillating frequency during SOFT operation (V_{SOFT}=5.5V)	R_{ON}=20kΩ, R_{OFF}=17kΩ, C_F=220pF	170	188	207	kHz
		(V_{SOFT}=2.5V)		111	131	151	kHz
		(V_{SOFT}=0.2V)		19.0	23.3	27.0	kHz
	I_{SOFTIN}	SOFT terminal input current	V_{SOFT}=1V	−0.5	−0.1	—	μA
	$I_{SOFTDIS}$	SOFT terminal discharging current	Discharge current of SOFT terminal at V_{CC} less than $V_{CC(STOP)}$	1	3.3	—	mA
REG	V_{REG}	Regulator output voltage		6.8	7.8	8.8	V
Output	V_{OL1}	Output low voltage	V_{CC}=18V I_O=10mA	—	0.04	0.4	V
	V_{OL2}		V_{CC}=18V I_O=100mA	—	0.7	1.4	V
	V_{OL3}		V_{CC}=5V I_O=1mA	—	0.85	1.0	V
	V_{OL4}		V_{CC}=5V I_O=100mA	—	1.30	2.0	V
	V_{OH1}	Output high voltage	V_{CC}=18V I_O=−10mA	16.0	16.7	—	V
	V_{OH2}		V_{CC}=18V I_O=−100mA	15.5	16.5	—	V
	T_{RISE}	Output voltage rise time		—	60	—	ns
	T_{FALL}	Output voltage fall time		—	40	—	ns
Detection	V_{DET}	Detecting voltage		2.4	2.5	2.6	V
	I_{INDET}	DET terminal input current	V_{DET}=2.5V	—	1.0	3.0	μA
	G_{AVDET}	Voltage gain of detection amp		30	40	—	dB
Over heating	T_{TS}	Thermal shutdown temperature		120	140	160	℃

FUNCTION DESCRIPTION

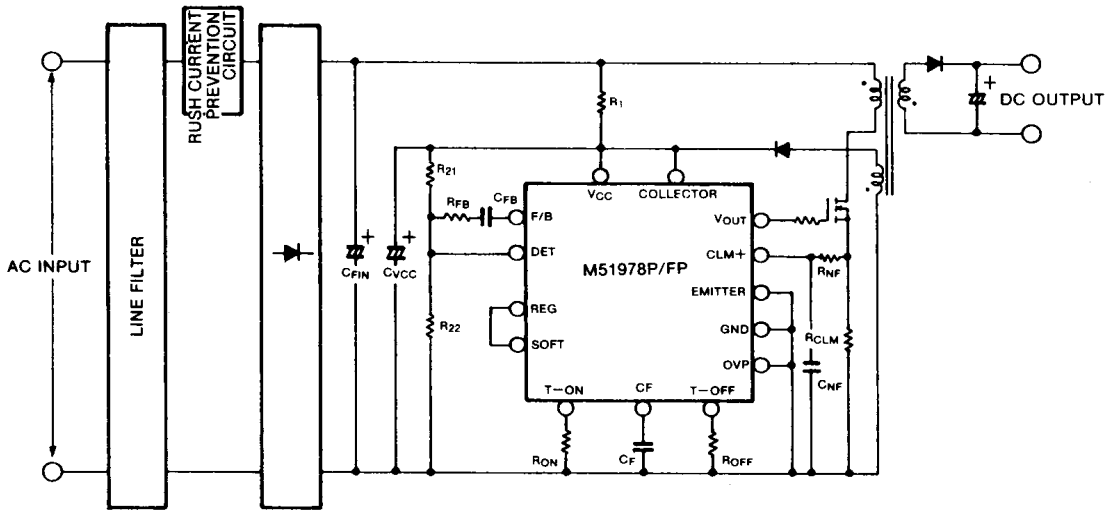
Types M51978P and M51978FP are especially designed for off-line primary PWM contorl IC of switching mode power supply to get DC voltage from AC power supply.
Using this IC, smart SMPS can be realized with reasonable cost and compact size as the number of external electric parts can be reduced and also parts can be replaced by reasonable one.
In the following circuit diagram, MOS-FET is used for output transistor, however, bipolar transistor can be replaced with no problem.

Application example



Soft start and OVP functions are used.
RC with small time constant connected to CLM+ pin is used to reduce noise when the MOS-FET is ON.
Small resistors connected to MOS FET gate is used to suppress noise generated from the MOS FET.

Fig.1 Application example of feed forward regulator



How to obtain regulated output voltage using the winding ratio of the transformer.
Soft start and OVP function are not used. (Even though soft start is not used, pulse-by-pulse current limit method prevents destruction of the device by a rush current at power on.) RC with small time constant connected to CLM+ pin is used to reduce noise when MOS-FET is switched on. Small resistor connected to MOS-FET gate is used to suppress noise generated from the MOS-FET.

Fig.2 Application example of fly-back regulator

Start-up circuit section

Fig. 3 shows that the start-up current is the low current level of 100μA typ. when the V_{CC} voltage is increased from low level to start-up voltage $V_{CC(START)}$.
In this voltage range, only a few parts in this IC, which functions make the output voltage low level, are alive. The I_{CC} current is used to keep output low level.
The large voltage difference between $V_{CC(START)}$ and $V_{CC(STOP)}$ makes start-up easy, because it takes rather long duration from $V_{CC(START)}$ to $V_{CC(STOP)}$.

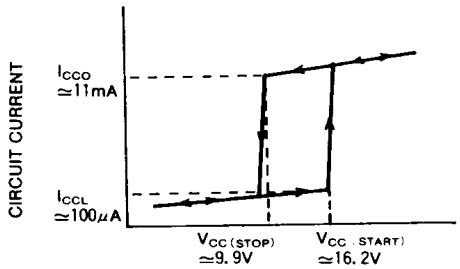


Fig.3 Start-up current vs. supply voltage

Oscillator section

The M51978 oscillator waveform is triangular one as shown in Fig. 5. The ON duration of output pulse depends on the rising duration of the triangle waveform and dead time is decided by the falling duration.
The rising duration is determined by the product of external resistor R_{ON} and capacitor C_F and the falling duration is mainly determined by the product of external resistor R_{OFF} and capacitor C_F.

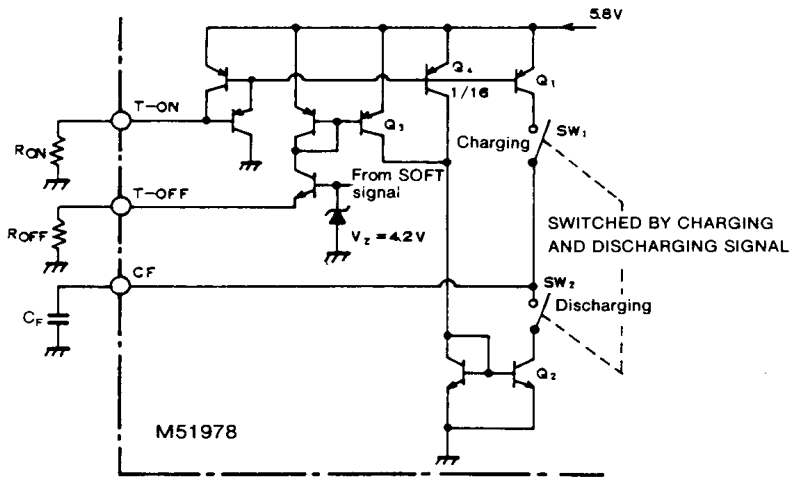


Fig.4 Control circuit for charging and discharging oscillator capacitor C_F

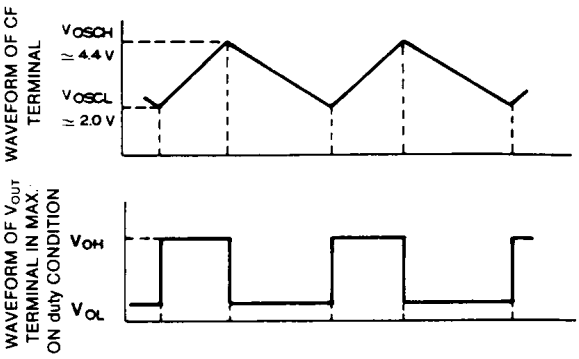


Fig.5 Oscillator waveform at normal condition (when the SOFT circuit is not operating.)

(1)Oscillator circuit operation when SOFT circuit does not operate. (Normal operation)

Fig. 4 shows the equivalent charging and discharging circuit diagram of oscillator.

The current flows through R_{ON} from the constant voltage source of 5.8V, C_F is charged up by the same amplitude as R_{ON} current, when internal switch SW_1, SW_2 is switched to "charging side".

The rise rate of C_F terminal is given as

$$\simeq \frac{V_{T-ON}}{R_{ON} \cdot C_F} \text{ (V/s)} \quad \cdots\cdots (1)$$

where $V_{T-ON} \simeq 4.5V$

The maximum on duration is approximately given as

$$\simeq \frac{(V_{OSCH} - V_{OSCL}) \cdot R_{ON} \cdot C_F}{V_{T-ON}} \text{ (s)} \quad \cdots\cdots (2)$$

where, $V_{OSCH} \simeq 4.4V$

$V_{OSCL} \simeq 2.0V$

C_F is discharged by the summed-up of R_{OFF} current and one sixteenth (1/16) of R_{ON} current by the function of Q_2, Q_3 and Q_4 when SW_1, SW_2 are switched to "discharge side".

The fall rate of oscillation waveform is given as

$$\simeq \frac{V_{T-OFF}}{R_{OFF} \cdot C_F} + \frac{V_{T-ON}}{16 \cdot R_{ON} \cdot C_F} \text{ (V/s)} \quad \cdots\cdots (3)$$

The minimum off duration approximately is given as

$$\simeq \frac{(V_{OSCH}-V_{OSCL})\cdot C_F}{\frac{V_{T-OFF}}{R_{OFF}}+\frac{V_{T-ON}}{16\cdot R_{ON}}}\ (s) \quad \cdots\cdots (4)$$

$V_{T-OFF} \simeq 3.5V$,

The period of oscillator waveform is given by the sum of equations (2) and (4). The frequency including the dead-time is not influenced by the temperature because of the built-in temperature conpensating circuit.

(2)Oscillator operation when the SOFT (soft start) circuit is operating

Output transistor is protected from rush current by CLM function at the start time of power on. SOFT terminal is used to improve the rising response of the output voltage of power supply (prevention of overshooting).

The ON duration of output is kept constant, and the OFF duration is extended as the SOFT terminal voltage becomes lower by the soft start circuit of this IC.

The maximum value of extension is set internally at approximately sixteen times of the maximum ON duration.

The features of this method are as follows:

① It is ideal for primary control as IC driving current is supplied from the third widing of the main transformer at the start-up because constant ON duration is obtained from start-up.

② It is possible to get a wide dynamic range for ON/OFF ratio by pulse-by-pulse current limit circuit.

③ The response characteristics at power-on is not affected by input voltage as the pulse-by-pulse limit current value is not affected by the input voltage.

Fig. 6 shows the circuit diagram of the soft start. If SOFT terminal voltage is low, T−OFF terminal voltage becomes low and V_{T-OFF} in equations (3) and (4) become low.

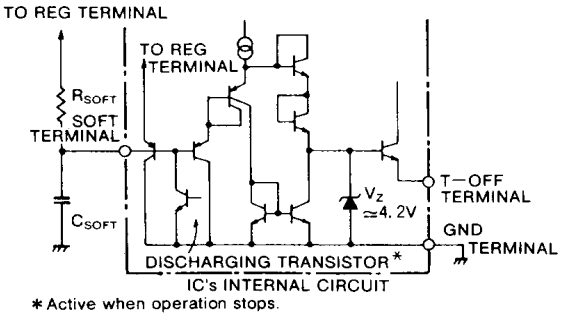


Fig.6 Circuit diagram of SOFT terminal section and T−OFF terminal section

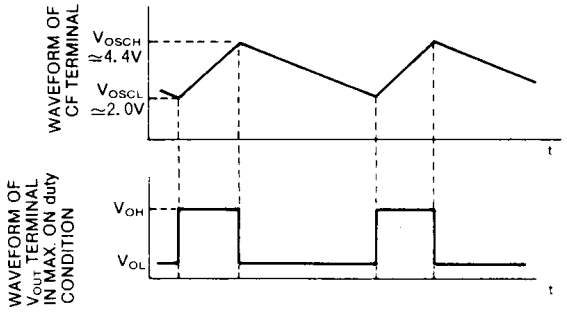


Fig.7 Oscillator waveform when the SOFT circuit is operating

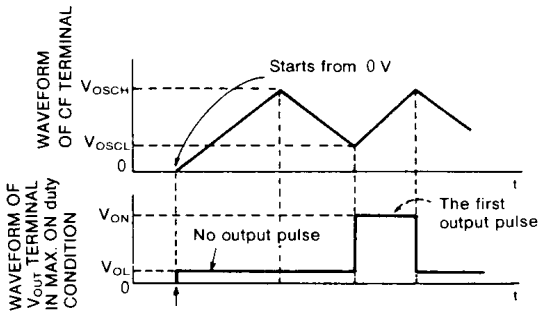


Fig.8 Relationship between oscillator waveform and output waveform at start-up

Fig. 7 shows the relationship between oscillator waveform and output puise.

If the SOFT terminal voltage is V_{SOFT}, the rise rate of CF terminal is given as

$$\simeq \frac{V_{T-ON}}{R_{ON}\cdot C_F}\ (V/S) \quad \cdots\cdots (5)$$

The fall rate of oscillation waveform is given as

$$\simeq \frac{V_{SOFT}-V_{BE}}{R_{OFF}\cdot C_F}+\frac{V_{T-ON}}{16\cdot R_{ON}\cdot C_F}\ (V/S) \quad \cdots\cdots (6)$$

where

V_{SOFT}; SOFT terminal applied voltage

$V_{BE} \simeq 0.65V$

If $V_{SOFT}-V_{BE}<0$, $V_{SOFT}-V_{BE}=0$

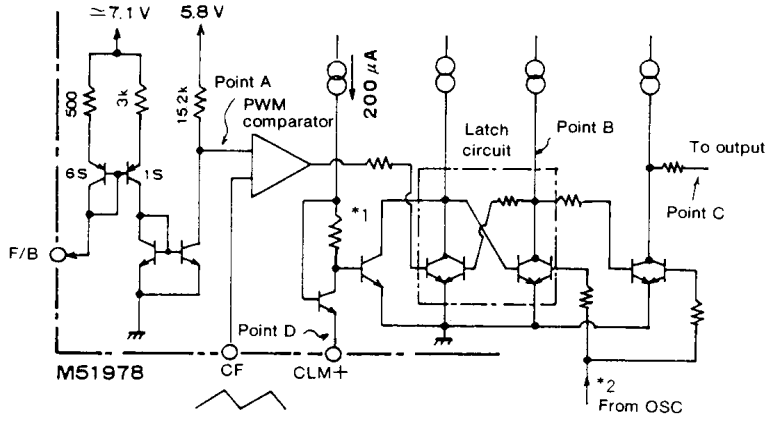
If $V_{SOFT}-V_{BE}>V_{T-OFF}$ ($\simeq 3.5V$), $V_{SOFT}-V_{BE}=V_{T-OFF}$

PWM comparator section, PWM latch section, current limit latch section

Fig. 9 shows the schematic diagram of PWM comparator and PWM latch section. The on-duration of output waveform coincides with the rising duration of CF terminal waveform when the no output current flows from F/B terminal.

When the F/B terminal has finite impedance and current

flows out from F/B terminal, "A" point potential shown in Fig. 9 depends on this current. So the "A" point potential is close to GND level when the flow-out current becomes large.
"A" point potential is compared to the CF terminal oscillator waveform and PWM comparator, and the latch circuit is set when the potential of oscillator waveform is higher than "A" point potential. The latch circuit is reset during the dead time of oscillator circuit (falling duration of oscillator



*1; Resistor to determine current limit sensitivity *2 ; High-level during dead time

Fig.9 PWM comparator section, PWM latch and current limit latch section

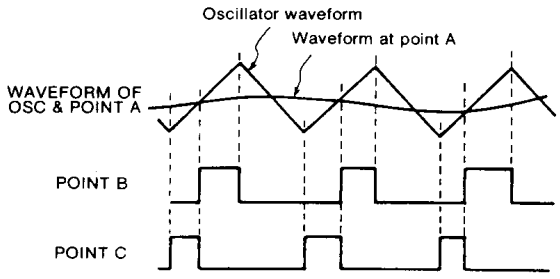


Fig.10 Waveforms of PWM comparator input point A, latch circuit points B and C

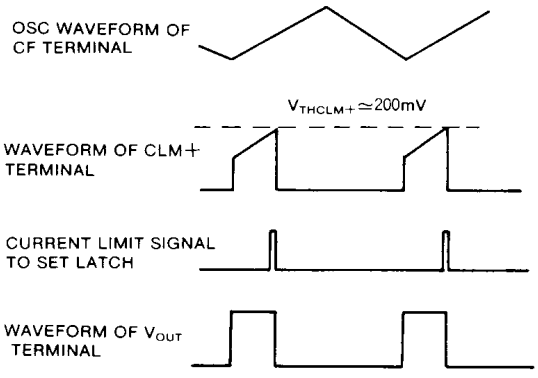


Fig.11 Operating waveforms of current limitting circuit

circuit). So the "B" point potential or output waveform of latch circuit is the one shown in Fig. 10. The final output waveform or "C" point potential is got by combining the "B" point signal and dead-time signal logically.
(please refer to Fig. 10)

Current limitting section

When the current-limit signal is applied before the crossing instant of "A" point potential and CF terminal voltage shown in Fig. 9, this signal makes the output "off" and the off state will continue until next cycle. Fig. 11 shows the timing relation among them.
If the current limitting circuit is set, no waveform is generated at output terminal, however this state is reset during the succeeding dead-time.
So this current limitting circuit is able to have the function in every cycle, and is named "pulse-by-pulse current limit."
There happen some noise voltage on R_{CLM} during the switching of power transistor due to the snubber circuit and stray capacitor of the transformer windings.
To eliminate the abnormal operation by the noise voltage, the low pass filter, which consists of R_{NF} and C_{NF} is used as shown in Fig. 12.
It is recommended to use 10~100Ω for R_{NF} because such

range of R_{NF} is not influenced by the flow-out current of some 200μA from CLM terminal and C_{NF} is designed to have the enough value to absorb the noise voltage.

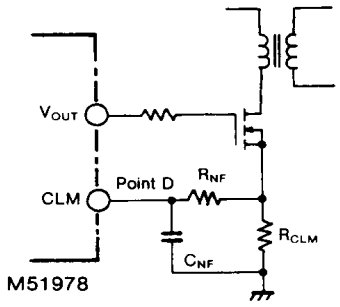


Fig.12 Connection diagram of current limit circuit

Voltage detector circuit (DET) section

The DET terminal can be used to control the output voltage which is determined by the winding ratio of fly back transformer in fly-back system or in case of common ground circuit of primary and secondary in feed forward system.

The circuit diagram is quite similar to that of shunt regulator type 431 as shown in Fig. 13. As well known from Fig. 13 and Fig. 14, the output of OP AMP has the current-sink ability, when the DET terminal voltage is higher than 2.5V but it becomes high impedance state when lower than 2.5V. DET terminal and F/B terminal have inverting phase characteristics each other, so it is recommended to connect the resistor and capacitor in series between them for phase compensation. It is very important one can not connect by resistor directly as there is the voltage difference between them and the capacitor has the DC stopper function.

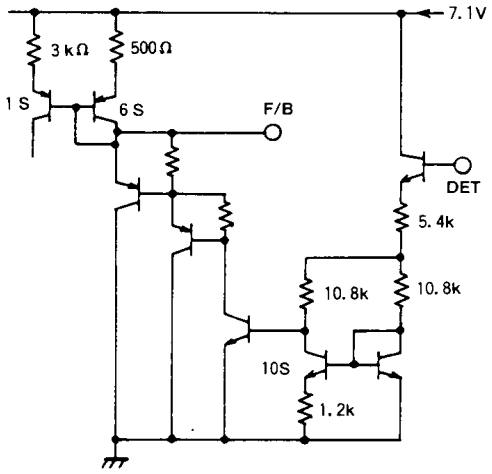


Fig.13 Voltage detector circuit section (DET)

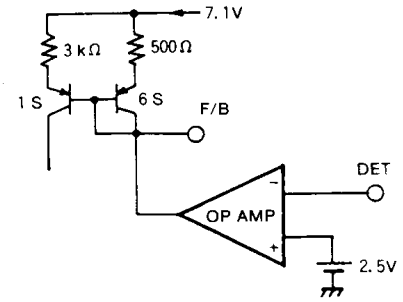


Fig.14 Schematic diagram of voltage detector circuit section (DET)

OVP circuit section

OVP circuit is basically constructed by the complementary flip-flop circuit as shown in Fig. 15. Once the input signal is applied to the OVP circuit which has the detect sensitivity of $2V_{BE}$ the output becomes "off" and this "off" state will be kept unitil V_{CC} becomes to less than OVP reset voltage($\simeq$ 8.5V).

As the OVP "off" state is kept by the current through R_1 shown in Fig. 1 and 2. M51978 is designed to have the low I_{CC}, which value is some level of adding 10μA to the start-up current at OVP reset voltage.

As M51978 has such the I_{CC} versus V_{CC} characteristics as shown in Fig. 16, no failure is occured by applied high vol-

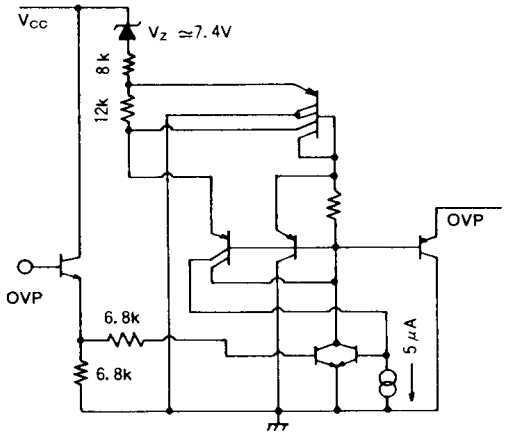


Fig.15 Detail diadram of OVP circuit

tage to IC. That is; higher the V_{CC} or DC supply voltage, higher the I_{CC} current and larger the voltage drop at R_1.
As the OVP reset voltage is settled rather high voltage of 8.5V, SMPS can be reset in rather short time from the switch-off of AC power source if the smoothing capacitor is not so large value.
However the reset time may become problem when the C_{FIN} is large and so the discharge time constant of $C_{FIN} \times (R_1+R_2)$ is large.

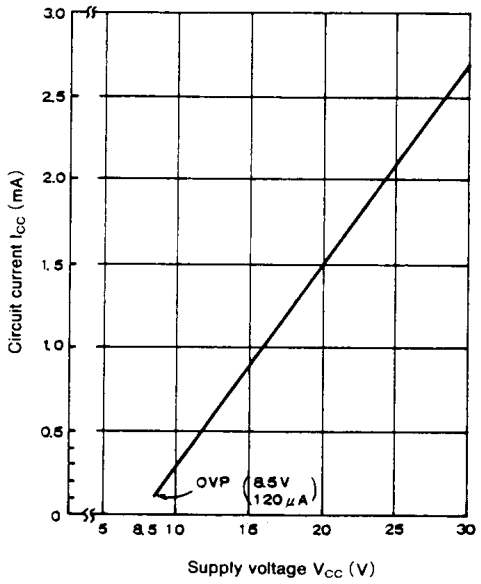


Fig.16 Circuit current vs. supply voltage during OVP circuit operation

Output section

It is required that the output circuit have the high sink and source abilities for MOS-FET drive. It is well known that the "totempole circuit has high sink and source ability. However, it has the demerit of high through current.
For example, the through current may reach such the high current level of 1A, if type M51978 has the "conventional" totempole circuit. For the high frequency application such as higher than 100kHz, this through current is very important factor and will cause not only the large I_{CC} current and the inevitable heat-up of IC but also the noise voltage.
This IC uses the improved totempole circuit, so without deteriorating the characteristic of operating speed, its through current is approximately 100mA.

APPLICATION NOTE OF TYPE M51978P,FP Design of start-up circuit and the power supply of IC

(1)The start-up circuit when it is not necessary to set the start and stop input voltage

Fig. 17 shows one of the example circuit diagram of the start-up circuit which is used when it is not necessary to set the start and stop voltage.
It is recommended that the current more than 300μA flows through R_1 in order to overcome the operation start-up current $I_{CC(START)}$ and C_{VCC} is in the range of 10 to 47μF. The product of R_1 by C_{VCC} causes the time delay of operation, so the response time will be long if the product is too much large.

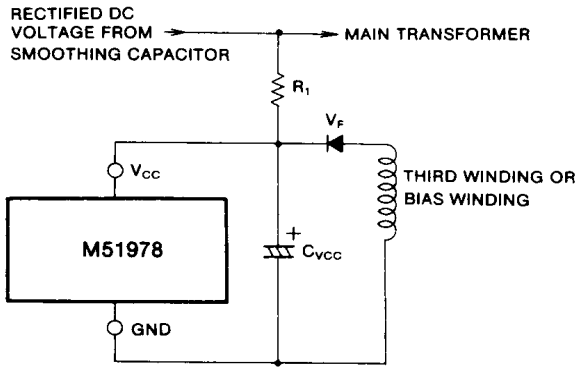


Fig. 17 Start-up circuit diagram when it is not necessary to set the start and stop input voltage

Just after the start-up, the I_{CC} current is supplied from C_{VCC}, however, under the steady state condition, IC will be supplied from the third winding or bias winding of transformer, the winding ratio of the third winding must be designed so that the induced voltage may be higher than the operation-stop voltage $V_{CC(STOP)}$.
The V_{CC} voltage is recommended to be 12V to 17V as the normal and optimum gate voltage is 10 to 15V and the output voltage (V_{OH}) of type M51978P, FP is about (V_{CC}−2V).
It is not necessary that the induced voltage is settled higher than the operation start-up voltage $V_{CC(START)}$, and the high gate drive voltage causes high gate dissipation, on the other hand, too low gate drive voltage does not make the MOS-FET fully on-state or the saturation state.

(2)The start-up circuit when it is necessary to set the start and stop input voltage

It is recommend to use the third winding of "forward winding" or "positive polarity" as shown in Fig. 18, when the DC source voltages at both the IC operation start and stop must be settled at the specified values.
The input voltage ($V_{IN(START)}$), at which the IC operation

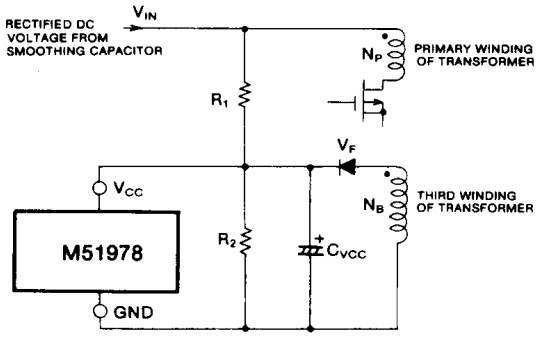


Fig. 18 Start-up circuit diagram when it is necessary to set the start and stop input voltage

starts, is decided by R_1 and R_2 utilizing the low start-up current characterisitics of type M51978P, FP.

The input voltage ($V_{IN\,(STOP)}$), at which the IC operation stops, is decided by the ratio of third winding of transformer.

The $V_{IN\,(START)}$ and $V_{IN\,(STOP)}$ are given by following equations.

$$V_{IN(START)} \simeq R_1 \cdot I_{CCL} + \left(\frac{R_1}{R_2}+1\right) \cdot V_{CC(START)} \quad \cdots\cdots(7)$$

$$V_{IN(STOP)} \simeq (V_{CC(STOP)} - V_F) \cdot \frac{N_P}{N_B} + \frac{1}{2} V'_{IN\ RIP(P\text{-}P)} \quad \cdots\cdots(8)$$

where

I_{CCL} is the operation start-up current of IC

$V_{CC(START)}$ is the operation start-up voltage of IC

$V_{CC(STOP)}$ is the operation stop voltage of IC

V_F is the forward voltage of rectifier diode

$V'_{IN\ (P\text{-}P)}$ is the peak to peak ripple voltage of

V_{CC} terminal $\simeq \frac{N_B}{N_P} V_{IN\ RIP(P\text{-}P)}$

It is required that the $V_{IN\,(START)}$ must be higher than $V_{IN\,(STOP)}$.

When the third winding is the "fly back winding" or "reverse polarity", the $V_{IN(START)}$ can be fixed, however, $V_{IN(STOP)}$ can not be settled by this system, so the auxiliary circuit is required.

(3)Notice to the V_{CC}, V_{CC} line and GND line

To avoid the abnormal IC operation, it is recommended to design the V_{CC} is not vary abruptly and has few spike voltage, which is induced from the stray capacity between the winding of main transformer.

To reduce the spike voltage, the C_{VCC}, which is connected between V_{CC} and ground, must have the good high frequency characteristics.

To design the conductor-pattern on PC board, following cautions must be considered as shown in Fig. 19.

(a) To separate the emitter line of type M51978 from the the GND line of the IC

(b) To locate the C_{VCC} as near as possible to type M51978 and connect directly

(c) To separate the collector line of type M51978 from the V_{CC} line of the IC

(d) To connect the ground terminals of peripheral parts of ICs to GND of type M51978 as short as possible

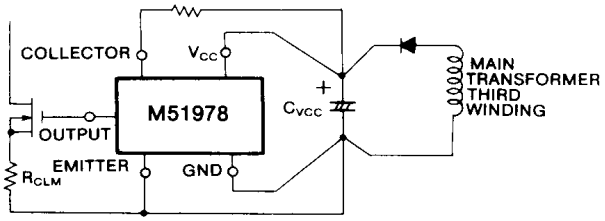


Fig. 19 How to design the conductor-pattern of type M51978 on PC board (schematic example)

(4)Power supply circuit for easy start-up

When IC start to operate, the voltage of the C_{VCC} begins to decrease till the C_{VCC} becomes to be charged from the third winding of main-transformer as the I_{CC} of the IC increases abruptly. In case shown in Fig. 17 and 18, some "unstable start-up" or "fail to start-up" may happen, as the charging interval of C_{VCC} is very short duration; that is the charging does occur only the duration while the induced winding voltage is higher than the C_{VCC} voltage, if the induced winding voltage is nearly equal to the "operation-stop voltage" of type M51978.

In this case the circuit shown in Fig. 27 is recommended.

It is recommended to use the 10 to 47μF for C_{VCC1}, and about 5 times capacity bigger than C_{VCC1} for C_{VCC2}.

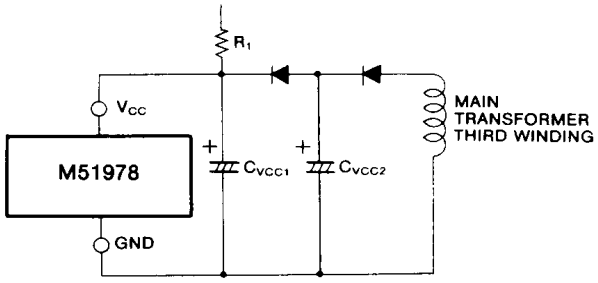


Fig. 20 DC source circuit for stable start-up

OVP circuit

(1)To avoid the miss-operation of OVP

It is recommended to connect the resistor of 12kΩ and capacitor between OVP terminal and GND, and also resistor of 10kΩ in series to the photo-coupler as the input impedance of OVP terminal is very high and the pulsive-displacement-current inclines to make the IC miss-operation when V_{CC} is changed abruptly.

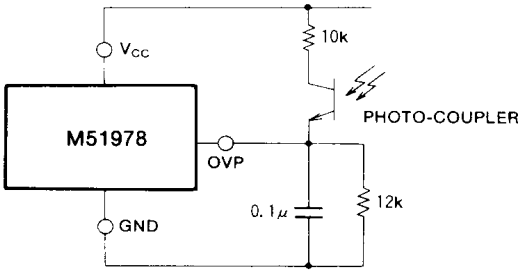


Fig. 21 Peripheral circuit of OVP terminal

(2)Application circuit to make the OVP-reset time fast

The reset time may becomes problem when the discharge time constant of $C_{FIN} \cdot (R_1+R_2)$ is long. Under such the circuit condition, it is recommended to discharge the C_{VCC} forcedly and to make the V_{CC} low value; This makes the OVP-reset time fast.

Similar circuit is used to make the V_{CC} low, when the reset of OVP is done by the external signal.

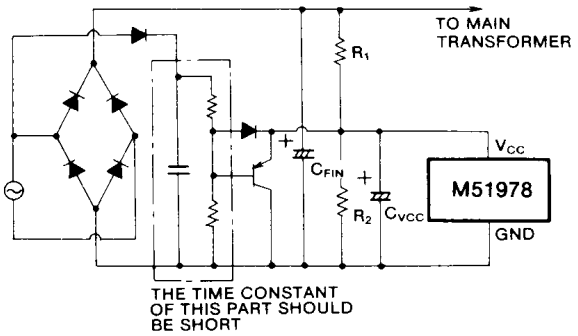


Fig. 22 Example circuit diagram to make the OVP-reset-time fast

(3)OVP setting method using the induced third winding voltage on fly back system

For the over voltage protection (OVP), the induced fly back type third winding voltage can be utilized, as the induced third winding voltage depends on the output voltage. Fig. 23 shows one of the example circuit diagram.

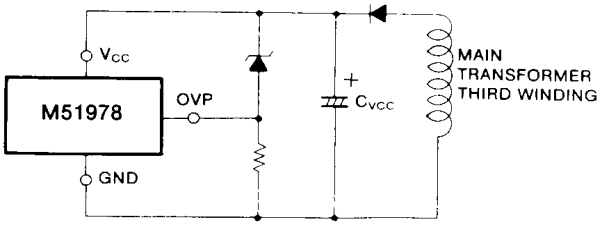


Fig. 23 OVP setting method using the induced third winding voltage on fly back system

Current limitting circuit

(1)Peripheral circuit of CLM + terminal

Fig.24 shows the example circuit diagrams around the CLM + terminal. It is required to connect the low pass filter, in oder to reduce the spike current component, as the main current or drain current contains the spike current especially during the turn-on duration of MOS-FET.

1,000pF to 22,000pF is recommended for C_{NF} and the R_{NF1} and R_{NF2} have the functions both to adjust the "current-detecting-sensitivity" and to consist the low pass filter.

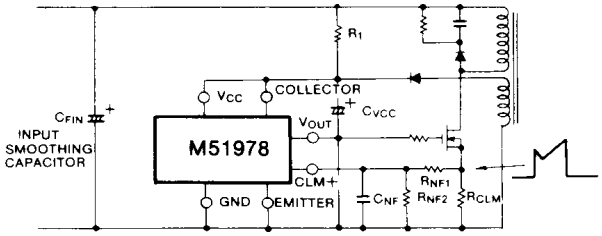


Fig. 24 Peripheral circuit diagram of CLM + terminal

To design the R_{NF1} and R_{NF2}, it is required to consider the influence of CLM + terminal source current (I_{INCLM+}), which value is in the range of 90 to 270μA.

In order to be not influenced from these resistor paralleled value of R_{NF1} and R_{NF2}, ($R_{NF1}//R_{NF2}$) is recommended to be less than 100Ω.

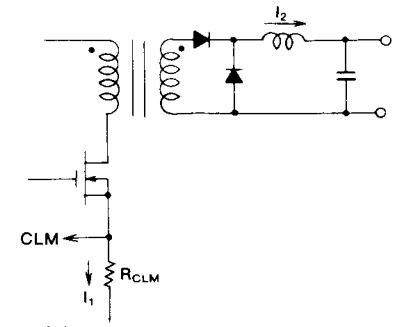
The R_{CLM} should be the non-inductive resistor.

(2)Over current limitting curve

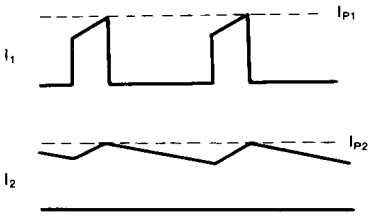
(a) In case of feed forward system

Fig. 25 shows the primary and secondary current waveforms under the current limitting operation.

At the typical application of pulse by pulse primary current detecting circuit, the secondary current depends on the primary current. As the peak value of secondary current is limitted to specified value, the characteristics curve of output voltage versus output current become to the one as shown in Fig. 26.



(a) Feed forward system



(b) Primary and secondary current

Fig. 25 Primary and secondary current waveforms under the current limitting operation condition on feed forward system

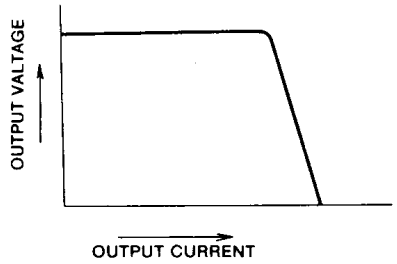


Fig. 26 Over current limitting curve on feed forward system

The demerit of the pulse by pulse current limitting system is that the output pulse width can not reduce to less than some value because of the delay time of low pass filter connected to the CLM+ terminal and propagation delay time T_{PDCLM+} from CLM+ terminal to output terminal of type M51978. The typical T_{PDCLM+} is 150ns.

As the frequency becomes higher, the delay time must be shorter. And as the secondary output voltage becomes higher, the dynamic range of on-duty must be wider; it means that it is required to make the on-duration much more narrower. So this system has the demerit at the higher oscillating frequency and higher output voltage applications.

To prevent that, the SOFT terminal is used to lower the frequency when the curve starts to become vertical.

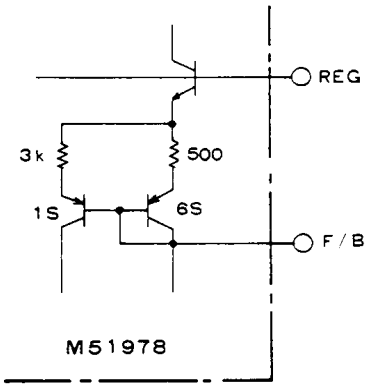


Fig. 27 Relationship between REG terminal and F/B terminal

If the curve becomes vertical because of an over current, the output voltage is lowered and no feedback current flows from feedback photo-coupler; the PWM comparator operates to enlarge the duty sufficiently, but the signal from the CLM+ section operates to make the pulse width narrower.

Under the condition in which I_2 in Fig. 25 does not become 0, the output voltage is proportional to the product of the input voltage V_{IN} (primary side voltage of the main transformer) and on duty. If the bias winding is positive, V_{CC} is approximately proportional to V_{IN} and the smoothed output voltage of the IC is proportional to V_{IN}. The existence of feed back current of the photo-coupler is known by measuring the F/B terminal voltage which becomes less than $2V_{BE}$ in the internal circuit of REG terminal and F/B terminal if the output current flows from the F/B terminal.

Fig. 28 shows an application example.

Q_1 is turned on when normal output voltage is controlled at a certain value. The SOFT terminal is clamped to a high-level voltage. If the output voltage decreases and the curve starts to drop, no feed back current flows, Q_1 is turned off and the SOFT terminal responds to the smoothed output voltage.

It is recommended to use an R_1 and R_2 of 10kΩ~30kΩ. An R_3 of 20~100kΩ and C of 1000pF~8200pF should be used.

To change the knee point of frequency drop, use the circuit in Fig. 29.

To have a normal SOFT start function in the circuit in Fig. 28, use the circuit in Fig. 30. It is recommended to use an R_4 of 10kΩ.

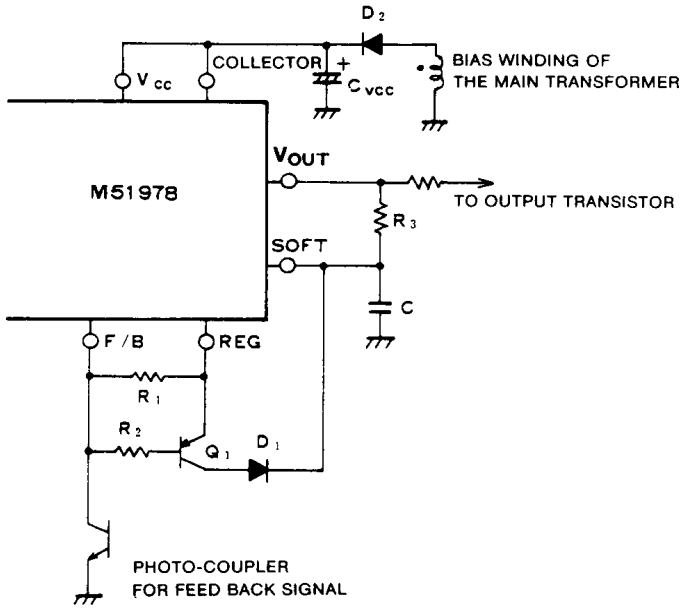


Fig. 28 Circuit to lower frequency during over current

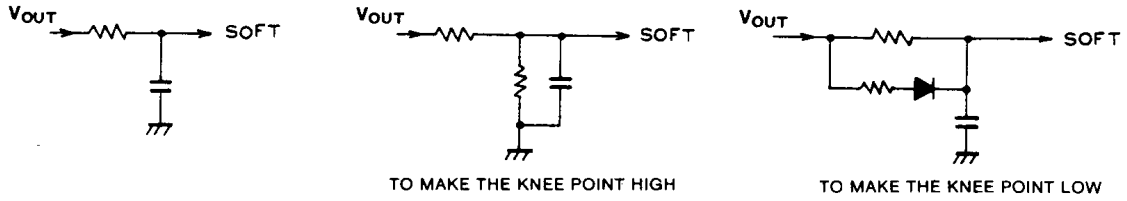


Fig. 29 Method to control the knee point of frequency drop

(b)In case of fly back system

The DC output voltage of SMPS depends on the V_{CC} voltage of type M51978 when the polarity of the third winding is negative and the system is fly back. So the operation of type M51978 will stop when the V_{CC} becomes lower than "Operation-stop voltage" of M51978 when the DC output voltage of SMPS decreases under specified value at over load condition.

However, the M51978 will non-operate and operate intermittently, as the V_{CC} voltage rises in accordance with the decrease of I_{CC} current.

The fly back system has the constant output power characteristics as shown in Fig. 31 when the peak primary current and the operating frequency are constant.

To avoid an increase of the output current, the frequency is lowered using the SOFT terminal when the DC output voltage of SMPS starts to drop. V_{CC} is divided and is input to the SOFT terminal as shown in Fig. 32, because the voltage in proportional to the output voltage is obtained from the bias winding. In this application example, the current flowing to R_3 is added to the start-up current. So please use high resistance or 100kΩ~200kΩ for R_3.

The start-up current is not affected by R_3 if R_3 is connected to C_{VCC2} in the circuit shown in Fig. 20.

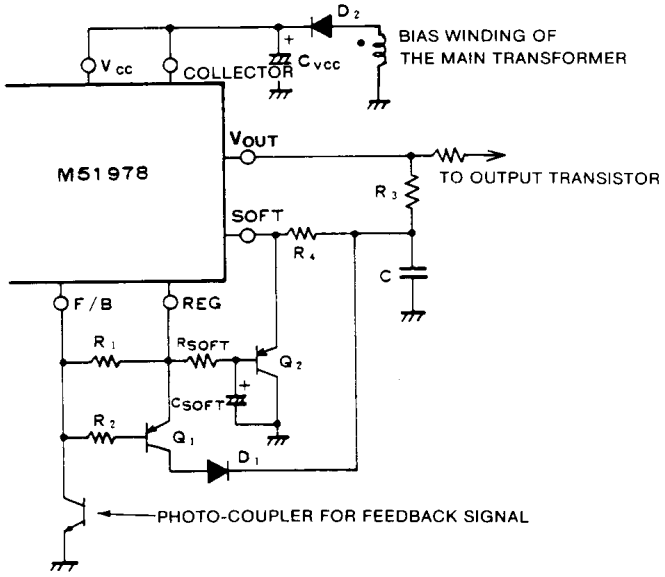


Fig. 30 Circuit to use frequency drop during the over current and normal soft start

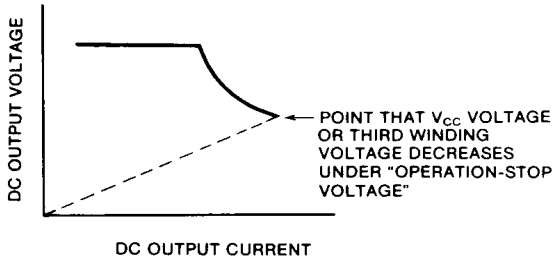


Fig. 31 Over current limitting curve on fly back system

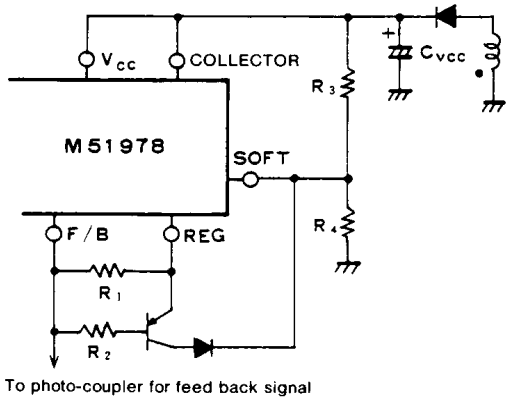


Fig. 32 Circuit to lower the frequency during the over current in the fly back system

Output circuit

(1)The output terminal characteristics at the V_{CC} voltage lower than the "Operation-stop" voltage

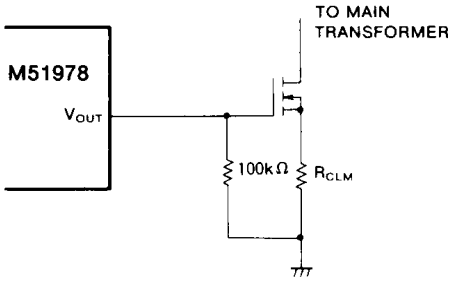


Fig. 33 Circuit diagram to prevent the MOS-FET gate potential rising

The output terminal has the current sink ability even though the V_{CC} voltage lower than the "Operation-stop" voltage or $V_{CC(STOP)}$. (It means that the terminal is "Output low state" and please refer characteristics of output low voltage versus sink current.)

This characteristics has the merit not to damage the MOS-FET at the stop of operation when the V_{CC} voltage decreases lower than the voltage of $V_{CC(STOP)}$, as the gate charge of MOS-FET, which shows the capacitive load characteristics to the output terminal, is drawn out rapidly.

The output terminal has the draw-out ability above the V_{CC} voltage of 2V, however, lower than the 2V, it loses the ability and the output terminal potential may rise due to the leakage current.
In this case, it is recommended to connect the resistor of 100kΩ between gate and source of MOS-FET as shown in Fig. 33.

(2)MOS-FET gate drive power dissipation

Fig. 34 shows the relation between the applied gate voltage and the stored gate charge.
In the region ①, the charge is mainly stored at C_{GS} as the depletion is spread and C_{GD} is small owing to the off-state of MOS-FET and the high drain votage.
In the region ②, the C_{GD} is multiplied by the "mirror effect" as the characteristics of MOS-FET transfers from off-state to on-state.
In the region ③, both the C_{GD} and C_{GS} affect to the characteristics as the MOS-FET is on-state and the drain voltage is low.
The charging and discharging current caused by this gate charge makes the gate power dissipation. The relation between gate drive current I_D and total gate charge Q_{GSH} is shown by following equation;

$$I_D = Q_{GSH} \cdot f_{OSC} \quad \cdots\cdots (9)$$

Where

f_{OSC} is switching frequency

As the gate drive current may reach up to several tenths milliampere at 500kHz operation, depending on the size of MOS-FET, the power dissipation caused by the gate current can not be neglected.

In this case, following action will be considered to avoid heat up of type M51978.

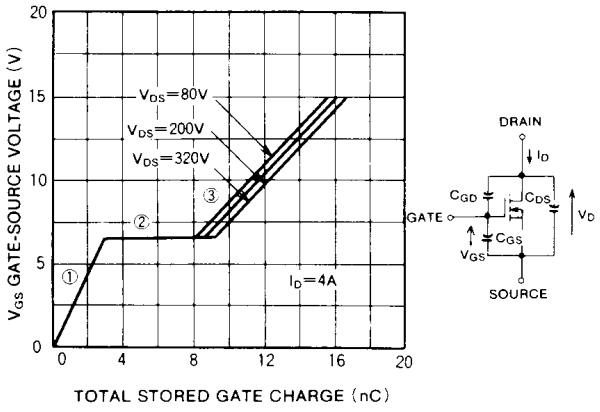


Fig. 34 The relation between applied gate-source voltage and stored gate charge

(1) To attach the heatsink to type M51978
(2) To use the printed circuit board with the good thermal conductivity
(3) To use the buffer circuit shown next section

(3)Output buffer circuit

It is recommended to use the output buffer circuit as shown in Fig. 35, when type M51978 drives the large capacitive load or bipolar transistor.

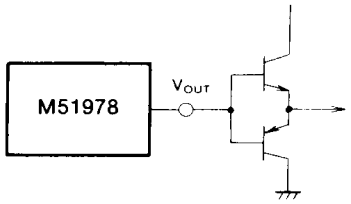


Fig. 35 Output buffer circuit diagram

DET

Fig. 36 shows how to use the DET circuit for the voltage detector and error amplifier.
For the phase shift compensation, it is recommended to connected the CR network between DET terminal and F/B terminal.

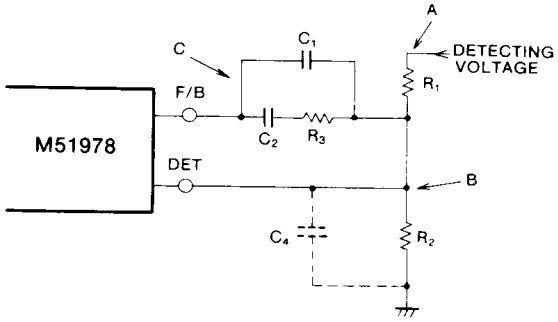


Fig. 36 How to use the DET circuit for the voltage detector

Fig. 37 shows the gain-frequency characteristics between point B and point C shown in Fig. 36.
The G_1, ω_1 and ω_2 are given by following euqations;

$$G_1 = \frac{R_3}{R_1 // R_2} \quad \cdots\cdots (10)$$

$$\omega_1 = \frac{1}{C_2 \cdot R_3} \quad \cdots\cdots (11)$$

$$\omega_2 = \frac{C_1 + C_2}{C_1 \cdot C_2 \cdot R_3} \quad \cdots\cdots (12)$$

At the start of the operation, there happen to be no output pulse due to F/B terminal current through C_1 and C_2, as the potential of F/B terminal rises sharply just after the start of the operation.
Not to lack the output pulse, is recommended to connect the capacitor C_4 as shown by broken line.
Please take notice that the current flows through the R_1 and R_2 are superposed to $I_{CC\,(START)}$. Not to superpose, R_1 is connected to C_{VCC2} as shown in Fig. 20

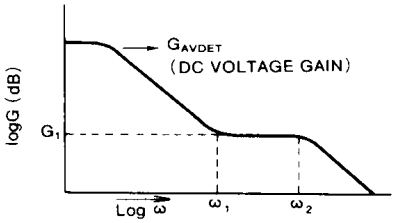


Fig. 37 Gain-frequency characteristics between point B and C shown in Fig. 36

How to get the narrow pulse width during the start of operation

Fig. 38 shows how to get the narrow pulse width during the start of the operation. If the pulse train of forcedly narrowed pulse-width continues too long, the misstart of operation may happen, so it is recommended to make the output pulse width narrow only for a few pulse at the start of operation 0.1μF is recommended for the C.

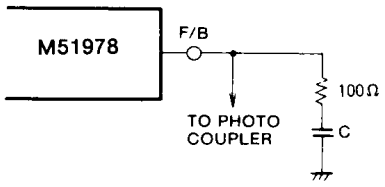


Fig. 38 How to get the narrow pulse width during the start of operation

How to synchronize with external circuit

Type M51978 has no function to synchronize with external circuit, however, there is some application circuit for synchronization as shown in Fig. 39.

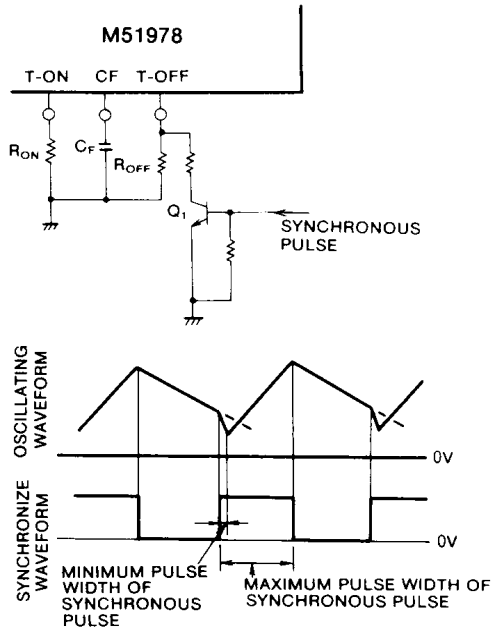


Fig. 39 How to synchronize with external circuit

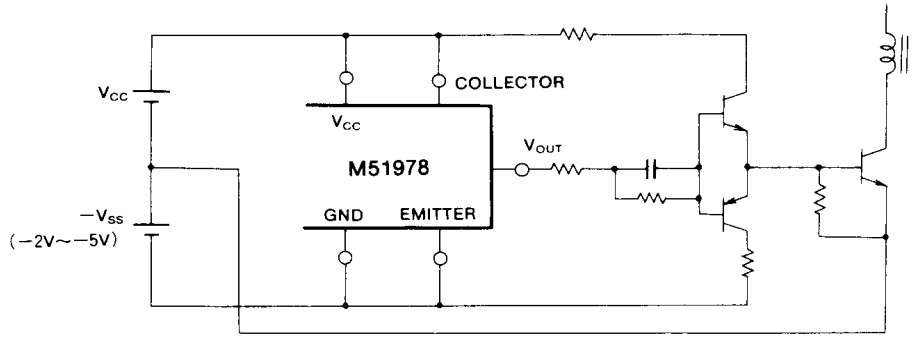


Fig. 40 Driver circuit diagram (1) for bipolar transistor

Driver circuit for bipolar transistor

When the bipolar transistor is used instead of MOS-FET, the base current of bipolar transistor must be sinked by the negative base voltage source for the switching-off duration, in order to make the switching speed of bipolar transistor fast one.

In this case, over current can not be detected by detecting resistor in series to bipolar transistor, so it is recommended to use the CT(current transformer).

For the low current rating transistor, type M51978 can drive it directly as shown in Fig. 41.

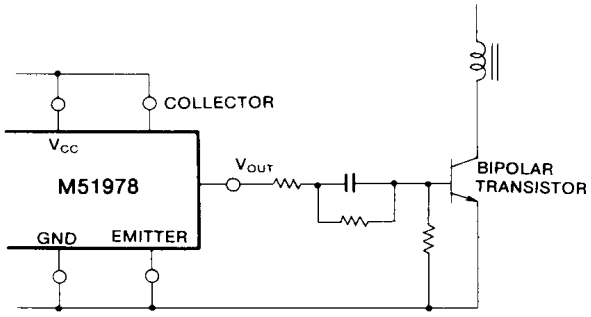


Fig. 41 Driver circuit diagram
(2) for small bipolar transistor

Attention for heat generation

The maximum ambient temperature of type M51978 is + 85°C, however, the ambient temperature in vicinity of the IC is not uniform and varies place by place, as the amount of power dissipation is fearly large and the power dissipation is generated locally in the switching regulator.

So it is one of the good idea to check the IC package temperature. The temperature difference between IC junction and the surface of IC package is 15°C or less, when the IC junction temperature is measured by temperature dependency of forward voltage of pn junction, and IC package temperature is measured by "thermo-viewer", and also the IC is mounted on the "phenol-base" PC board in normal atmosphere.

So it is concluded that the maximum case temperature (surface temperature of IC) rating is 120°C with adequate margin. It is noticed that the minimum thermal protection operating temperature is 120°C.