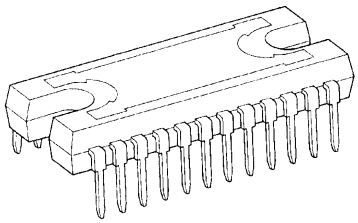
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA8411L

STEPPING MOTOR SYSTEM DRIVER

The TA8411L is Stepping Motor System Driver IC incorporates Dual Bipolar Stepping Motor Drivers, DC Motor Driver and Serial to Parallel Signal Conversion Circuit (12 bit Serial to Parallel Shift Resistor with Latch) which control the 3 Output Drivers states by means of Input Serial Signal trains.



HDIP24-P500-2.00

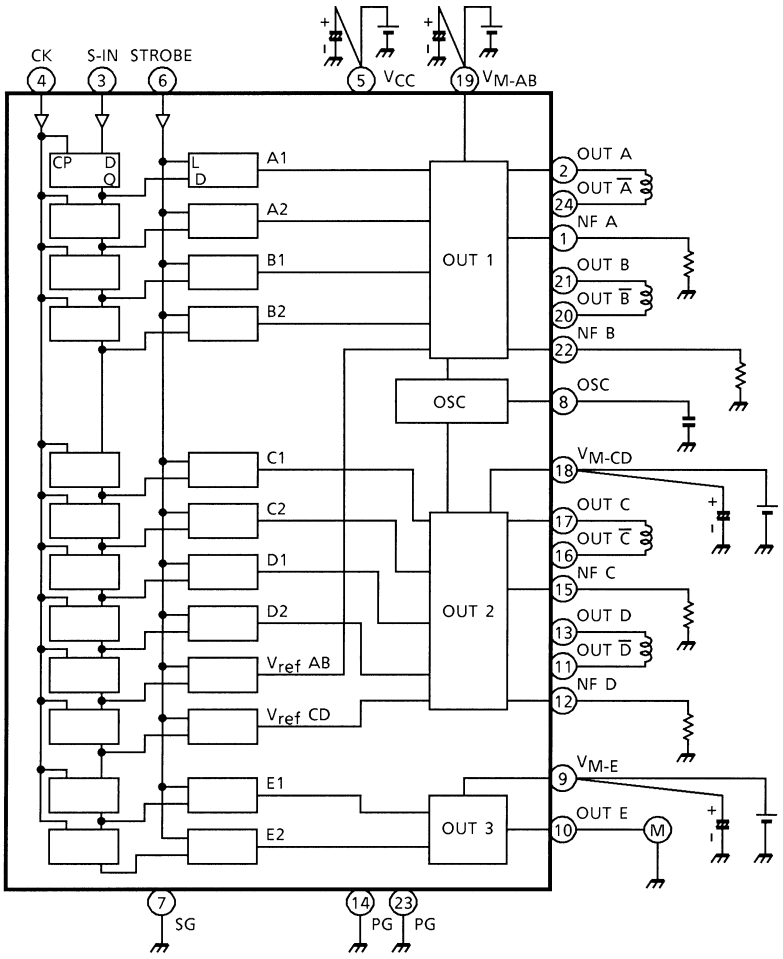
Weight: 4.30 g (Typ.)

FEATURES

- 2 Bipolar Stepping Motors and 1 Brush DC Motor (or Solenoid) are controlled by input serial signal trains and latch signals.
- Output Current up to 0.8 A (for Stepper) and 0.6 A (for DC Motor).
- PWM Chopper type Stepping Motor Drivers.
- All C−MOS Compatible Inputs.
- Operating Supply Voltage: $V_{M1, 2}$ = 0~27 V
  V_{CC} = 4.5~5.5 V

961001EBA1

BLOCK DIAGRAM



Note 1: Capacitance connect to each Power Supply Terminal is required to change to optimum value for noise elimination and also required to connect directly to each Power Supply Terminal (V_{CC}, $V_{M1, 2}$) and the corresponding GND Terminal (See Table 1) for stable operations.

Table 1

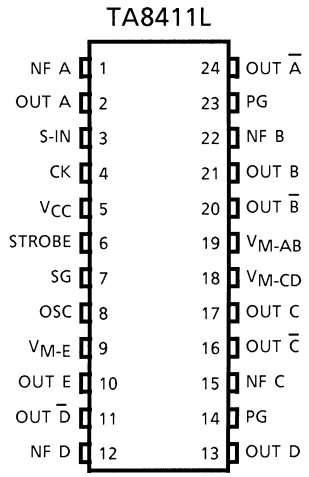
GND	POWER SUPPLY
Pin (7) (SG)	Pin (5) (V_{CC})
Pin (23) (PG)	Pin (19) (V_{M-AB})
Pin (14) (PG)	Pin (18) (V_{M-CD}), Pin (9) (V_{M-E})

Note 2: Heat Fin is connect to GND terminal with Low Impedance.

PIN FUNCTION

PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION
1	NF A	A channel current detection output terminal.
2	OUT A	OUTPUT A
3	S−IN	Serial signal input terminal.
4	CK	Clock signal input terminal.
5	V_{CC}	Supply voltage terminal for control circuit.
6	STROBE	STROBE signal input terminal.
7	SG	Signal GND terminal.
8	OSC	Internal osc frequency setting terminal.
9	V_{M-E}	E channel power supply input terminal.
10	OUT E	E channel output terminal. (pushpull output)
11	OUT $\overline{D}$	OUTPUT $\overline{D}$
12	NF D	D channel current detection output terminal.
13	OUT D	OUTPUT D
14	PG	Power GND terminal.
15	NF C	C channel current detection output terminal.
16	OUT $\overline{C}$	OUTPUT $\overline{C}$
17	OUT C	OUTPUT C
18	V_{M-CD}	Supply voltage terminal for C channel D channel.
19	V_{M-AB}	Supply voltage terminal for A channel B channel.
20	OUT $\overline{B}$	OUTPUT $\overline{B}$
21	OUT B	OUTPUT B
22	NF B	B channel current detection output terminal.
23	PG	Power GND terminal.
24	OUT $\overline{A}$	OUTPUT $\overline{A}$

PIN CONNECTION



INPUT SERIAL PULSE TRAIN (PIN (3)) AND POWER OUTPUT STATES

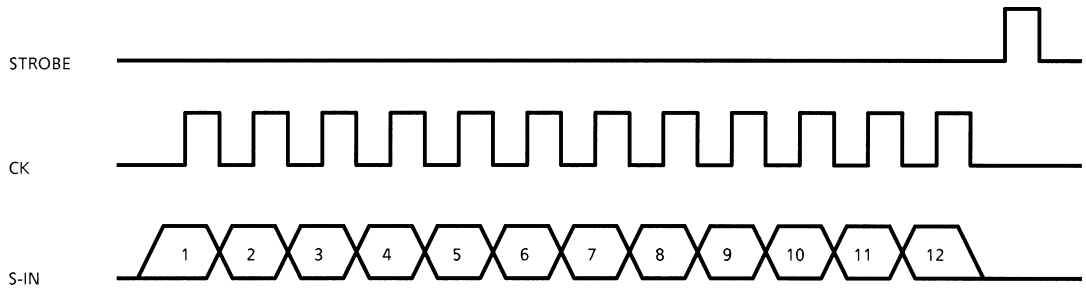
SERIAL INPUT SIGNAL TRAIN			CONTROL	OPERATION
↑	1	E2	DC Motor Control	See table below
	2	E1		
	3	V_{ref} CD	Stepping Motor 2 Chopping Rate Control (V_{ref} CD)	V_{ref} = 0.7 V Typ. (at "H" Mode) = 0.55 V Typ. (at "L" Mode)
	4	V_{ref} AB	Stepping Motor 1 Chopping Rate Control (V_{ref} AB)	
	5	D2	Stepping Motor 2 Control (OUT C, D)	See table below
	6	D1		
	7	C2		
	8	C1		
	9	B2	Stepping Motor 1 Control (OUT A, B)	B1, B2 → B, $\overline{B}$ C1, C2 → C, $\overline{C}$ D1, D2 → D, $\overline{D}$ are all the same.
	10	B1		
	11	A2		
	12	A1		

INPUT		OUTPUT	MODE
E1	E2	E	
L	L	∞	STOP
H	L	H	CW / CCW
L	H	L	Brake
H	H	∞	STOP

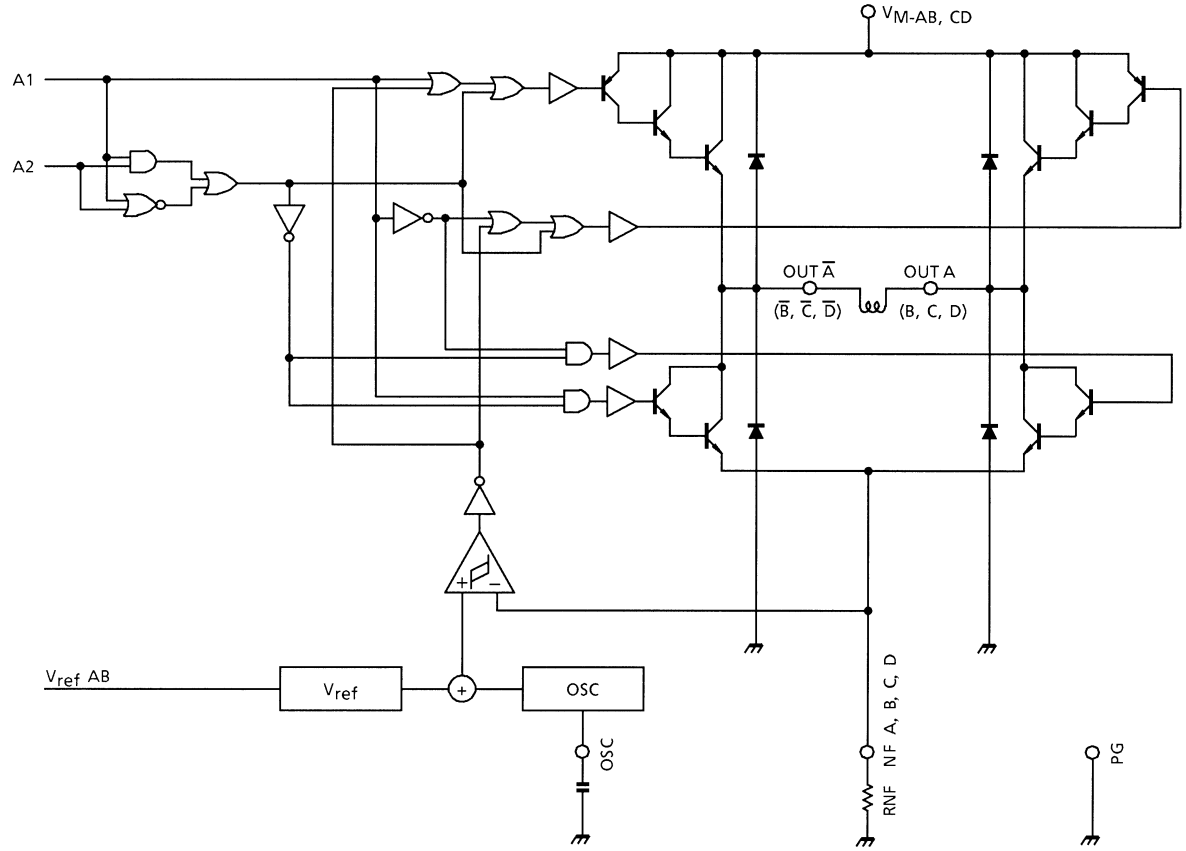
INPUT		OUTPUT		MODE
A1	A2	A	$\overline{A}$	
L	L	∞	∞	STOP
H	L	H	L	CW / CCW
L	H	L	H	CCW / CW
H	H	∞	∞	STOP

∞: High impedance

INPUT SERIAL PULSE TRAIN TIMING CHART



OUTPUT STAGE 1, 2 1 / 2 CIRCUIT



FUNCTION (Comp.$^{+}$ > Comp.$^{-}$)

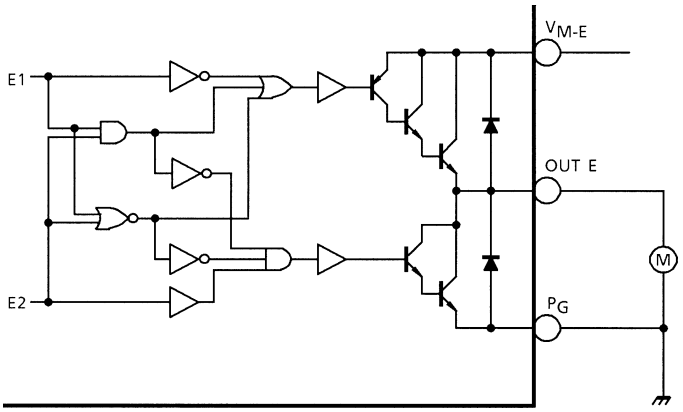
A1	A2	A	$\overline{A}$	MODE
L	L	∞	∞	STOP
H	L	H	L	CW / CCW
L	H	L	H	CCW / CW
H	H	∞	∞	STOP

∞: High impedance

Note 1: In case of Comp.$^{+}$ < Comp.$^{-}$, Upper side Power Transistor turned off.

Note 2: Free wheeling diode connects between Output A terminal and GND is required for stable operations. And also recommend to connect free wheeling diodes other Output terminals for reliable operations.

OUTPUT STAGE 3

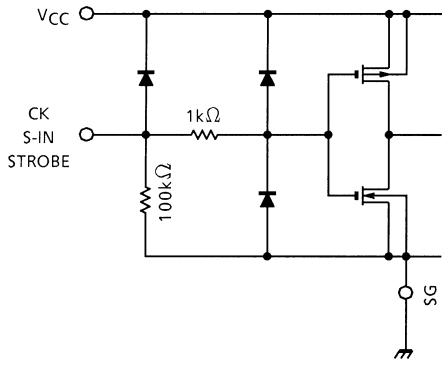


FUNCTION

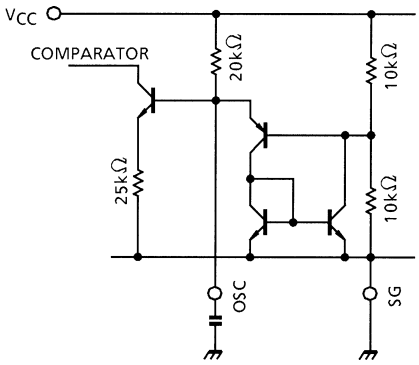
E1	E2	E	MODE
L	L	∞	STOP
H	L	H	CW
L	H	L	BRAKE
H	H	∞	STOP

∞: High impedance

INPUT STAGE (CK, S−IN, STROBE)



OSC STAGE (OSC)



$$f_{OSC} = \frac{1}{21.4C_{OSC}} \langle kHz \rangle$$

C_{OCS} : μF

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage (Motor)	V_M	30	V
Supply Voltage (Control)	V_{CC}	5.5	V
Input Voltage	V_{IN}	5.5	V
Output Current	I_{O1}, I_{O2}	0.8	A
	I_{O3}	0.6	
Power Dissipation	P_D	16.2 (Note 1)	W
		2.5 (Note 2)	
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−55~150	°C

Note 1: Tc = 85°C
Note 2: No heat sink

RECOMMENDED OPERATION CONDITION

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage (Control)		V_{CC}	—	4.5	5.0	5.5	V
Supply Voltage (Motor)		V_M	—	21.6	24	26.4	V
Input Voltage		V_{IN}	—	0	—	V_{CC}	V
Output Current	I_{OUT} A, B, C, D	I_{OUT}	Ta = 0~70°C V_{CC} = 5 V V_M = 24 V	—	—	0.7	A
	I_{OUT} E			—	—	0.4	
Clock Frequency		f_{CK}		—	—	1.0	MHz
		f_{STROBE}		—	—	1.0	
Clock Pulse Width		$t_{w\,CK}$		500	—	—	ns
		$t_{w\,STROBE}$		500	—	—	
Data Set Up Time		t_{su}		250	—	—	ns
Data Hold Time		t_H		250	—	—	ns
PWM Oscillation Frequency		f_{PWM}		20	—	100	kHz

ELECTRICAL CHARACTERISTICS

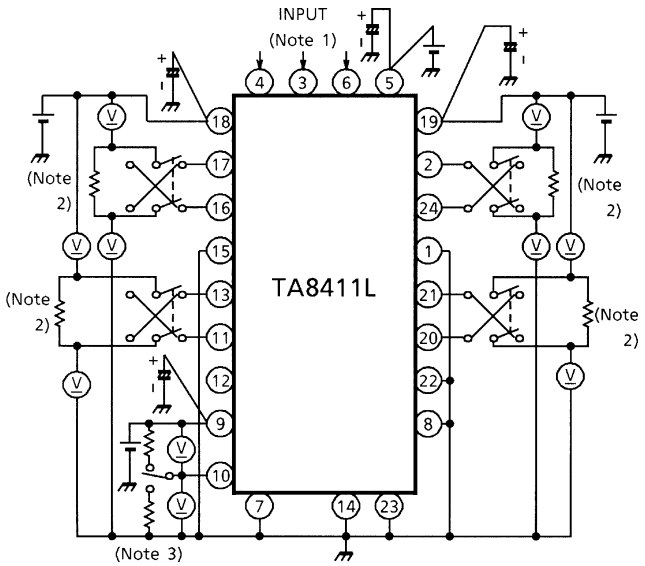
Output stage (Ta = 25°C, V_{CC} = 5 V, V_M = 24 V)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
Operation Power Supply Voltagege		$V_{M\,(opr)}$	—	—		0	—	27	V
Saturation Voltage	AB DC	$V_{CE\,(SAT)}$ Upper	1	I_{OUT} = 0.7 A	Output − V_{CC}	—	2.0	2.5	V
				I_{OUT} = 0.5 A		—	1.8	2.3	
	AB CD	$V_{CE\,(SAT)}$ Lower	1	I_{OUT} = 0.7 A	Output − NF	—	1.5	2.0	
				I_{OUT} = 0.5 A		—	1.3	1.8	
	E	$V_{CE\,(SAT)}$ Upper	1	I_{OUT} = 0.5 A	Output − V_{CC}	—	1.8	2.3	
				I_{OUT} = 0.3 A		—	1.7	2.2	
	E	$V_{CE\,(SAT)}$ Lower	1	I_{OUT} = 0.5 A	Output − NF	—	1.5	2.0	
				I_{OUT} = 0.3 A		—	1.2	1.7	
Output Leak Current		I_{OL-H}	2	V_{CE} = 30 V		—	—	50	μA
		I_{OL-L}				—	—	50	
Clamp Diode Forward Voltage	AB CD	V_{F-U}	3	I_F = 700 mA	Output A~D	—	1.6	2.0	V
		V_{F-L}				—	1.6	2.0	
	E	V_{F-U}	3	I_F = 500 mA	Output E	—	1.5	1.9	
		V_{F-L}				—	1.7	2.1	
Propagation Delay Time (ST−OUT)		t_P	7	—		—	600	—	ns

Small signal stage (Ta = 25°C, V_{CC} = 5 V, V_M = 24 V)

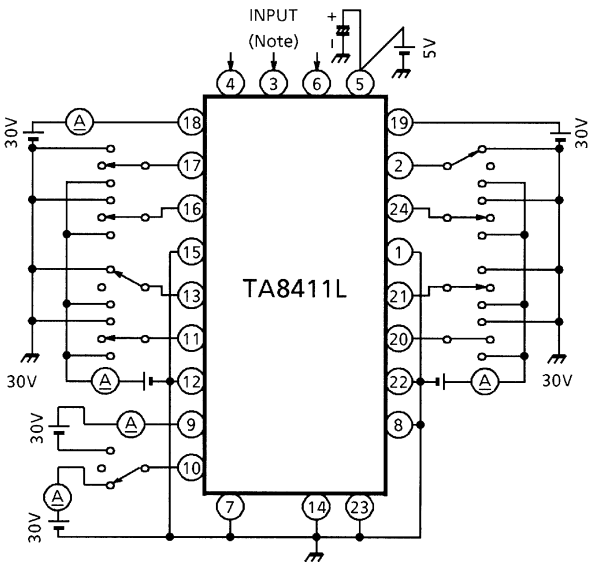
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
Operating Supply Voltage		$V_{(opr)}$	—	—		4.5	—	5.5	V
Quiescent Current		I_{CC1}	4	V_{CC} = 5 V Output Open	Output off mode	—	26.0	40	mA
		I_{CC2}			Output on mode: output stage 1 or 2	—	26.0	40	
		I_{CC3}			Output on mode: output stage 1 and 2	—	24.0	37	
		I_{CC4}			Output on mode: output stage 3	—	25.0	38	
Input Voltage	"H" Level	$V_{IN\,H}$	—	V_{CC} = 5.0 V	CK, S−IN STROBE	3.5	—	V_{CC}	V
	"L" Level	$V_{IN\,L}$				−0.4	—	1.5	
Input Current	"H" Level	$I_{IN\,H}$	5	V_{CC} = 5.0 V	$V_{IN\,H}$ = 5.5V	—	55	150	μA
					$V_{IN\,H}$ = 3.5V	—	35	100	
	"L" Level	$I_{IN\,L}$			$V_{IN\,L}$ = 1.5V	—	15	50	
V_{ref}	"H" Level	$V_{ref\,H}$	6	Tj = − 40~125°C C_{OSC} = 3300 pF R_{NF} = 3.3 Ω L = 19.5 mH	$V_{ref\,IN}$ = "H"	0.6	0.7	0.8	V
	"L" Level	$V_{ref\,L}$			$V_{ref\,IN}$ = "L"	0.45	0.55	0.65	
V_{ref} Level Differential Voltage		ΔV_{ref}	6	$V_{ref\,(H)}$ − $V_{ref\,(L)}$		—	0.15	—	V
Reset Voltage		V_{CCR}	—	—		3.4	3.9	4.4	V
PWM Oscillation Frequency		f_{PWM}	—	—		10	—	200	kHz
Clock Frequency		f_{CK}	7	—		—	—	1.5	MHz
		f_{STROBE}	7	—		—	—	1.5	
Min. Clock Width		t_{CK}	7	—		340	—	—	ns
		t_{STROBE}	7	—		340	—	—	
Data Set Up Time		t_{SU}	7	—		170	—	—	ns
Data Hold Up Time		t_H	7	—		170	—	—	ns

TEST CIRCUIT 1. $V_{CE\ (SAT)}$ Upper, Lower



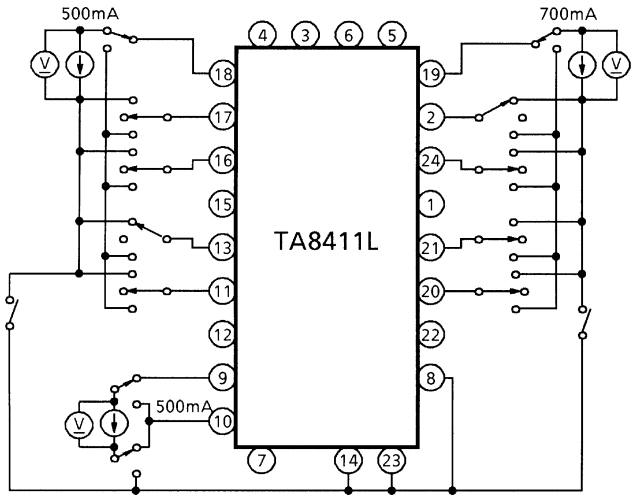
Note 1: Sets Output Transistor active with Input mode select.
Note 2: Calibrate Output Current becomes 0.5 A (or 0.7A) with this resistor.
Note 3: Calibrate Output Current becomes 0.3 A (or 0.5A) with this resistor.

TEST CIRCUIT 2. I_{OL-H}, I_{OL-L}



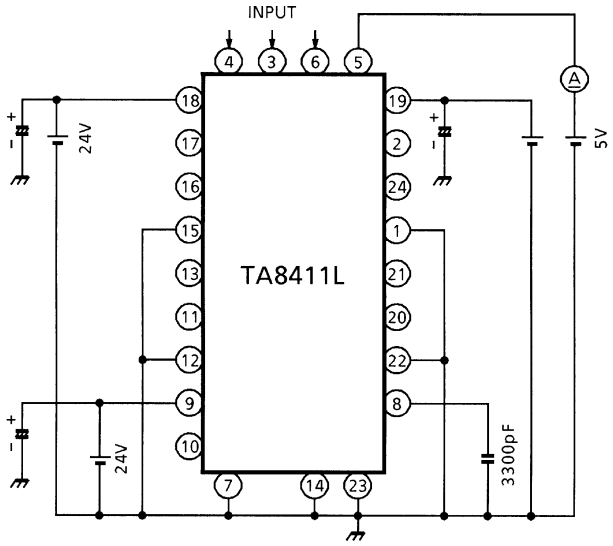
Note: All "L" level S−IN signal, normal CK and Strobe signals are required to measure.

TEST CIRCUIT 3. V_{F-U}, V_{F-L}

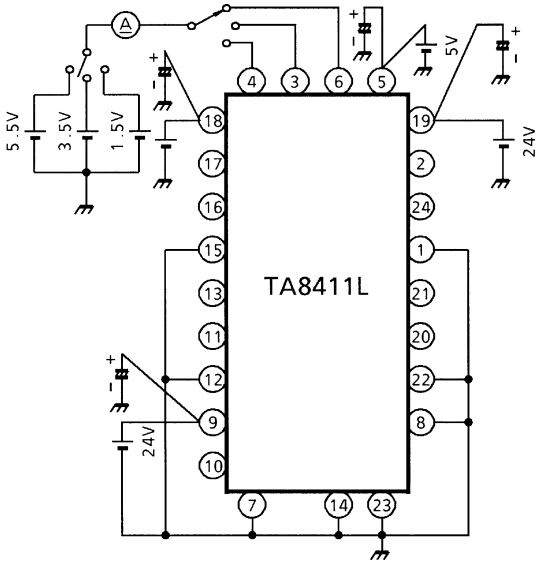


Note: Not to take a GND with any non−connecting Pins.

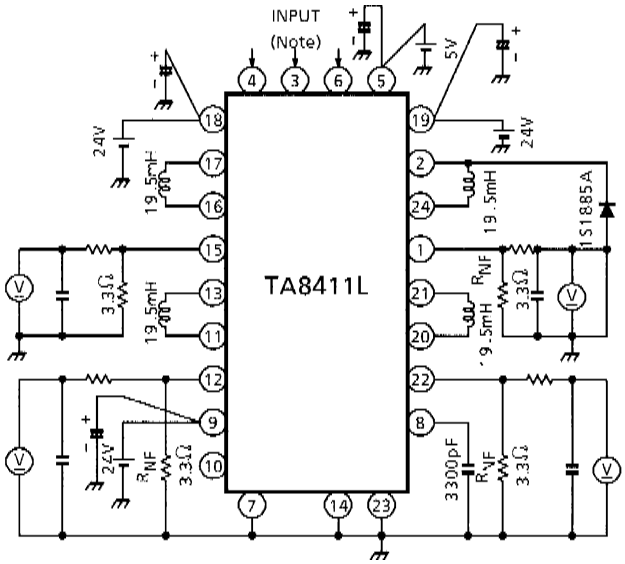
TEST CIRCUIT 4. $I_{CC1, 2, 3, 4}$



TEST CIRCUIT 5. I_{INH}, I_{INL}



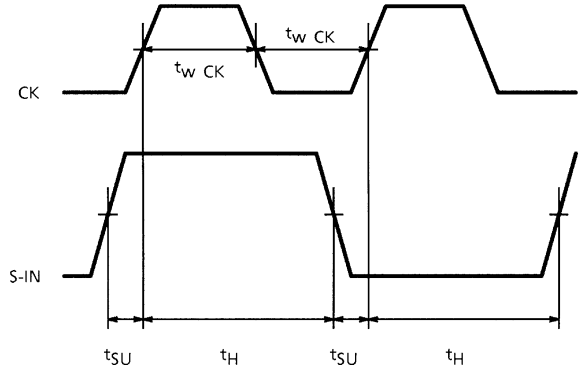
TEST CIRCUIT 6. V_{ref-H}, V_{ref-L}, ΔV_{ref}



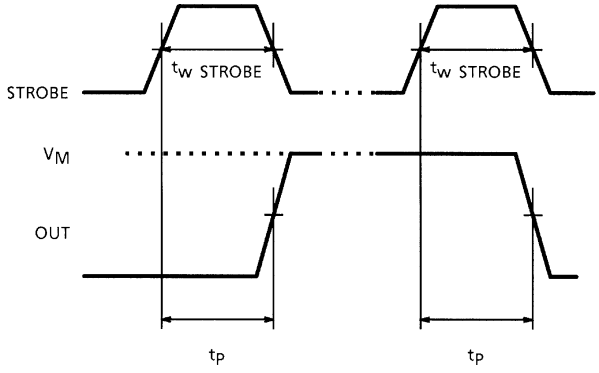
Note: Hold the state (2 Phase excitation mode) and measure.

AC ELECTRICAL CHARACTERISTIC MEASUREMENT WAVEFORM

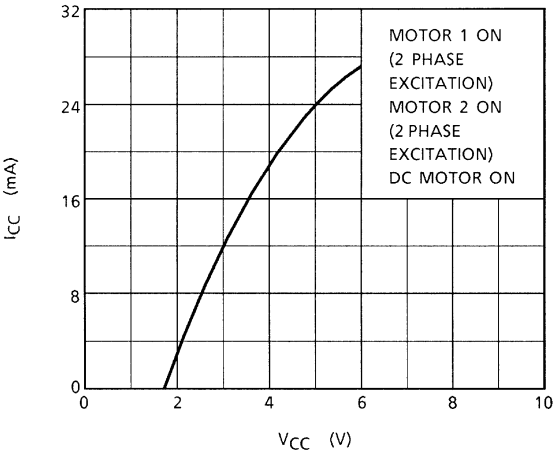
7-1 CK-S-IN



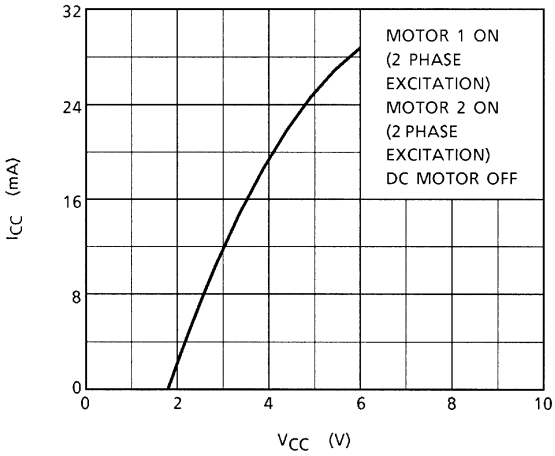
7-2 STROBE-OUT



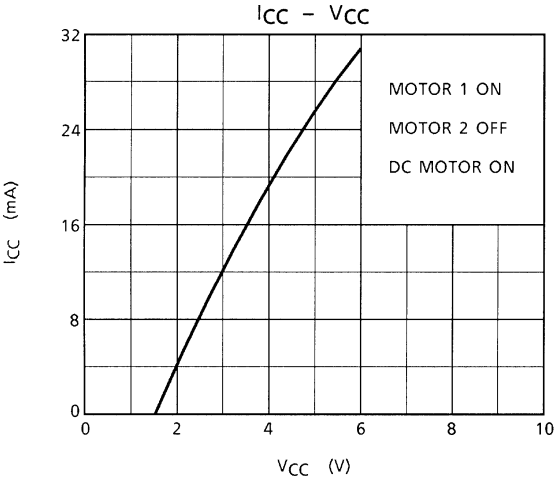
I_{CC} – V_{CC}



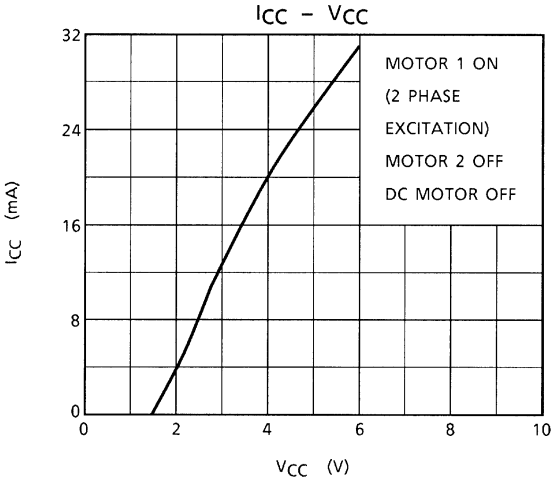
I_{CC} – V_{CC}



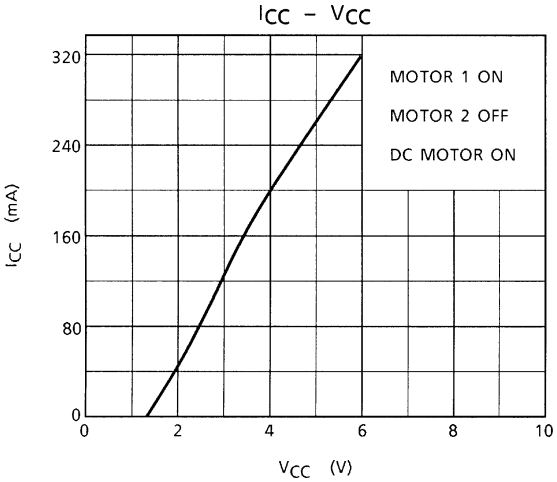
I_{CC} – V_{CC}



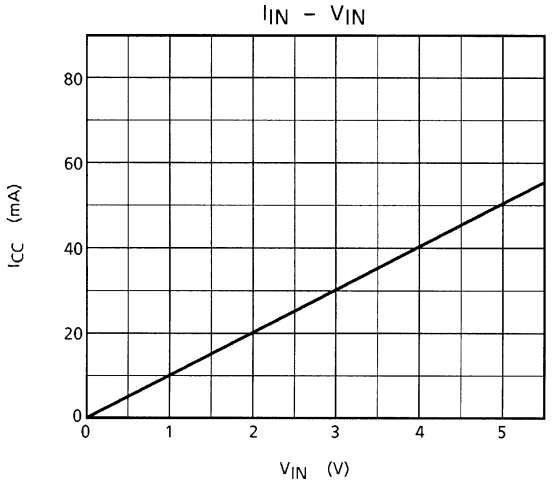
I_{CC} – V_{CC}



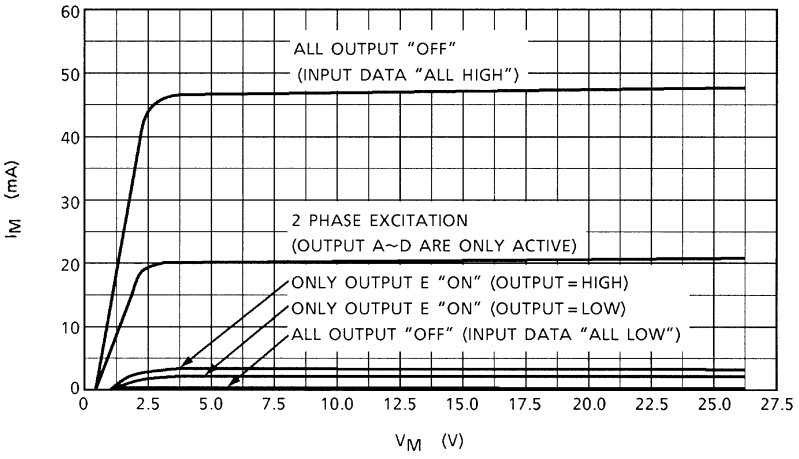
I_{CC} – V_{CC}



I_{IN} – V_{IN}

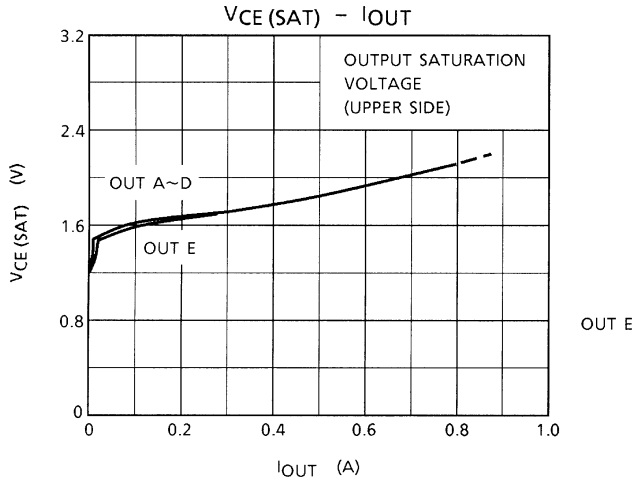


I_M – V_M (OUTPUT "OPEN")



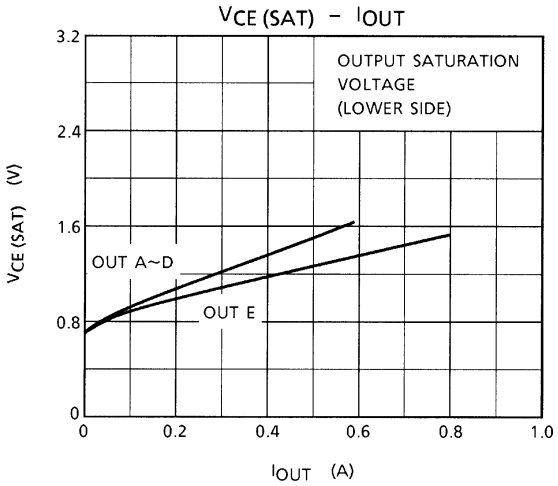
NOTE: $I_M = I_{M-AB} + I_{M-CD} + I_{M-E}$

$V_{CE(SAT)}$ – I_{OUT}

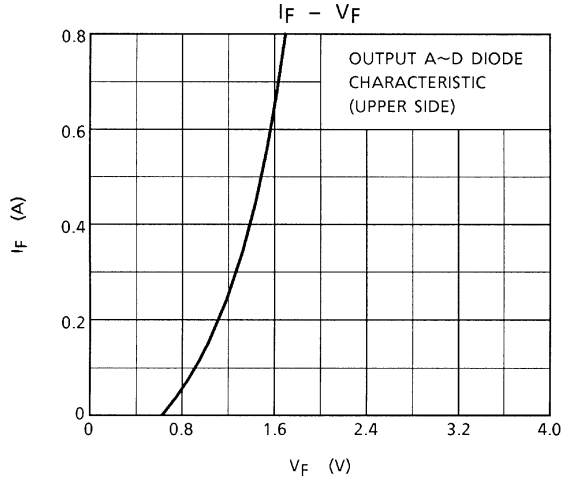


OUT E

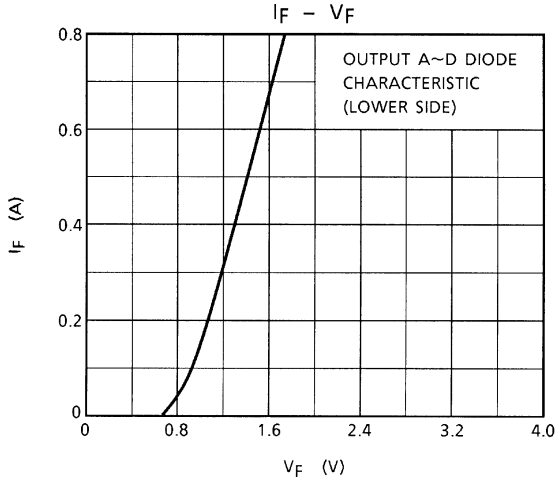
$V_{CE(SAT)}$ – I_{OUT}



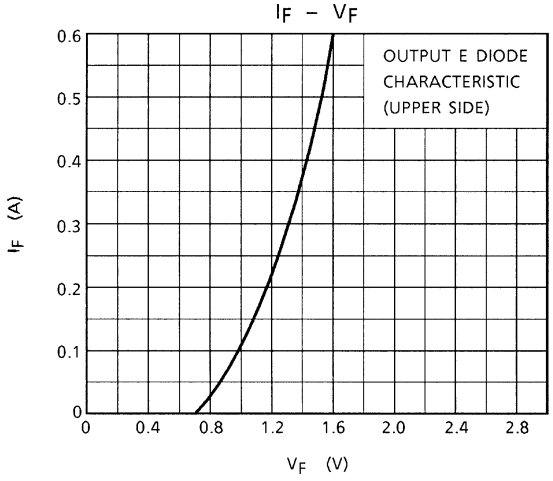
I_F – V_F



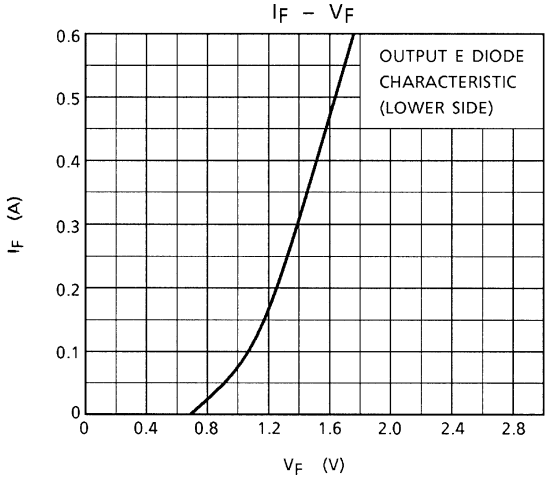
I_F – V_F



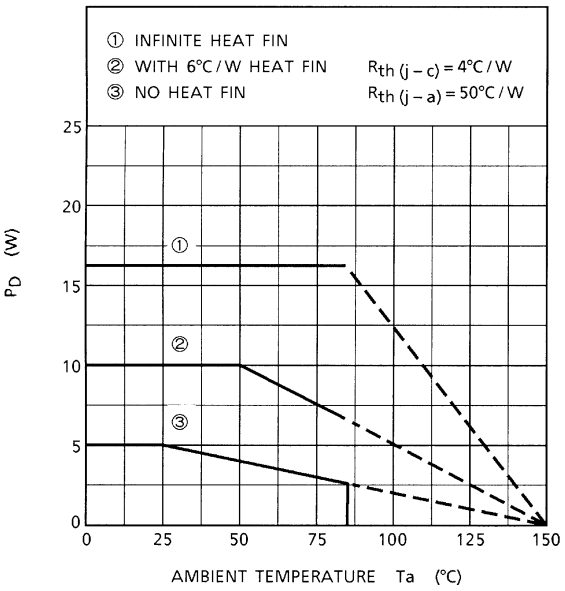
$I_F - V_F$



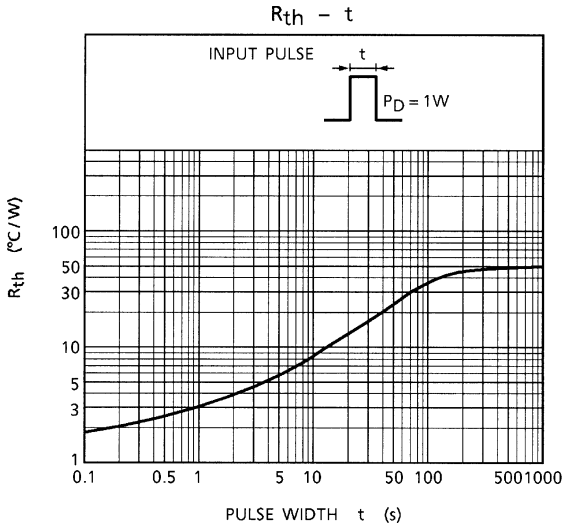
$I_F - V_F$



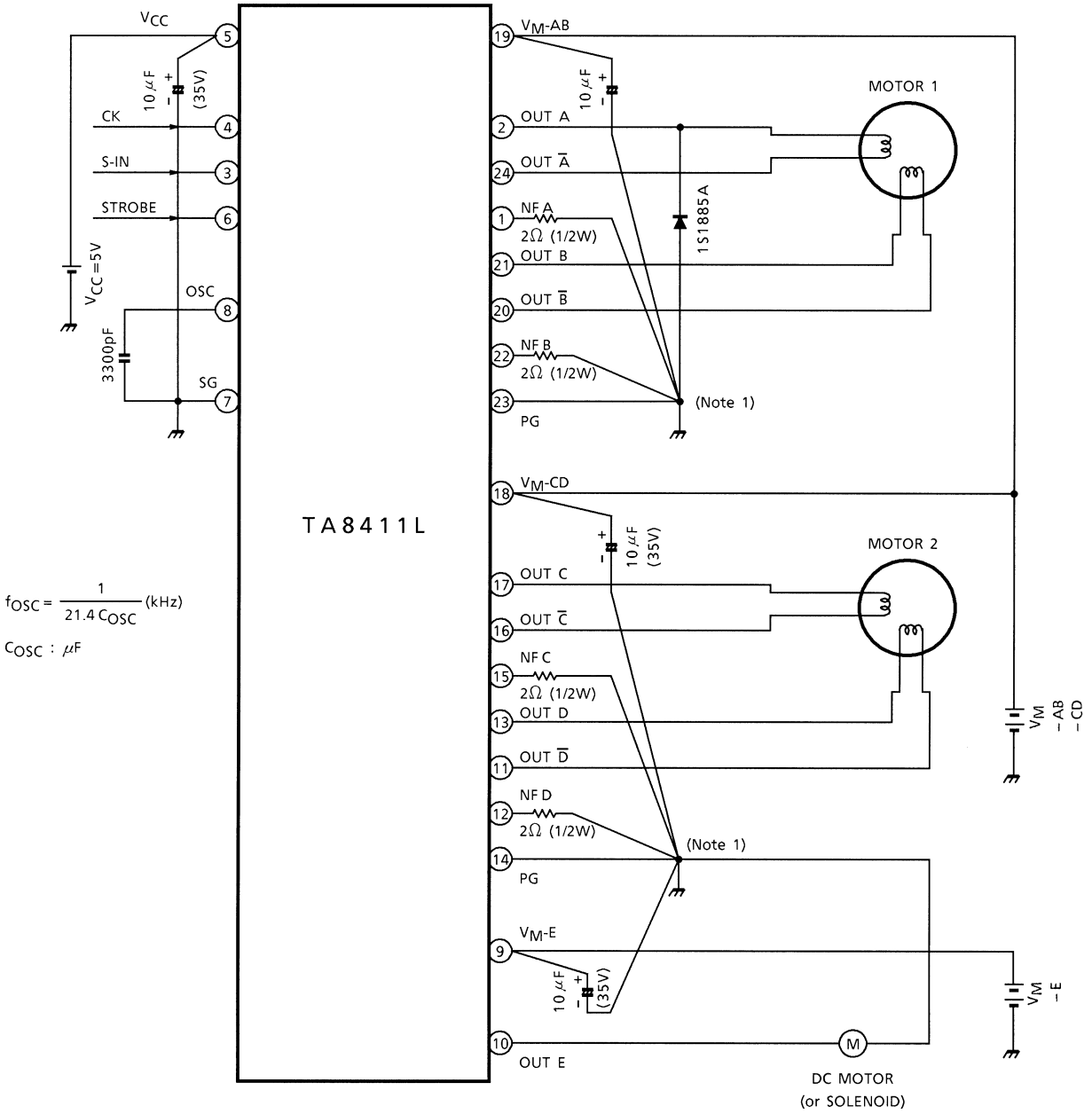
$P_D - Ta$



$R_{th} - t$



APPLICATION CIRCUIT

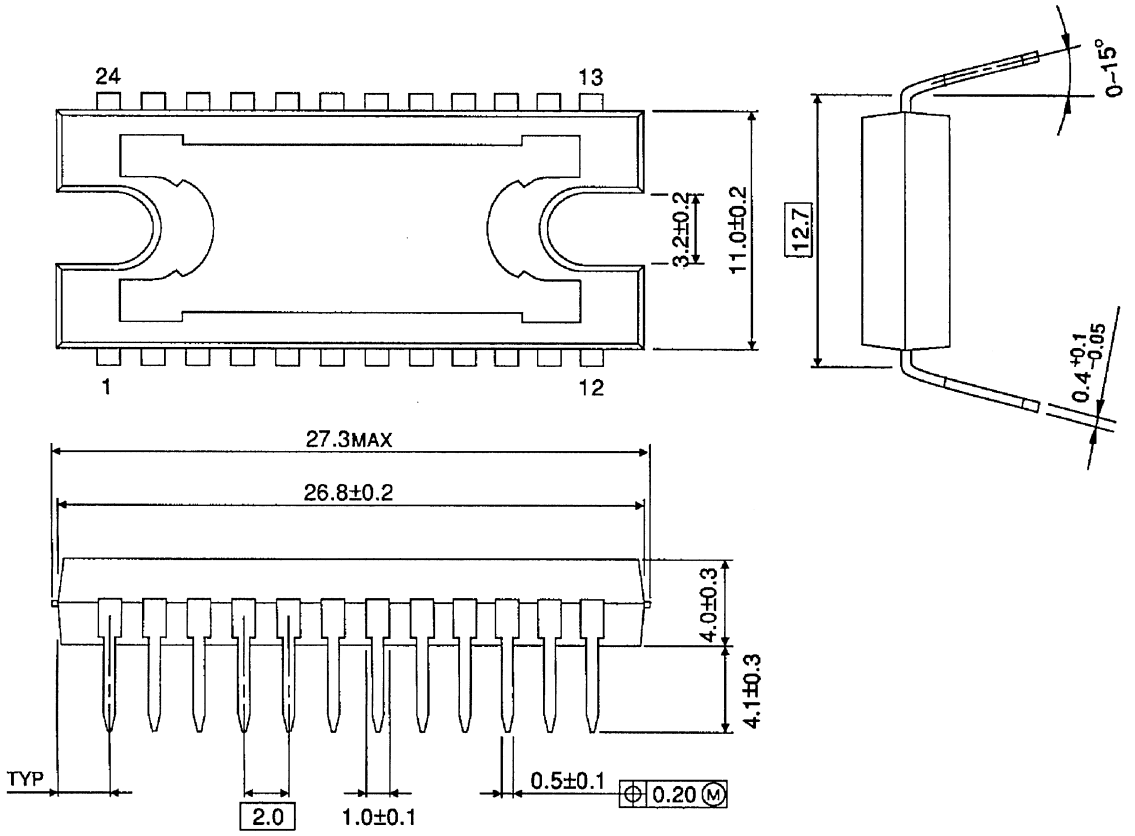


Note 1: Care should be taken not to have a common impedance with Output Current pass of each Motor (NF A, NF B for Motor 1, NF C, NF D for Motor 2 and PG for DC Motor) and any other signal lines.
And recommend to take One Point GND with each Output Current pass and corresponding PG terminal.
(See Table 1 of Block Diagram.

Note 2: Utmost care is necessary in the design of the output line, V_M and GND line since IC may be destroyed due to short−circuit between outputs, air contamination fault, or fault by improper grounding.

OUTLINE DRAWING

HDIP24−P500−2.00 Unit: mm



Weight: 4.30 g (Typ.)