

6367254 MOTOROLA SC (XSTRS/R F)
 BU204, BU205

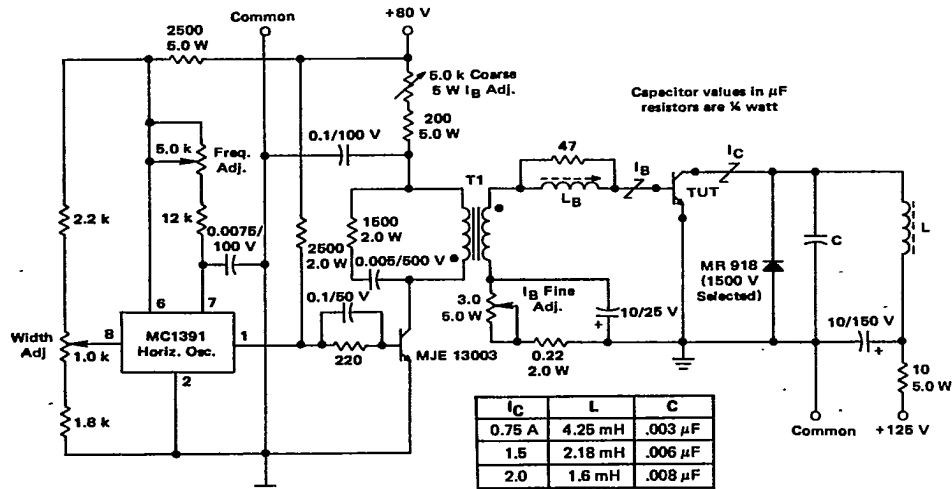
96D 80661 D
 T-33-11

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage ($I_C = 100$ mA, $I_B = 0$)	BU204 BU205	$V_{CE(sus)}$	600 700	— —	— —	Vdc
Collector Cutoff Current ($V_{CE} = 1300$ Vdc, $V_{BE} = 0$) ($V_{CE} = 1500$ Vdc, $V_{BE} = 0$)	BU204 BU205	I_{CES}	— —	— —	1.0 1.0	mA
Emitter Base Voltage ($I_E = 10$ mA, $I_C = 0$)		V_{EBO}	5.0	—	—	Vdc
ON CHARACTERISTICS (1)						
Collector-Emitter Saturation Voltage ($I_C = 2.0$ A, $I_B = 1.0$ A)		$V_{CE(sat)}$	—	—	5.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 2.0$ A, $I_B = 1.0$ A)		$V_{BE(sat)}$	—	—	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased		$I_{S/B}$	See Figure 14			
DYNAMIC CHARACTERISTICS						
Current-Gain - Bandwidth Product (1) ($I_C = 0.1$ A, $V_{CE} = 5.0$ Vdc, $f_{test} = 1.0$ MHz)		f_T	—	4.0	—	MHz
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f = 1.0$ MHz)		C_{ob}	—	50	—	pF
SWITCHING CHARACTERISTICS						
Fall Time ($I_C = 2.0$ A, $I_{B1} = 1.0$ A, $L_B = 25$ μ H) (See Figure 1)		t_f	—	0.65	—	μ s

(1) Pulse Test: Pulse Width < 300 μ s, Duty Cycle = 2%.

FIGURE 1 - TEST CIRCUIT



DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance - 39 mH. Secondary Inductance - 22 mH. Leakage Inductance with primary shorted - 2.0 μ H. Primary 260 turns #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.



BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM} . Worst case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM} , I_{B1} , and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B , at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown

in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1} , and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1} h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM} . As L_B is increased, the curves become broader and flatter above the $I_{B1} h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE} , essentially moves the curves to the left or right according to the relation $I_{B1} h_{FE} = \text{constant}$. It then becomes obvious that, for a specified I_{CM} , an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1} . The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM} . These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

TEST CIRCUIT WAVEFORMS

FIGURE 2

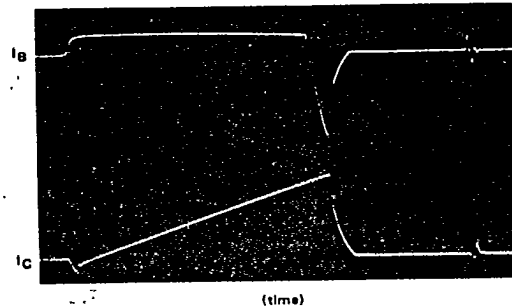
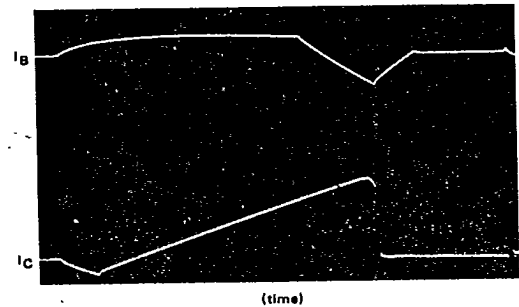


FIGURE 3



3

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance.

Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

6367254 MOTOROLA SC (XSTRS/R F)
 BU204, BU205

96D 80663 D

T-33-11

FIGURE 4 - OPTIMIZING DRIVE @ $I_C = 0.75$ A

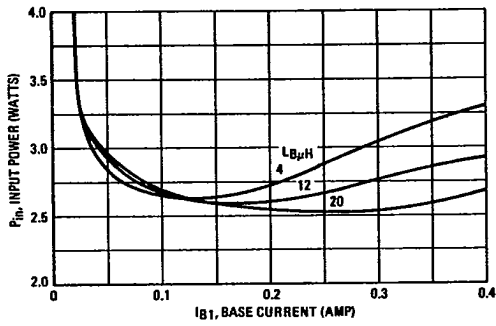


FIGURE 5 - OPTIMIZING DRIVE @ $I_C = 1.5$ A

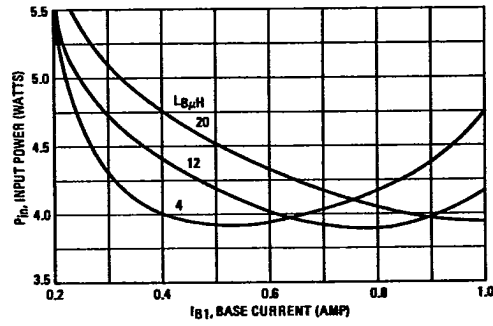


FIGURE 6 - OPTIMIZING DRIVE @ $I_C = 2.0$ A

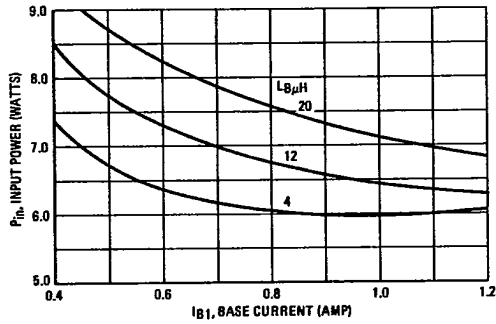


FIGURE 7 - SWITCHING BEHAVIOR versus TEMPERATURE

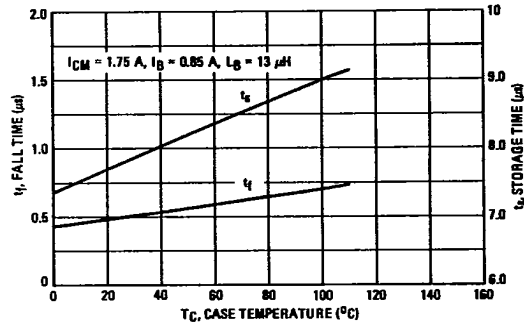


FIGURE 8 - OPTIMUM DRIVE CONDITIONS

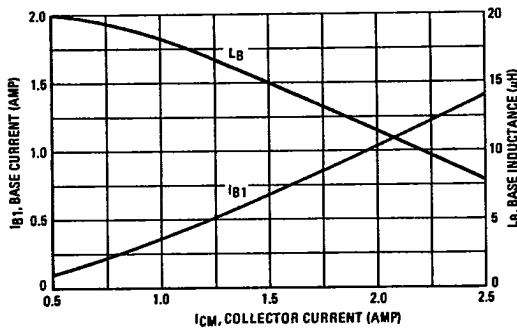


FIGURE 9 - SWITCHING BEHAVIOR versus I_{CM}

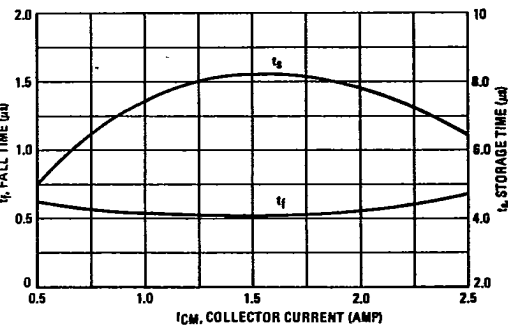


FIGURE 10 - THERMAL RESPONSE

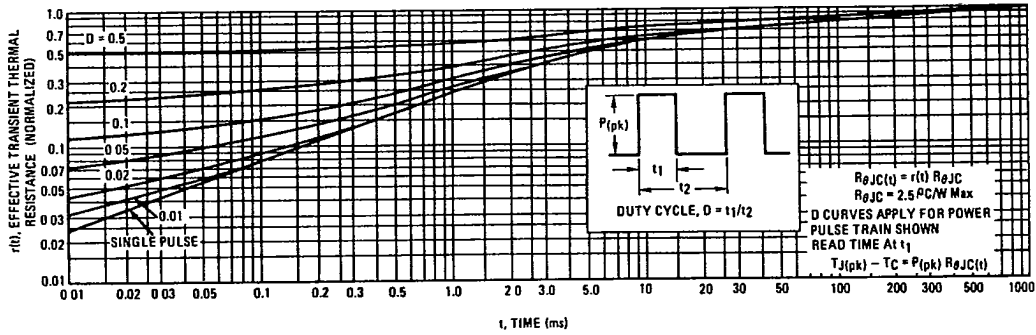


FIGURE 11 - COLLECTOR SATURATION REGION

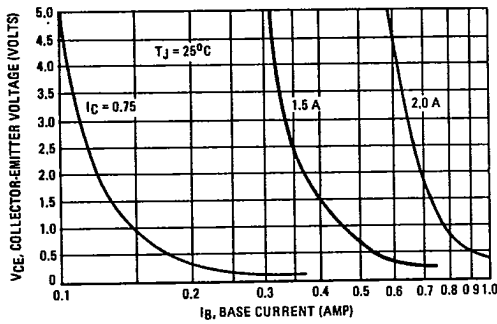


FIGURE 12 - DC CURRENT GAIN

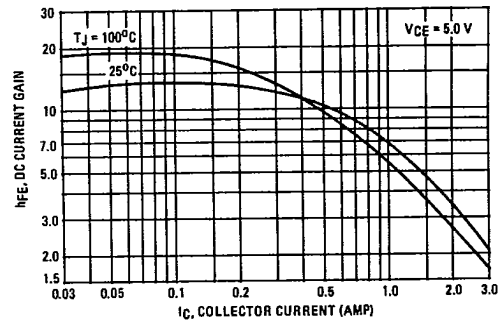


FIGURE 13 - "ON" VOLTAGES

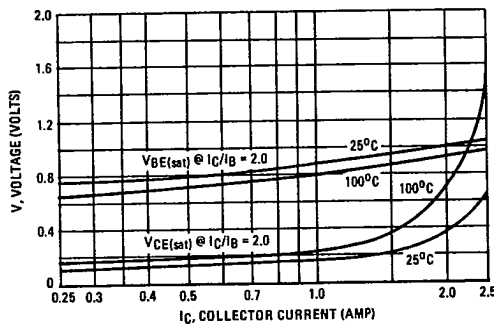


FIGURE 14 - MAXIMUM FORWARD BIAS SAFE OPERATING AREA

