

# BUV27

## NPN Silicon Power Transistor

This device is designed for use in switching regulators and motor control.

### Features

- Low Collection Emitter Saturation Voltage
- Fast Switching Speed
- Pb-Free Package is Available\*

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	120	Vdc
Collector-Emitter Breakdown Voltage	$V_{CBO}$	240	Vdc
Emitter-Base Voltage	$V_{EBO}$	7.0	Vdc
Collector Current – Continuous – Peak (Note 1)	$I_C$ $I_{CM}$	12 20	Adc
Base Current	$I_B$	4.0	Adc
Total Device Dissipation ( $T_C = 25^\circ\text{C}$ ) Derate above $25^\circ\text{C}$	$P_D$	70 0.56	W W/ $^\circ\text{C}$
Operating and Storage Temperature	$T_J, T_{stg}$	- 65 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case Junction-to-Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.78 62.5	$^\circ\text{C}/\text{W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle  $\leq 10\%$ .

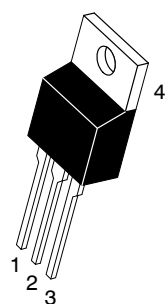


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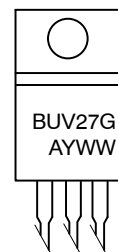
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**POWER TRANSISTOR**  
**12 AMPERES**  
**120 VOLTS**  
**70 WATTS**

### MARKING DIAGRAM



**TO-220AB**  
**CASE 221A**  
**STYLE 1**



BUV27 = Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping
BUV27	TO-220AB	50 per Rail
BUV27G	TO-220AB (Pb-Free)	50 per Rail

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I <sub>CER</sub>	Collector Cut-off Current (R <sub>BE</sub> = 50 Ω)	V <sub>CE</sub> = 240 V, T <sub>C</sub> = 125°C			3.0	mA
I <sub>CEX</sub>	Collector Cut-off Current	V <sub>CE</sub> = 240 V, V <sub>BE</sub> = -1.5 V, T <sub>C</sub> = 125°C			1.0	mA
I <sub>EBO</sub>	Emitter Cut-off Current (I <sub>C</sub> = 0)	V <sub>BE</sub> = 5 V			1.0	mA
V <sub>CEO(sus)</sub>	Collector-Emitter Sustaining Voltage	I <sub>C</sub> = 0.2 A, L = 25 mH	120			V
V <sub>EBO</sub>	Emitter-Base Voltage (I <sub>C</sub> = 0)	I <sub>E</sub> = 50 mA	7.0		30	V
V <sub>CE(sat)</sub> (Note 2)	Collector-Emitter Saturation Voltage	I <sub>C</sub> = 4 A, I <sub>B</sub> = 0.4 A I <sub>C</sub> = 8 A, I <sub>B</sub> = 0.8 A			0.7 1.5	V
V <sub>BE(sat)</sub> (Note 2)	Base-Emitter Saturation Voltage	I <sub>C</sub> = 8 A, I <sub>B</sub> = 0.8 A			2.0	V

### Resistive Load

t <sub>on</sub>	Turn-on Time	V <sub>CC</sub> = 90 V, I <sub>C</sub> = 8 A		0.4	0.8	ms
t <sub>s</sub>	Storage Time	V <sub>BE</sub> = -6 V, I <sub>B1</sub> = 0.8 A		0.5	1.2	μs
t <sub>f</sub>	Fall Time	R <sub>BB</sub> = 3.75 Ω		0.12	0.25	μs

### Inductive Load

t <sub>s</sub>	Storage Time	V <sub>CC</sub> = 90 V, I <sub>C</sub> = 8 A		0.6		μs
t <sub>f</sub>	Fall Time	I <sub>B1</sub> = 0.8 A, V <sub>BE</sub> = -5 V L <sub>B</sub> = 1 μH		0.04		
t <sub>s</sub>	Storage Time	V <sub>CC</sub> = 90 V, I <sub>C</sub> = 8 A			2.0	
t <sub>f</sub>	Fall Time	I <sub>B1</sub> = 0.8 A, V <sub>BE</sub> = -5 V L <sub>B</sub> = 1 μH, T <sub>J</sub> = 125°C			0.15	

2. Pulsed: Pulse Duration = 300 μs, Duty Cycle = 2%

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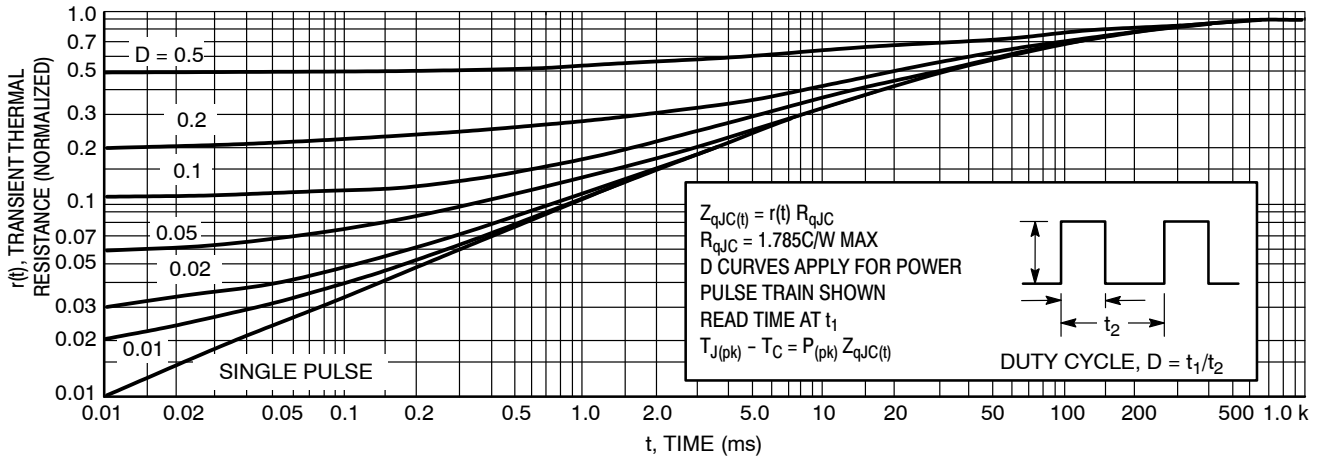


Figure 1. Thermal Response

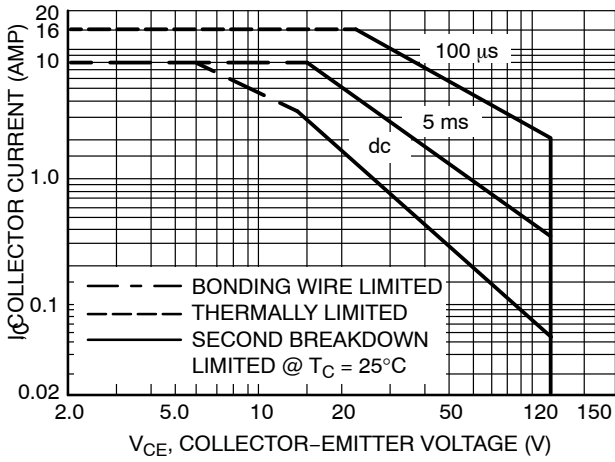


Figure 2. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 2 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

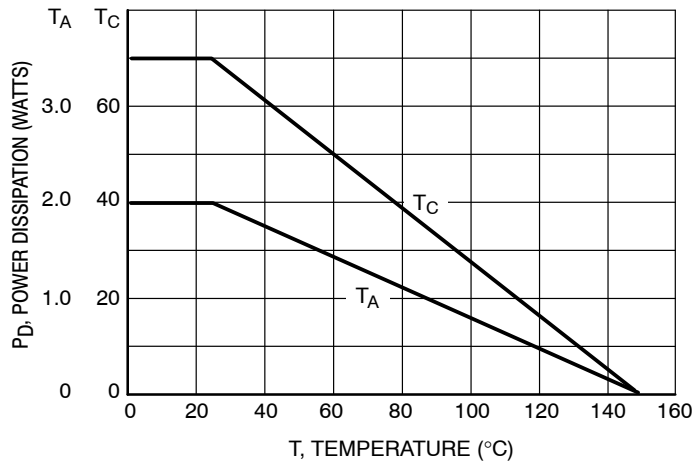
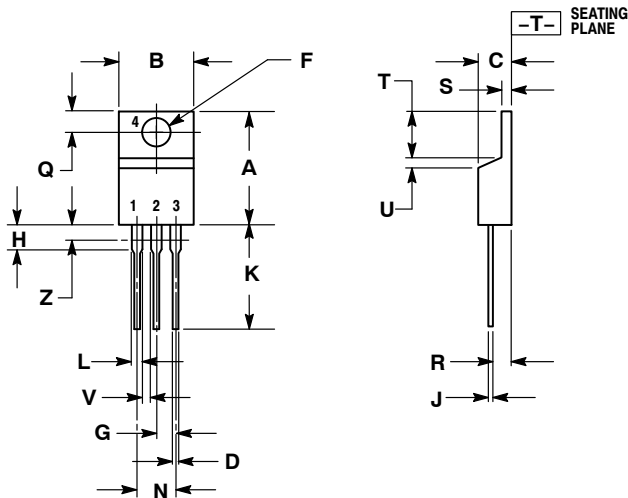


Figure 3. Power Derating

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## PACKAGE DIMENSIONS

### TO-220 CASE 221A-09 ISSUE AG



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.036	0.64	0.91
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

#### STYLE 1:

- PIN 1. BASE
- COLLECTOR
- EMITTER
- COLLECTOR

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