Cortina Systems® LXT971A, LXT972A, LXT972M Single-Port 10/100 Mbps PHY Transceivers

Specification Update

15 March 2007

Document Number 249354

Revision 13.0

*Other names and brands may be claimed as the property of others.

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1.0 Revision History

Revision 13.0 Revision Date: 07 March 2007
First release of this document from Cortina Systems, Inc.

Revision 012 Revision Date: 01 November 2005
• Modified Table 3, Product Ordering Information, on page 18. • Modified Figure 9, Ordering Information Matrix - Sample, on page 19.

Revision 011 Revision Date: 29 September 2005
• Modified Figure 1, Sample LQFP Package - Intel* LXT971A and LXT972A Transceivers, on page 9. • Modified Figure 2, Sample Pb-Free (RoHS-Compliant) LQFP Package - Intel* LXT971A and LX972A Transceivers, on page 9. • Added new figures: Figure 3, Sample LQFP Package - Intel* LXT972M Transceiver, on page 10, Figure 4, Sample Pb-Free (RoHS-Compliant) LQFP Package - Intel* LXT972M Transceiver, on page 10, Figure 5, Sample TPBGA Package - Intel* LXT971A Transceiver, on page 11, Figure 6, Sample Pb-Free (RoHS-Compliant) TPBGA Package - Intel* LXT971A Transceiver, on page 11 • Changed Table 3, Product Ordering Information, on page 18 • Changed Figure 9, Ordering Information Matrix - Sample, on page 19 • Removed Sightings from this document and placed into a Sightings Report.

Revision 010 Revision Date: 13 January 2005
• Revised Figure 1, “Example of Pb-Free LQFP Package for LXT971A, LX972A, and LXT972M Transceivers” and descriptive text that references this figure. • Revised Figure 2, “Example of LQFP Package for LXT971A, LXT972A, and LXT972M Transceivers” and descriptive text that references this figure. • Revised Table 2, “Product Information”. • Revised Figure 5, “Ordering Information - Sample”.

Revision 009 Revision Date: 29 September 2004
• Added the LXT972M Single-Port 10/100 Mbps PHY Transceiver where appropriate. • Revised Erratum item 4. Clarified workaround. • Revised Erratum item 5. Moved previous Note to Errata table. • Revised Erratum item 9. Moved previous Note to Errata table. • Revised Erratum item 10. Moved previous Note to Errata table. • Revised Erratum item 11. Moved previous Note to Errata table. • Revised “Sightings” section.

Revision 008 Revision Date: 02 September 2003
• Added Errata items 13 through 15 to “Errata” table. • Removed Item 1 in “Specification Clarifications” table. • Modified steppings table under “Identification Information” section (added JTAG ID information). • Added Erratum 13: “Changing Advertised Duplex While Link Is Up” to “Errata” section. • Added Erratum 14: “Far-End Fault Reporting” to “Errata” section. • Added Erratum 15: “Detection of Illegal Symbols After SSD” to “Errata” section. • Incorporated tables under “Specification Clarifications” into the LXT971A and LXT972A Datasheets and removed from this document. • Incorporated “Item 3: Increased MII Drive Strength” under the “Addenda” section into the LXT971A and LXT972A Datasheets and removed from this document.

Revision 007 Revision Date: 17 May 2002
• Updated “Affected Documents” Table. • Updated “Codes Used in Summary Table”. • Updated “Errata” Listing. • Added Erratum: “Switching Clocks from 100 Mbps to 10 Mbps Prior to End of Packet”. • Added Addendum: ”Increased MII Drive Strength”.

Revision 006 Revision Date: 17 August 2001
• Documentation Changes: Modified to reflect document rev numbers. • Modified Absolute Maximum Ratings table.

Revision 005 Revision Date: 27 June 2001
• Addenda: Clarified Description 1.

Revision 004 Revision Date: 20 June 2001
• Added Product Ordering Information.

Revision 003 Revision Date: 09 May 2001
• Errata 7, 9, 10, 11, 12 were fixed in Stepping 2. Removed “Xs” for correct status.

Revision 002 Revision Date: 20 March 2001
• Updated “Markings” table with Manufacturer’s Revision Code information. • Replaced text with “None” for Workaround under Errata 9. • Added BSDL text to Workaround under Errata 11.

Revision 001 Revision Date: 15 January 2001
First release.

2.0 Preface

This document is an update to the specifications contained in the Affected Documents/ Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Stepping 2 devices are labeled as LXT971A, LXT972A, and LXT972M Transceivers.

2.1 Affected Documents/Related Documents

Title	Document Number
Cortina Systems® LXT971A 3.3V Dual-Speed Fast Ethernet Transceiver Datasheet	249185
Cortina Systems® LXT972A 3.3V Dual-Speed Fast Ethernet Transceiver Datasheet	249186
Cortina Systems® LXT971A/972A 3.3V PHY Transceivers Design and Layout Guide Application Note	249016
Cortina Systems® LXT971A — LXT970A-to-LXT971A Migration Application Note	249028
Cortina Systems® LXD971B Demo Board for 3.3V 10/100 Applications (Board Rev A1) Development Kit Manual	249246
Cortina Systems® LXD971L Demo Board for 3.3V 10/100 Applications (Board Rev B2) Development Kit Manual	249247
Cortina Systems® LXT972M Single-Port 10/100 Mbps PHY Transceiver Datasheet	302875
Cortina Systems® LXT972M Transceiver Demo Board (Board Rev A1)	303125
Cortina Systems® LXT971A 3.3V Dual-Speed Fast Ethernet Transceiver Datasheet	249185
Cortina Systems® LXT972A 3.3V Dual-Speed Fast Ethernet Transceiver Datasheet	249186

2.2 Nomenclature

Errata are design defects or errors. These may cause the behaviors of the following to deviate from published specifications:

- LXT971/LXT971A 3.3V Dual-Speed Fast Ethernet Transceiver (called hereafter the LXT971A Transceiver)
- LXT972/LXT972A 3.3V Dual-Speed Fast Ethernet Transceiver (called hereafter the LXT972A Transceiver)
- LXT972M Single-Port 10/100 Mbps PHY Transceiver (called hereafter the LXT972M Transceiver).

Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, and so on).

3.0 Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Cortina Systems® LXT971A, LXT972A, LXT972M Single-Port 10/100 Mbps PHY Transceivers (LXT97x PHY Transceivers). Cortina Systems, Inc. (Cortina) may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

3.1 Codes Used in Summary Table

3.1.1 Stepping

X: Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.

(No mark)

or (Blank box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

3.1.2 Page

(Page): Page location of item in this document.

3.1.3 Status

Doc: Document change or update will be implemented.

Plan Fix: This erratum may be fixed in a future stepping of the product.

Fixed: This erratum has been previously fixed.

No Fix: There are no plans to fix this erratum.

3.2 Errata (Sheet 1 of 2)

No.	Steppings			Page	Status	ERRATA
	#	#	#			
1	X			page 15	Fixed	Section 1, *Incorrect Auto-Negotiation Link Partner Base Page Ability Register*
2	X			page 15	Fixed	Section 2, *Incorrect Auto-Negotiation Next Page*
3	X			page 15	Fixed	Section 3, *Incorrect Remote Fault*
4	X			page 15	Fixed	Section 4, *Incorrect Auto-Negotiation Duplex Status*
5	X	X		page 16	Fixed	Section 5, *Incorrect JTAG Revision Code*
6	X	X		page 16	Fixed	Section 6, *Incorrect Duplex - Collision LED Display*

Notes:
1. Refer to Section 4.1, *Markings, on page 10* for codes to identify various silicon steppings.
2. Devices with an A suffix (such as the LXT971A and LXT972A Transceiver) are Stepping 2.
3. The LXT972M Transceiver is available only as Stepping 2.

3.2 Errata (Sheet 2 of 2)

No.	Steppings			Page	Status	ERRATA
	#	#	#			
7	X	X		page 17	Fixed	Section 7, *Incorrect Activity LED Display*
8	X			page 17	Fixed	Section 8, *MII Pins Not Three-Stateable*
9	X	X		page 17	Fixed	Section 9, *100 M External Loopback Using Short Cable Length*
10	X	X		page 18	Fixed	Section 10, *10BASE-T Data Inversion*
11	X	X		page 18	Fixed	Section 11, *Power Cycling and JTAG TRST Reset Pin*
12	X	X		page 18	Fixed	Section 12, *Switching Clocks from 100 Mbps to 10 Mbps Prior to End-of-Packet*
13	X	X	X	page 18	No Fix	Section 13, *Changing Advertised Duplex While Link Is Up*
14	X	X	X	page 19	No Fix	Section 14, *Far-End Fault Reporting*
15	X	X	X	page 19	No Fix	Section 15, *Detection of Illegal Symbols After SSD*

Notes:
1. Refer to Section 4.1, *Markings, on page 10* for codes to identify various silicon steppings.
2. Devices with an A suffix (such as the LXT971A and LXT972A Transceiver) are Stepping 2.
3. The LXT972M Transceiver is available only as Stepping 2.

3.3 Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	#	#			
					None for this revision of this specification update.

3.4 Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

3.5 Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES

4.0 Identification Information

4.1 Markings

This section explains the markings for the LXT97x PHY Transceivers. Table 1 list the types of packages available. (For more ordering information, see Figure 10, *Ordering Information Matrix - Sample, on page 24*.)

Table 1 Types of Available Packages

Product	Non-RoHS-Compliant Package Available	Reduction of Hazardous Substances (RoHS) Package Available
LXT971A and LXT972A Transceivers	Low-Profile Quad Flat Pack (LQFP)	LQFP RoHS
LXT971AB Transceiver	Thin Plastic Ball Grid Array (TPBGA)	TPBGA RoHS
LXT972L Transceiver	LQFP	LQFP RoHS
LXT972M Transceiver	Micro LQFP	Micro LQFP RoHS

Figure 2 shows a sample LQFP package for the LXT971A and LXT972A Transceivers.

Note: In contrast to the Pb-Free (RoHS-compliant) LQFP package, the non-RoHS-compliant package does not have the “e3” symbol in the last line of the package label.

Figure 1 Example of Top Marking Information Labeled as Cortina Systems, Inc.

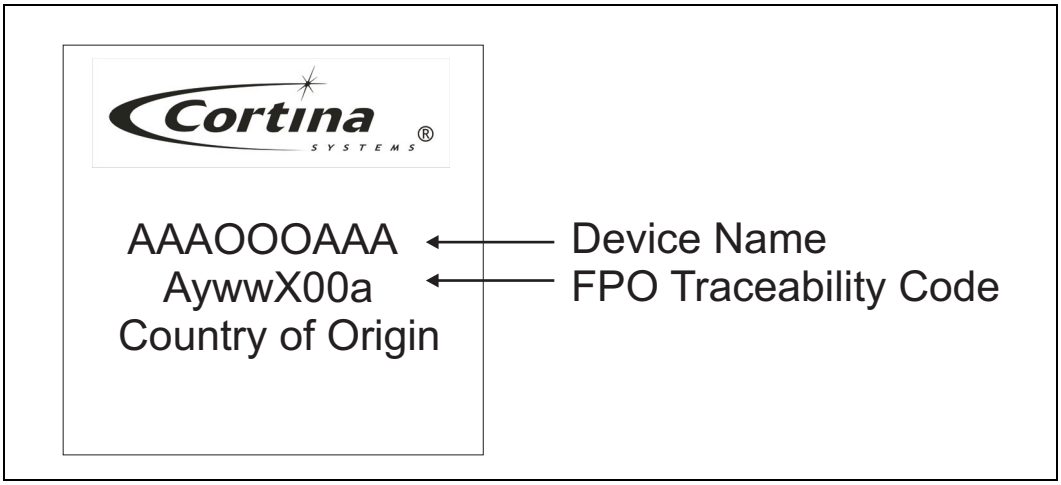


Figure 2 Sample LQFP Package - Intel* LXT971A and LXT972A Transceivers

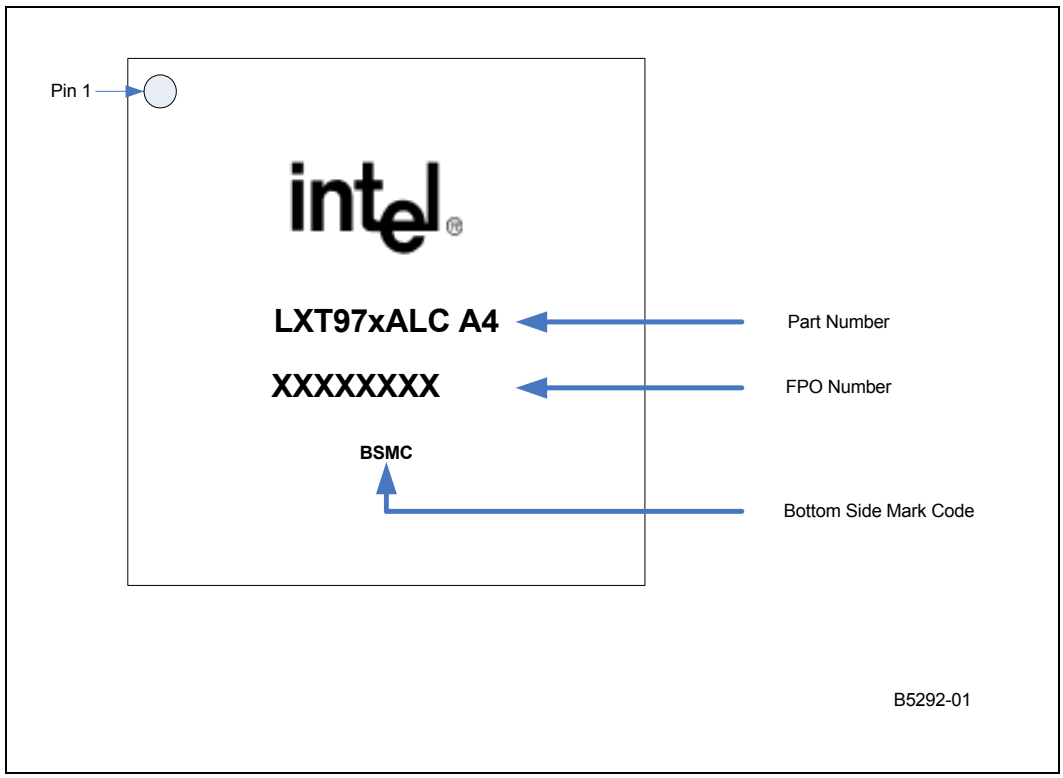


Figure 3 shows a sample Pb-Free (RoHS-compliant) LQFP package for the LXT971A and LXT972A Transceivers.

Figure 3 Sample Pb-Free (RoHS-Compliant) LQFP Package - Intel* LXT971A and LX972A Transceivers

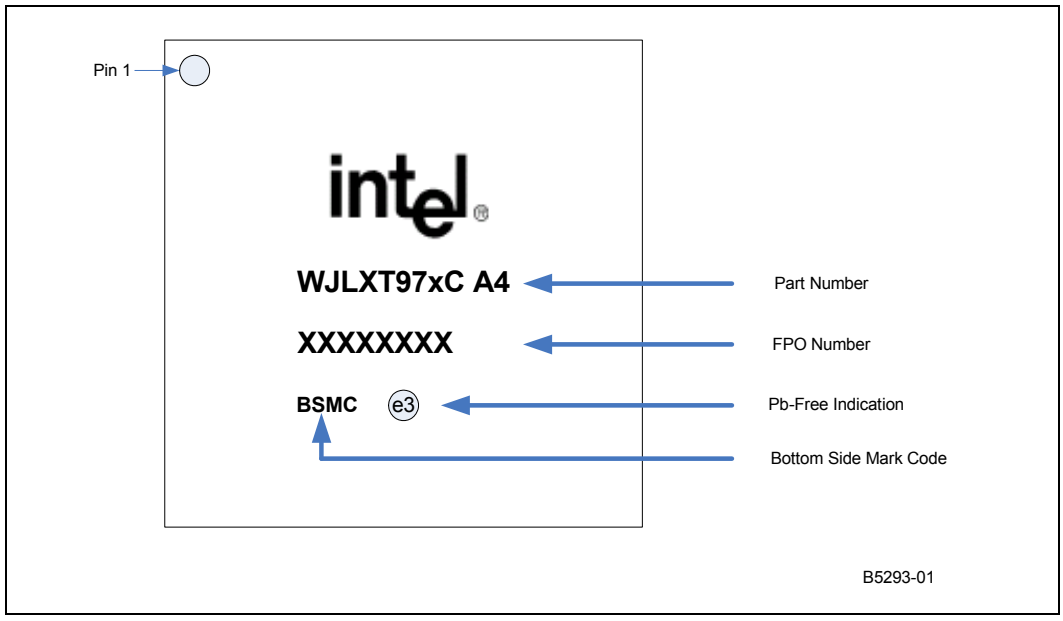


Figure 4 shows a sample LQFP package for the LXT972M Transceiver.

Note: In contrast to the Pb-Free (RoHS-compliant) LQFP package, the non-RoHS-compliant package does not have the “e3” symbol in the last line of the package label.

Figure 4 Sample LQFP Package - Intel* LXT972M Transceiver

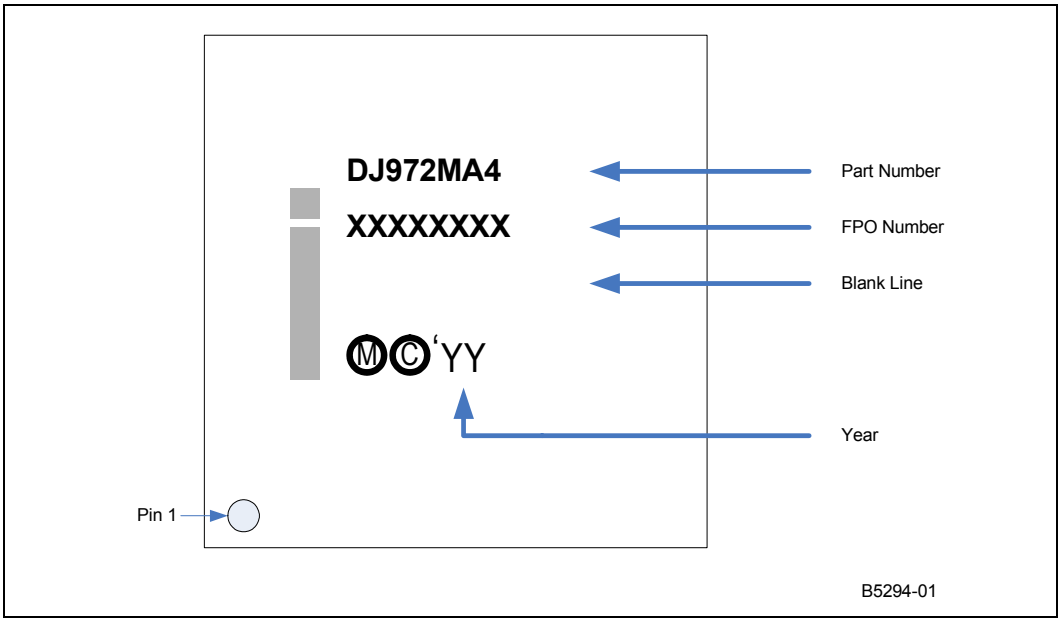


Figure 5 shows a sample Pb-Free (RoHS-compliant) LQFP package for the LXT972M Transceiver.

Figure 5 Sample Pb-Free (RoHS-Compliant) LQFP Package - Intel* LXT972M Transceiver

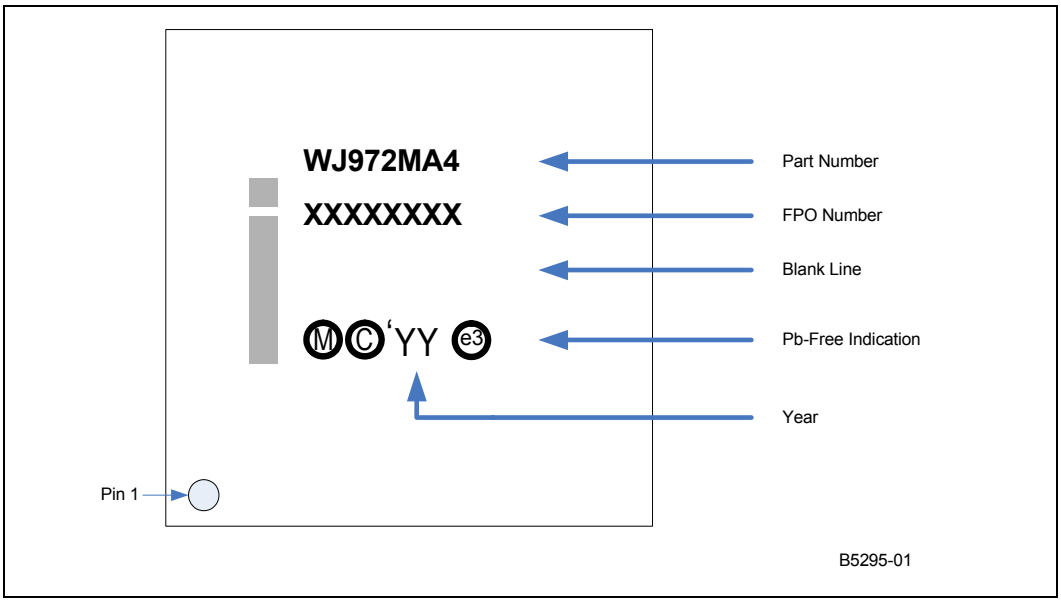


Figure 6 shows a sample TPBGA package for the LXT971A Transceiver.

Note: In contrast to the Pb-Free (RoHS-compliant) TPBGA package, the non-RoHS-compliant package does not have the “e3” symbol in the last line of the package label.

Figure 6 Sample TPBGA Package - Intel* LXT971A Transceiver

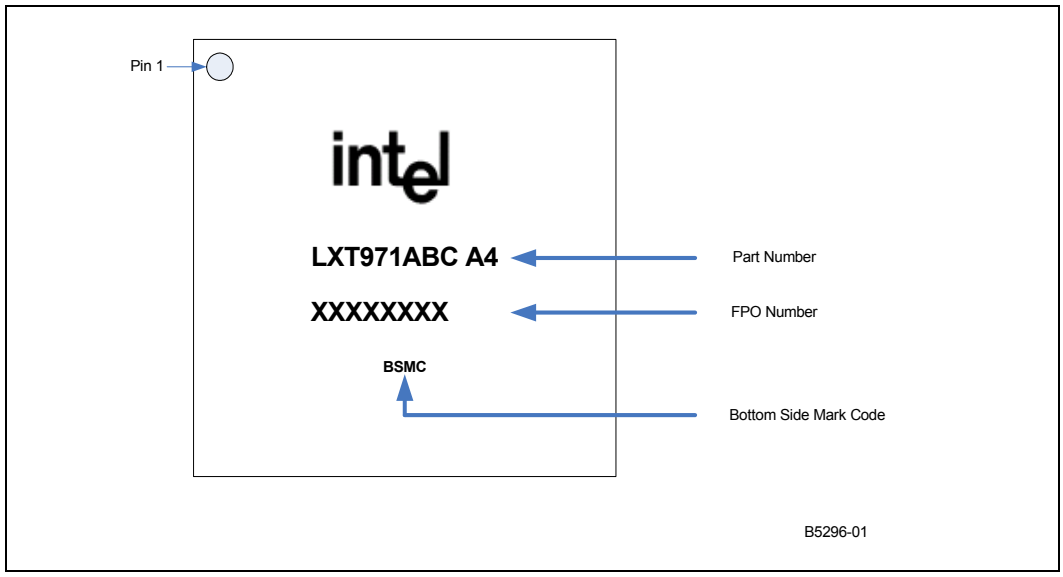


Figure 7 shows a sample Pb-Free (RoHS-Compliant) TPBGA package for the LXT971A Transceiver.

Figure 7 Sample Pb-Free (RoHS-Compliant) TPBGA Package - Intel* LXT971A Transceiver

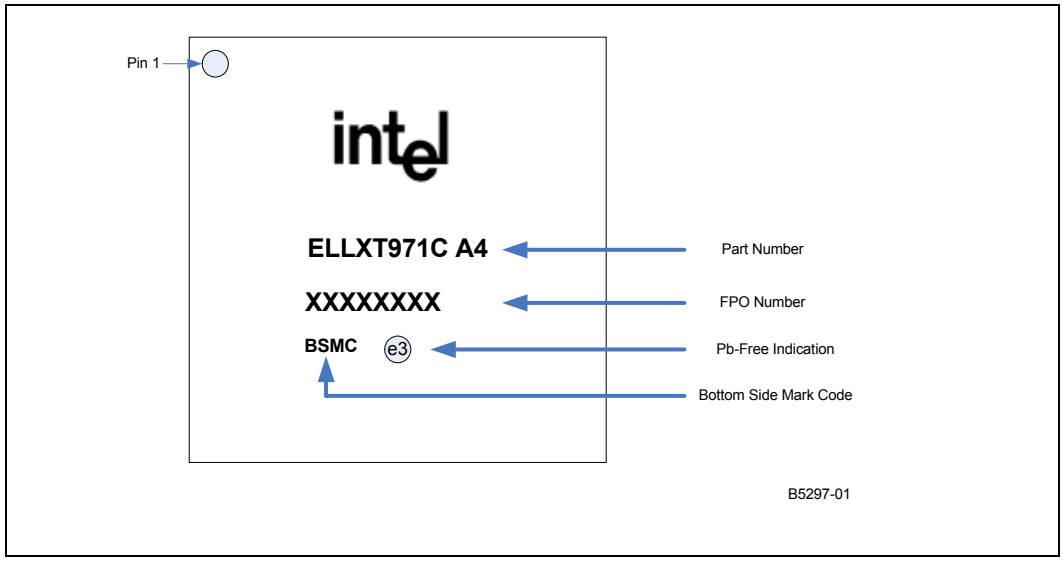


Figure 8 shows the LQFP package for previous revisions of the LXT971A and LXT972A Transceivers.

Figure 8 Package for Previous Revision of Intel* LXT971A and LXT972A Transceivers

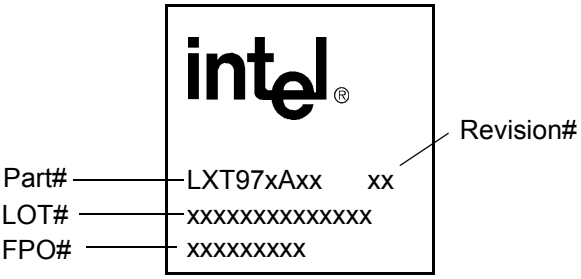
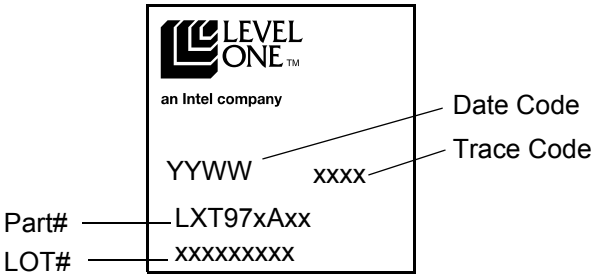


Figure 9 shows the LQFP package for previous revisions of the LXT971A and LXT972A Transceivers. (This figure is for reference only.)

Figure 9 Package for Level One LXT971A and LXT972A Transceivers (Reference Only)



In the datasheets for the LXT97x PHY Transceivers, the silicon stepping is referred to as "Manufacturer's Revision Number." Software can read the silicon stepping number from Register bits 3.3:0. Table 2 lists the manufacturer's revision number, trace codes, and JTAG version IDs for LXT97x PHY Transceivers steppings.

Table 2 Revision Numbers, Trace Codes, and JTAG Versions IDs

Stepping	Revision Number	Trace Codes[1]	Manufacturer's Revision Number[2]	JTAG Version ID[3]
0	A1	xxAx	0000	0000
1	A2	xxBx	0001	0001
2	A4	xxDx	0010	0010

1. The letter "*x*" indicates an insignificant variable.
2. The value of the revision number is from register bits 3.3:0. For details, see the datasheets for the LXT97x PHY Transceivers.
3. For details on the JTAG version ID, see the Device ID Register tables in the datasheets for the LXT97x PHY Transceivers.

5.0 Errata

Item 1: Incorrect Auto-Negotiation Link Partner Base Page Ability Register

Problem Upon completing the parallel detection function, the Auto-Negotiation Link Partner Base Page Ability Register (Register 5) should be updated to reflect the link partner's capability. Register 5 is not updated correctly and always reads 0000h.

Workaround The Status Register #2 (Register 17) is properly updated with the arbitrated link status information and can be used to identify link speed and duplex status.

Status Fixed.

Item 2: Incorrect Auto-Negotiation Next Page

Problem The Auto-Negotiation Next Page state machine functions incorrectly and does not support Next Page operations.

Workaround Bit 4.15 in the Auto-Negotiation Advertisement Register must be set to 0 (port has no ability to send multiple pages).

Status Fixed.

Item 3: Incorrect Remote Fault

Problem In fiber mode, the Remote Fault bit (Register bit 1.4) in MII Status Register #1 is used to report receipt of the Far End Fault Indication (FEFI) code to the MAC. The Remote Fault bit fails to indicate receipt of the FEFI code under certain conditions.

This occurs only when the following conditions are true:

- The device is operating in fiber mode, AND
- The device hardware configuration is set to enable auto-negotiation.

Workaround Strap the LED/CFG1 pin to ground to disable auto-negotiation.

Status Fixed.

Item 4: Incorrect Auto-Negotiation Duplex Status

Problem The LXT971A and LXT972A Transceivers fail to update the initial control setting for full-duplex or half-duplex operation (Register bit 0.8) after link is established. Under certain conditions, this can cause incorrect reporting of duplex status and collision events. This problem occurs under the following conditions:

- The LXT971A and LXT972A Transceivers are initially set for full-duplex operation, AND
- The LXT971A and LXT972A Transceivers establish a half-duplex link through auto-negotiation or parallel detection

OR

- The LXT971A and LXT972A Transceivers is initially set for half-duplex operation, AND
- The LXT971A and LXT972A Transceivers establish a full-duplex link through auto-negotiation or parallel detection.

Implication In the first case (half-duplex link established while control register is set for full-duplex), the LXT971Aand LXT972A Transceivers do the following:

- Function as a full-duplex port
- Indicate full-duplex through LED and Register bit 0.8
- Indicate half-duplex through Register bit 17.9
- Do not indicate collision (through the LED, MII COL signal, or Register bit 17.11) when transmitting and receiving concurrently

In the second case (full-duplex link established while control register is set for half-duplex), the LXT971A and LXT972A Transceivers do the following:

- Function as a half-duplex port
- Indicate half-duplex through the LED
- Indicate full-duplex through Register bit 17.9
- Indicate collision (through LED, MII COL signal, and Register bit 17.11) when transmitting and receiving concurrently

Workaround Set Status Register #2 (Register bit 17.9) to update the duplex status in the Control Register (Address 0). The Status Register #2 (Address 2) is updated with the correct duplex status when auto-negotiation is completed. Each time link is established, the duplex status in Register bit 17.9 can be used to update the duplex mode in the Control Register (Register bit 0.8).

Status Fixed.

Item 5: Incorrect JTAG Revision Code

Problem LXT971A and LXT972A Transceivers (A2) JTAG Device ID is as follows - 0001 03CB 1110 111 1110 1

As per the standard, the Jedec Continuation Character (Register bit 11:8) for the Cortina devices should have been 0000 instead of 1110.

Implication JTAG boundary scan receives an incorrect JTAG ID for the LXT971A and LXT972A Transceivers.

Workaround Use a continuation character of 1110 when addressing an LXT971A Transceiver Stepping 1.

Status Fixed.

Item 6: Incorrect Duplex - Collision LED Display

Problem When the port LED is configured to indicate Duplex and Collision through the LED Configuration Register (Address 20), the LED does not indicate Collision when transmitting and receiving in a half-duplex link.

Workaround Configure a separate LED for Collision only. A dedicated LED properly indicates a collision is occurring.

Status Fixed.

Item 7: Incorrect Activity LED Display

Problem With pulse stretching enabled, port activity is indicated with a slow blinking rate on the activity LED when the port is in full-duplex and the port transmit and receive traffic has the same packet size and inter-packet gap (IPG) for an extended period of time. A correct indication is for the activity LED to remain active when continuously transmitting and receiving.

The activity LED resumes normal operation if either packet size or IPG is altered.

Implication The activity LED indication will not match the traffic rate at the port. Only the Activity LED behavior is affected. Neither transmit nor receive status LED functionality are affected.

The activity LED operation has no impact on data reliability.

Workaround Use the following steps for a possible workaround:

1. Use either transmit or receive status instead of activity as the LED indication.
2. Logically 'OR' transmit status and receive status to generate an activity indicator. This workaround requires external hardware to complete the 'OR' function.
3. Add external pulse stretching through a PLD while disabling on-chip pulse stretching through Register 20 (Register bit 20.1 = 0). This workaround requires external hardware and manageability through the MDIO interface. Also, because pulse stretching is global to the device, external logic must be added for any LED signal that requires stretching.
4. Display both transmit and receive status individually.

Status Fixed.

Item 8: MII Pins Not Three-Stateable

Problem In hardware power-down mode, the receive clock MDINT pins do not go into a high-impedance state or are not three-stated.

Implication In hardware power-down mode, the receive clock (RxClk) and the MDINT pins are continuously driven. The transmit clock will be in a true three-state condition. However, the LXT971A and LXT972A Transceivers continue to source a receive clock.

Workaround None.

Status Fixed.

Item 9: 100 M External Loopback Using Short Cable Length

Problem Link may not occur in applications requiring a short external looping plug (looping TPFO to TPFI) with cable lengths typically less than 2 feet.

Implication During external loopback operations requiring a line-loop length less than two feet, the LXT971A and LXT972A Transceivers input-receiver reference levels may incorrectly slice the twisted-pair signal, causing a loss of link.

Workaround None.

Status Fixed.

Item 10: 10BASE-T Data Inversion

Problem If jitter on the twisted-pair data occurs within a time window relative internally to the DPLL Reference Clock and remains constant, inverted RxData can occur.

Implication When the receive twisted-pair data jitters, the LXT971A and LXT972A Transceivers may pass errored data to the Reconciliation Sublayer. This errored data would be calculated as CRC errors at the MAC and the RXER signal/bit would be active.

Workaround None.

Status Fixed.

Item 11: Power Cycling and JTAG TRST Reset Pin

Problem Power-on cycling may cause the LXT971A and LXT972A Transceivers to hang in an unknown state due to the improper reset of some internal JTAG control flip-flops.

Implication Some internal JTAG flip-flops may not be reset properly, causing the input and output steering muxes to be selected incorrectly. This incorrect selection may disable any of the digital, MII signal outputs and inputs.

Workaround Designs not using JTAG should tie the TRST pin directly to GND.

Designs using the 5-signal option should tie the TRST pin to GND through a resistor. The suggested value for this resistor is 20 kΩ. A 20 kΩ resistor to GND is strong enough to pull down the internal, weak pull-up to a logic 0 for normal operation. This pull down also allows a JTAG tap controller to operate successfully and overcome the pull-up and pull-down resistors.

Designs using the 4-signal option and not using the TRST pin for reset should use a 20 kΩ pull-down resistor from TRST to GND and control the JTAG TRST pin, accordingly.

Designs using the LXT971A or LXT972A Transceivers require a new BSDL file that may be found on the Cortina website (www.cortina-systems.com).

Status Fixed.

Item 12: Switching Clocks from 100 Mbps to 10 Mbps Prior to End-of-Packet

Problem Switching clocks from 100 Mbps to 10 Mbps prior to the End-of-Packet (EOP), as the PLL transitions to its reset state, can cause the output to become random and unknown, and result in the corruption of the last nibble of the CRC in the receive packet.

Implication A CRC error occurs randomly on a small percentage of devices and can result in an error rate up to 10 ppm.

Workaround None.

Status Fixed.

Item 13: Changing Advertised Duplex While Link Is Up

Problem Writing to Register bits 4.9:5, which control duplex mode advertisement while link is up and auto-negotiation is enabled, immediately changes the PHY mode of operation to the new duplex mode. When written, the values in this register are not intended to affect PHY operation until a new auto-negotiation cycle is completed.

Implication A possible mixed-duplex operation will exist during the time between Register bits 4.9:5 writes and the start of a new auto-negotiation process.

Workaround Write Register bits 4.9:5 immediately before the start of a new auto-negotiation process.

Status No Fix.

Item 14: Far-End Fault Reporting

Problem If a link partner continuously sends successive Far-End Fault (FEF) codes (three sets of 84 1s followed by a 0), the LXT971A/LXT972A Transceiver sets the Remote Fault bit High (Register bit 1.4 = 1) and drops link (Register bit 1.2 = 0). Register 1.4 is cleared after a Read and is not set High again while the Far-End Fault signal is present.

Implication Implication: If the MAC reads Register bit 1.4 more than once under a continuous Far-End Fault condition, a Far-End Fault is not indicated after the first Read.

Workaround Once a remote fault has been indicated by Register bit 1.4 = 1, the following sequence can be used to monitor the remote-fault status.

Managed Systems:

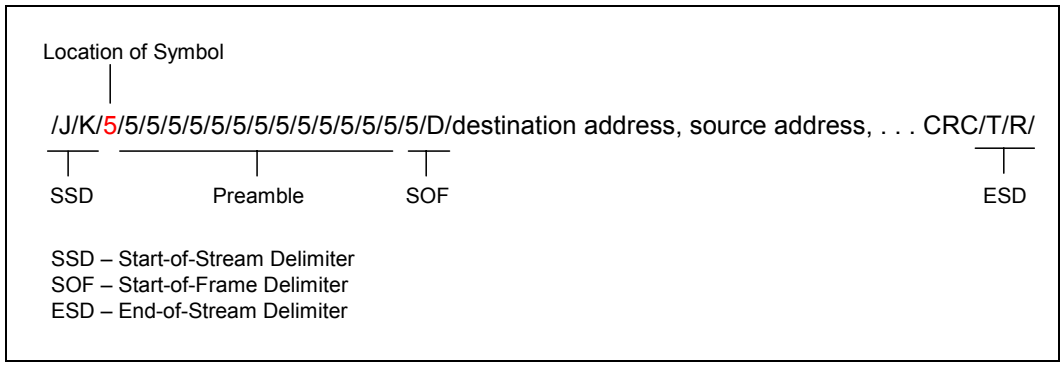
1. Write Register 0 = 0x6100. This forces the port to 100 Mbps full-duplex internal loopback, link is up, Register bit 1.2 = 1, and Register bit 1.4 = 0.
2. Wait approximately 100 mS.
3. Write Register 0 = 0x2100. This forces the port into 100 Mbps full-duplex. If Far-End Fault is present, Register bit 1.4 = 1 indicates Far-End Fault and Register bit 1.2 = 0 indicates link is down.

Status No Fix.

Item 15: Detection of Illegal Symbols After SSD

Problem An illegal symbol placed immediately after the SSD (preamble after JK) is not detected. However, any subsequent corrupt symbol will be detected.

Standard Frame Contents:



Implication RXER does not assert if this symbol location is corrupted. However, an error in this location does not affect packet integrity.

Workaround Use the MAC layer protocol to detect corrupt symbols in the packet.

Status No Fix.

6.0 Specification Changes

There are no specification changes.

7.0 Specification Clarifications

There are no specification clarifications.

8.0 Documentation Changes

There are no specification clarifications.

9.0 Ordering Information

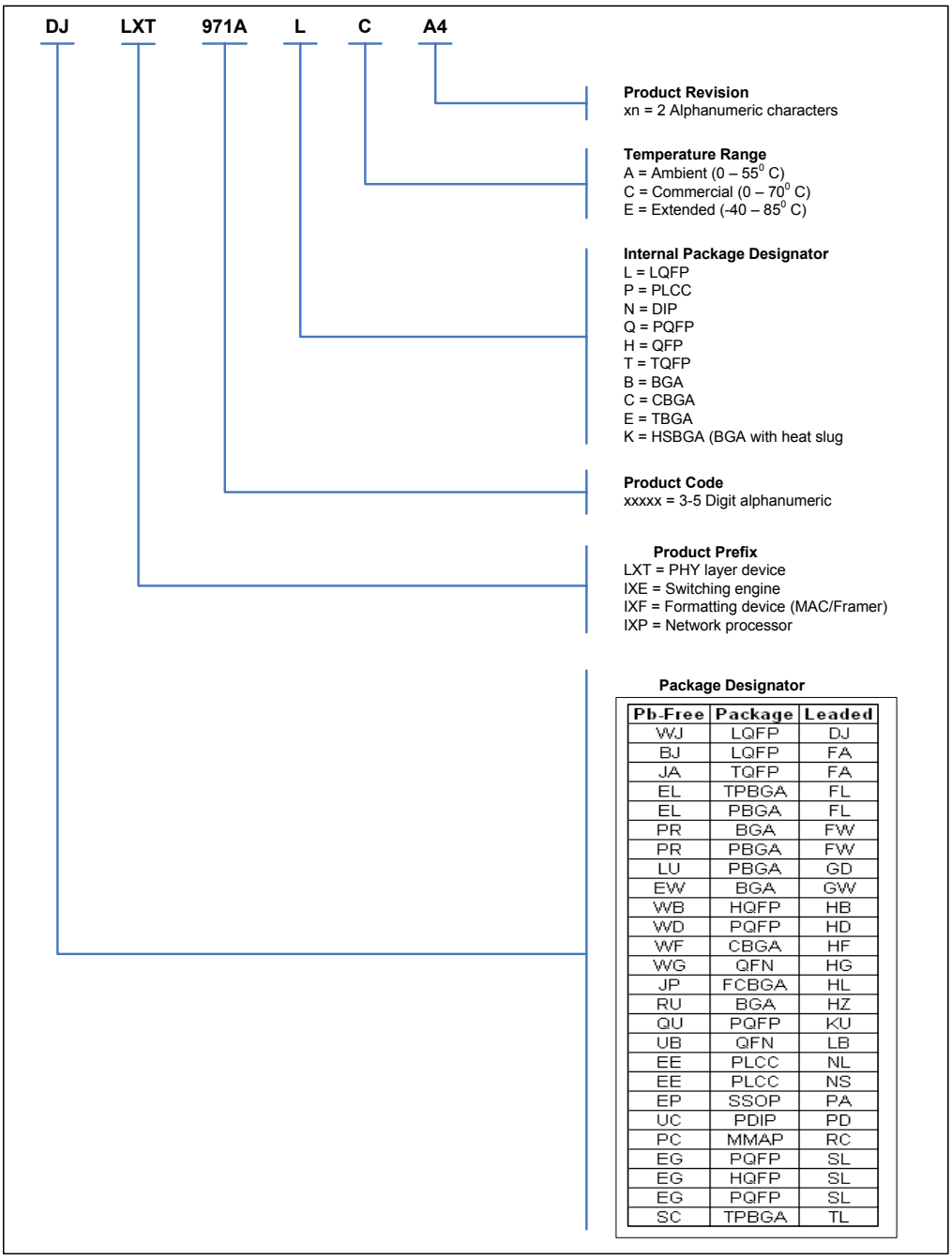
Change 1. Table 3 provides product ordering information.

Table 3 Product Ordering Information

Number	Revision	Package Type	Pin Count	RoHS Compliant
DJLXT971ALC.A4	A4	LQFP	64	No
DJLXT971ALE.A4	A4	LQFP	64	No
WJLXT971ALC.A4	A4	LQFP	64	Yes
WJLXT971ALE.A4	A4	LQFP	64	Yes
FLLXT971ABC.A4	A4	TPBGA	64	No
FLLXT971ABE.A4	A4	TPBGA	64	No
ELLXT971ABC.A4	A4	TPBGA	64	Yes
ELLXT971ABE.A4	A4	TPBGA	64	Yes
DJLXT972ALC.A4	A4	LQFP	64	No
DJLXT972MLC.A4	A4	LQFP	48	No
WJLXT972ALC.A4	A4	LQFP	64	Yes
WJLXT972MLC.A4	A4	LQFP	48	Yes

Change 2. The ordering information matrix changes as shown in Figure 10.

Figure 10 Ordering Information Matrix - Sample



Pb-Free	Package	Leaded
WJ	LQFP	DJ
BJ	LQFP	FA
JA	TQFP	FA
EL	TPBGA	FL
EL	PBGA	FL
PR	BGA	FW
PR	PBGA	FW
LU	PBGA	GD
EW	BGA	GW
WB	HQFP	HB
WD	PQFP	HD
WF	CBGA	HF
WG	QFN	HG
JP	FCBGA	HL
RU	BGA	HZ
QU	PQFP	KU
UB	QFN	LB
EE	PLCC	NL
EE	PLCC	NS
EP	SSOP	PA
UC	PDIP	PD
PC	MMAP	RC
EG	PQFP	SL
EG	HQFP	SL
EG	PQFP	SL
SC	TPBGA	TL

For additional product and ordering information:

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