

Low Skew Multiple Frequency PCI Clock Generator with EMI Reducing SSCG.

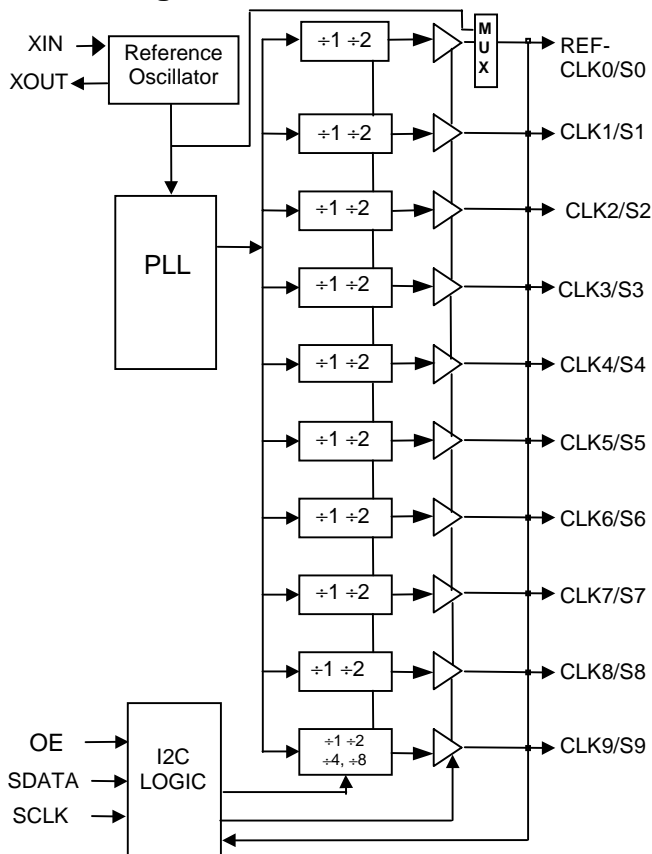
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Product Features

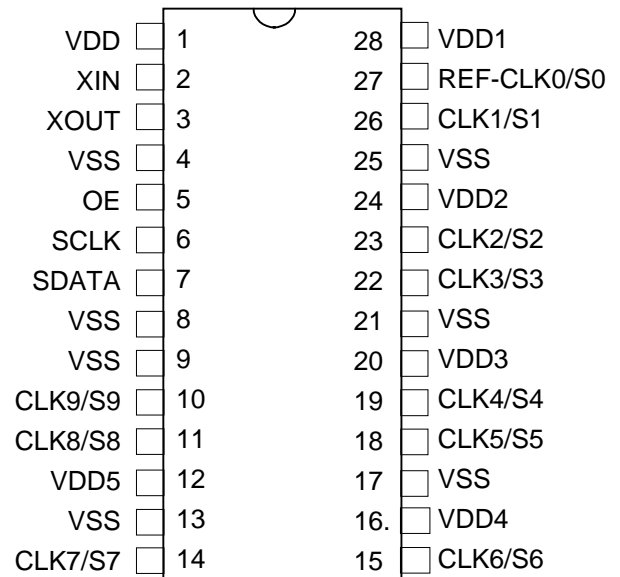
- Produces PCI output clocks that are individually selectable for 33.3 or 66.6 MHz under I²C or strapping control.
- Separate output buffer power supply for reduced noise, crosstalk and jitter.
- input clock frequency standard 14.31818 MHz
- Output clocks frequency individually selectable via I²C or hardware bi-directional pin strapping.
- SSCG EMI reduction at 1.0% width
- Individual clock disables via I²C control
- All output clocks skewed within a 500 pS window
- Cycle to Cycle jitter ± 250 pS
- Output duty cycle is automatically 50% ($\pm 10\%$) adjusted
- Clock feed through mode and OE pins for logic testing
- Glitchless clock enabling and disabling transitions
- 28-pin TSSOP or SSOP package

OE	CLK(0:9)	PLL
1 (HIGH)	Enabled	Running
0 (LOW)	Tri State	Running

Block Diagram



Pin Configuration



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Pin Description

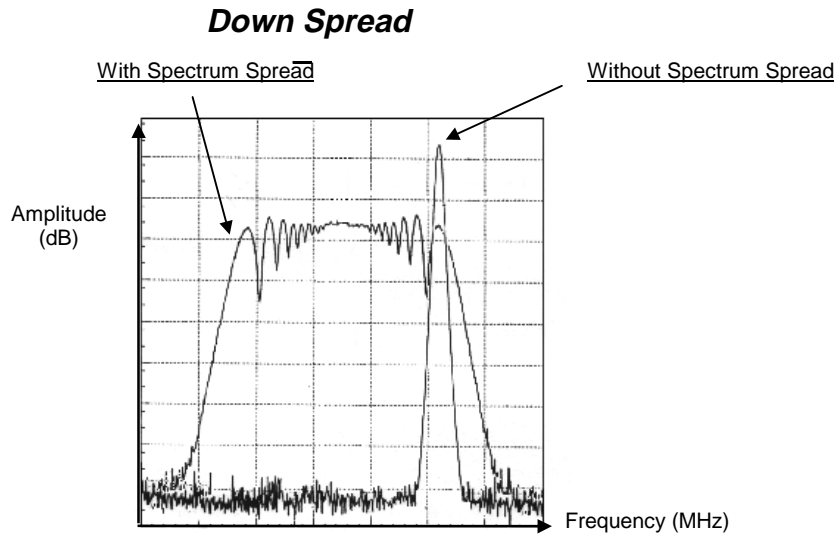
Pin Number	Pin Name	PWR	I/O	Description
2	XIN	VDDA	I	This pin is the connection point for the devices Loop reference frequency. This may be either a CMOS 3.3 volt reference clock or the output of an external crystal. A nominal 14.31818 MHz frequency must be supplied to obtain the frequencies listed on this data sheet
3	XOUT	VDDA	O	This pin the devices output drive that is to be used when an external crystal is used. In this configuration the device provides the analog gain function of a crystal oscillator. When the device is being supplied with an external reference frequency, this pin is left disconnected.
1	VDDA	-	PWR	This pin is the power supply source for the internal PLL circuitry and core control logic. It should be bypassed separately from all other device VDD supply pins.
5	OE	-	I	Output Enable. See logic table on page 1 for functionality
12, 16, 20, 24, 28	VDD	-	PWR	Logic power for All buffers
6	SDATA	VDDA	I/O	I ² C Serial data pin
7	SCLK	VDDA	O	I ² C serial interface clock pin
27	REF-CLK0/S0	VDD1	O	Individual output clocks and power up divisor select pins. Each of these pins is both a clock output pin and, at power up, a temporary input pin. When they act as an input pin they set the initial output frequency of the device to either the input frequency or half of the input frequency. Subsequently, the divisor may be changed or disabled via the device's I2C register bits. Reference clock and its programmable input value are saved internally for when it PCI clock function is selected.
26	CLK1/S1	VDD1	O	
23	CLK2/S2	VDD2	O	
22	CLK3/S3	VDD2	O	
19	CLK4/S4	VDD3	O	
18	CLK5/S5	VDD3	O	
15	CLK6/S6	VDD4	O	
14	CLK7/S7	VDD4	O	
11	CLK8/S8	VDD5	O	
10	CLK9/S9	VDD5	O	
4, 8, 9, 13, 17, 21, 25	VSS	-	PWR	Ground pins for the chip.
1	VDD	-	PWR	Power for core logic
28	VDD1	-	PWR	Power for CLK1 and CLK2 output buffers
24	VDD2	-	PWR	Power for CLK3 and CLK4 output buffers
20	VDD3	-	PWR	Power for CLK5 and CLK6 output buffers
16	VDD4	-	PWR	Power for CLK7 and CLK8 output buffers
12	VDD5	-	PWR	Power for CLK9 and CLK10 output buffers

A bypass capacitor (0.1 mF) should be placed as close as possible to each Vdd pin.

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Spectrum Spread Clocking



Spectrum Analysis

Spectrum Spreading Selection Table

Unspread Frequency in MHz	Down Spreading			
	F Min (MHz)	F Center (MHz)	F Max (MHz)	Spread (%)
Desired (actual)				
33.3 (xx.x)	33.00	33.16	33.3	+0 -1.00%
66.6 (xx.x)	66.00	66.33	66.6	+0 -1.00%

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Power Up Bi-Directional Pin Timing (all clock outputs)

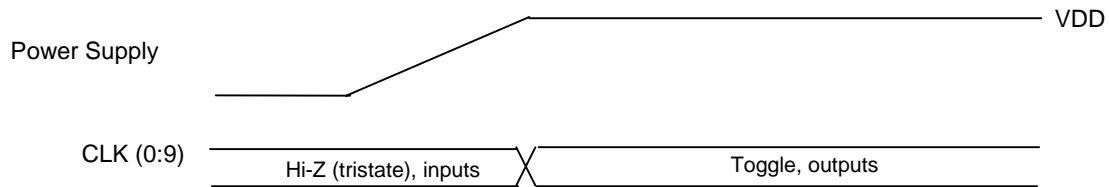


Fig.1

Note: a pull-up or logic high programming voltage will select a 66.6 MHz output clock frequency on that specific pin. A logic low level will select a 33.3 MHz clock frequency in that specific pin.

Output Frequency Selections

The device contains 3 specific output mode type pins. They are:

REF-CLK0/S0

This pin powers up as a 33.3 or 66.6 MHz PCI clock. Via I²C command byte 1 bit 4 it may be changed to be a 14.318 MHz PCI clock. When it is acting as a PCI clock its frequency may be changed between 33 and 66 MHz using I²C command byte 1 bit 3. The PCI clock may also be initially set at device power up using the bi-directional programming capability of the pin (device pin number 27)

CLK(1:8)

These are dual frequency PCI clock pins that may be stopped enabled and have their frequency changed at power up and then on the fly (at any time) via their respective I²C register control bits.

CLK9/S9

This bit acts in the same manner as the CLK (1:8) bits. Additionally by selection in I²C byte 3 Bits 5 and 6 it can output both 16.5 MHz or 8.25 MHz on its pin. Like the other clock pins I²C byte 3 Bit 6 is initially set (via the clocks bi-directional; pin function) at power up depending on the level of the clocks pin.

NOTE:

Clocks REF-CLK0/S0 (pin 27) and CLK1/S1 (pin 26) are powered from VDD1 (pin 28). This data sheet characterizes the guaranteed performance of these 2 clocks with respect to jitter and skew. Designers that use this device need to understand that if these 2 clocks are operated at different frequencies (i.e., pin 27 is set to the REF output mode while pin 26 is enabled at either 33 or 66 MHz frequency mode) that the data sheet values of these clocks will not be guaranteed. It is therefore prudent to disable the CLK1 output when the REF-CLK0/S0 output has been programmed to output a 14.31818 MHz clock to realize the devices best performance.

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Application Note for Selection on Bi-Directional Pins

Pins 10, 11, 14, 15, 18, 19, 22, 23, 26 and 27 are Power up bi-directional pins and are used for selecting power up output frequencies of this devices output clocks (see Pin description, Page 2). During power-up of the device, these pins are in input mode, therefore, they are considered input select pins internal to the IC, these pins have a large value pull-up each (250K Ω), therefore, a selection "1" is the default and will select a 66 MHz output frequency. If the system uses a slow power supply (over 5 ms settling time), then it is recommended to use an external pull-up (Rup) in order to insure a high selection. In this case, the designer may choose one of two configurations, see FIG. 3A and Fig. 3B.

Fig. 3A represents an additional pull up resistor 50K Ω connected from the pin to the power line, which allows a faster pull to a high level.

If a selection "0" is desired, then a jumper is placed on JP1 to a 5K Ω resistor as implemented as shown in Fig. 3A. Please note the selection resistors (Rup and Rdn) are placed before the Damping resistor (Rd) close to the pin.

Fig. 3B represents a single resistor 10K Ω connected to a 3-way jumper, JP2. When a "1" selection is desired, a jumper is placed between leads 1 and 3. When a "0" selection is desired, a jumper is placed between leads 1 and 2.

If the system power supply is fast (less than 5 mSec settling time), then Fig. 3A only applies and Pull up Rup resistor is not necessary.

The electrical length of the trace that connects the selection resistor to the devices pin should be kept as short as possible.

Input and Output Relationships

The device acts a PCI clock generator. Output clocks may be individually controlled to be either 33.3 or 66.6 MHz in frequency by setting or clearing the clocks respective I²C control register bit. All output clocks are rising edge aligned to within a shared 500 pS window. There is no specified relationship between the input reference clock and the output clocks.

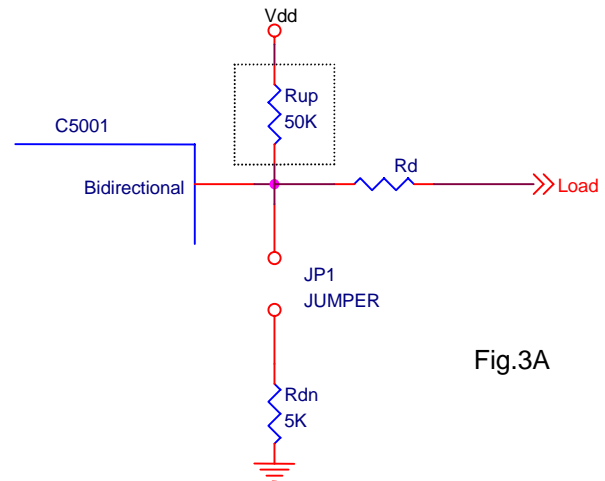


Fig.3A

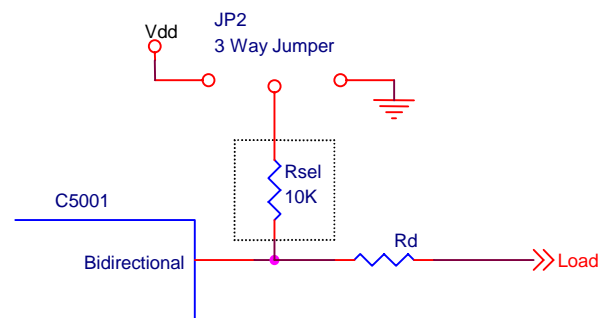


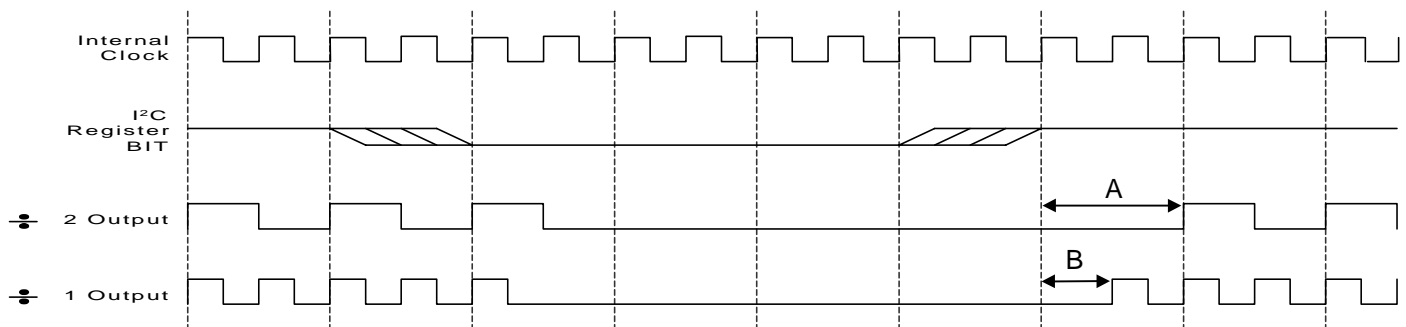
Fig.3B

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Clock Enable Functions and Timing

Each output clock may be either disabled or enabled by either setting or clearing its respective I²C register control bit. All clocks are stopped in the low state. All clocks maintain a valid high period before transitioning from running to stopped. The clocks transition between running and stopped occurs immediately after the I²C register bit is cleared and the clock transitions to a low state. See figure below.



A: represents one output ÷2 clock cycle (one 33.3 MHz cycle period).

B: represents one output clock ÷ 1 cycle (one 66.6 MHz cycle period)..

Output Frequency Change Relationships

The I²C registers are initially set (initialized) by the voltage levels present on the clocks output pins at power up. Subsequently these bits may be changed via I²C commands.

Output clocks have the capability to be changed, on the fly, via the devices I²C register bits. If Synchronous switching is required, it may be achieved by first disabling a specific clock, changing its frequency and then re-enabling it via the I²C register control bits that are provided for these functions.

Synchronous switching is defined as the changing of the output frequency of a clock from one frequency to another in such a manner as to not produce any clock cycles shorter than the higher of the 2 frequencies or longer than the period of the lower of the 2 frequencies. The disable and enable I²C register bit control of each clock is logically implemented to eliminate clock glitches when each clock is either disabled or enabled.

CAUTION: Switching clock frequencies without first disabling the clock may produce an output clock glitch (short or stretched period clock) during frequency transition!

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2-Wire I²C Control Interface

The 2-wire control interface implements write block mode write only slave interface. Sub addressing is not supported, thus all preceding bytes must be sent in order to read or change one of the control bytes. The 2-wire control interface allows each clock output to be individually controlled.

During normal data transfer, the SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit as the LSB (bit 0). Data is transferred MSB (bit 7) first.

The device will respond to writes up to 6 bytes (max) of data to address **D2**. The device will not respond to any other control interface conditions.

Serial Control Registers

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up.

Following the acknowledge of the Address Byte (D2), two additional bytes must be sent:

- 1) "**Command Code**" byte, and
- 2) "**Byte Count**" byte.

Although the data (bits) in these two bytes are considered "don't care"; they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the described sequence below (Byte 0, Byte 1, Byte2,) will be valid and acknowledged.

Byte 0: Function Select Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	14	CLK7 (Active = 1, Forced low = 0)
6	1	15	CLK6 (Active = 1, Forced low = 0)
5	1	18	CLK5 (Active = 1, Forced low = 0)
4	1	19	CLK4 (Active = 1, Forced low = 0)
3	1	22	CLK3 (Active = 1, Forced low = 0)
2	1	23	CLK2 (Active = 1, Forced low = 0)
1	1	26	CLK1 (Active = 1, Forced low = 0)
0	1	27	CLK0 (Active = 1, Forced low = 0)

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Serial Control Registers (Cont.)

Byte 1: Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	-	0= Test Mode (XIN replaces VCO output), 1=Normal
6	0	10	Bit 6 Bit 5 PCI9 Frequency -----
5	HW	10	0 0 33 MHz 0 1 66 MHz 1 0 16.5 MHz 1 1 8.25 MHz
4	0	27	REF-CLK0 mode (1 = REF, 0 = PCI0)
3	HW	27	CLK0 (33.3 MHz = 0, 66.6 MHz = 1)(if Byte 3 Bit 4=0)
2	0	-	SSCG (OFF = 0, ON = 1)
1	1	10	CLK9 (Active = 1, Forced low = 0)
0	1	11	CLK8 (Active = 1, Forced low = 0)

Byte 2: Clock Register (1 = 66.6 MHz, 0 = 33.3 MHz)

Bit	@Pup	Pin#	Description
7	HW	11	CLK8 (33.3 MHz = 0, 66.6 MHz = 1)
6	HW	14	CLK7 (33.3 MHz = 0, 66.6 MHz = 1)
5	HW	15	CLK6 (33.3 MHz = 0, 66.6 MHz = 1)
4	HW	18	CLK5 (33.3 MHz = 0, 66.6 MHz = 1)
3	HW	19	CLK4 (33.3 MHz = 0, 66.6 MHz = 1)
2	HW	22	CLK3 (33.3 MHz = 0, 66.6 MHz = 1)
1	HW	23	CLK2 (33.3 MHz = 0, 66.6 MHz = 1)
0	HW	26	CLK1 (33.3 MHz = 0, 66.6 MHz = 1)

Note: HW = Power up programmed via hardware (voltage at pin).

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Maximum Ratings

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	0°C to + 125°C
Operating Temperature:	0°C to +70°C
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

$$VSS < (V_{in} \text{ or } V_{out}) < VDD$$

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
VDD supply		3.0	-	3.6	Vdc	
Temperature		0		70	°C	
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL			-100	μA	
Input High Current	IIH			100	μA	
Tri-State leakage Current	Ioz	-	-	10	μA	
Dynamic Supply Current	Idd	-	-	150	mA	All outputs fully loaded at 30 pF @ 66 MHz
Static Supply Current		-	-	35	mA	All outputs driven low with I ² C control 66 MHz

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AC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input (REF) Duty Cycle	-	40	50	60	%	When external reference is used
REF input frequency	FREF	12	14.3	16	MHz	
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
Skew from any output to any output	tOFF _{CC}	0	200	500	pS	30 pF Load, Measured at 1.5V (all outputs fall within a 500 pSec time window)
Jitter Cycle to Cycle	t _{Jpp}	-250	-	+250	pS	Any Output
Output Freq.	F _O	30	33/66	70	MHz	At device output pins
Long term output jitter	t _{Jlt}	-500	-	+500	pS	Any output, 2 minute sample
Power up to output lock time	T _{VR} T _L	-	-	10	mS	Measured from the point VDD reaches 3.15 Volts with a stable reference
OE Rising to Output Lock Time	T _{OEL}	-	-	3	mS	Measured in a stabilized environment where OE has been previously brought to a logic low level.
Input Capacitance	CIN	-	-	4	pF	(FBIN and REF pins)
VDD = VDDA = 3.3V ±5%, TA = 0°C to +70°C						

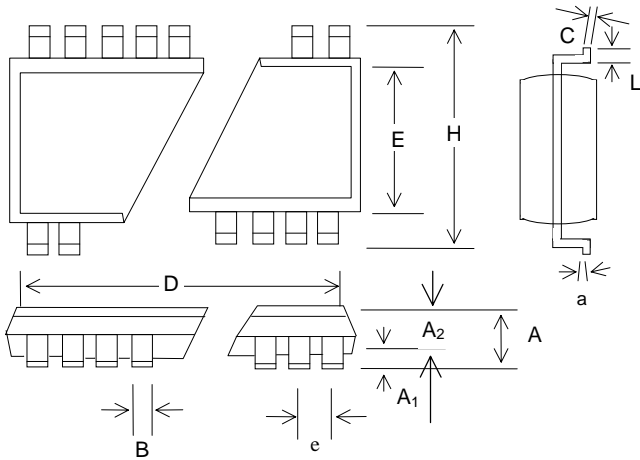
Buffer Characteristics (All Output Clocks)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH _{min}	22	-	-	mA	Vout = VDD - .5V
Pull-Up Current	IOH _{max}	-	-	-45	mA	Vout = 1.5V
Pull-Down Current	IOL _{min}	26	-	-	mA	Vout = 0.4V
Pull-Down Current	IOL _{max}	-	-	65	mA	Vout = 1.5V
Rise Time Min Between 0.4 V and 2.4 V	TR _{min}	0.4	-	2.5	nS	30 pF Load
VDD= VDDA = 3.3V ±5%, TA = 0°C to +70°C						

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Package Drawing and Dimensions



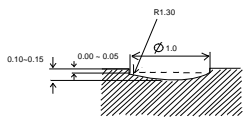
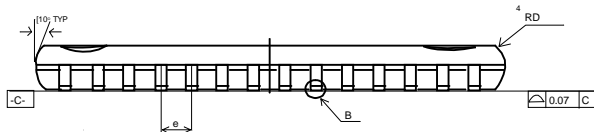
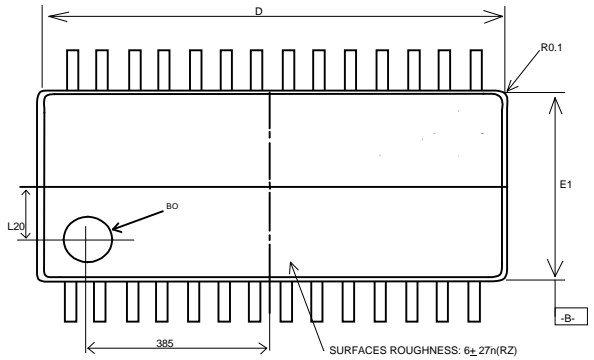
28 Pin SSOP Outline Dimensions

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.068	0.073	0.078	1.73	1.86	1.99
A ₁	0.002	0.005	0.008	0.05	0.13	0.21
A ₂	0.066	0.068	0.070	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.006	0.009	0.13	0.15	0.22
D	0.397	0.402	0.407	10.07	10.20	10.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.0256 BSC			0.65 BSC		
H	0.301	0.307	0.311	7.65	7.80	7.90
a	0°	4°	8°	0°	4°	8°
L	0.022	0.030	0.037	0.55	0.75	0.95

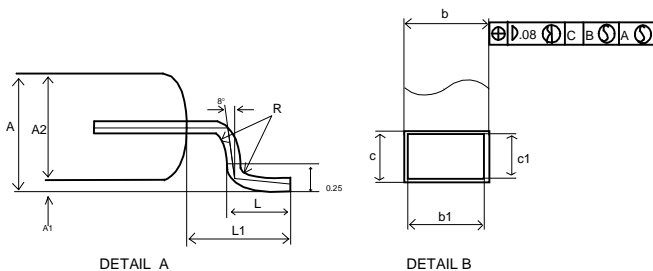
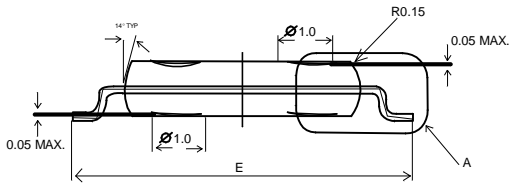
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Package Drawing and Dimensions (Cont.)



SECTION V-V



28 Pin TSSOP Dimensions

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A1	0.002	0.004	0.006	0.05	0.10	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
L	0.019	0.023	0.029	0.50	0.60	0.75
L1	0.035	0.039	0.043	0.90	1.00	1.10
b	0.007	-	0.011	0.19	-	0.30
b1	0.007	0.008	0.010	0.19	0.22	0.25
c	0.004	-	0.007	0.105	-	0.175
c1	0.004	0.005	0.006	0.105	0.125	0.145
θ	0°	-	8°	0°	-	8°
e	0.026 BSC			0.65 BSC		
D	0.378	0.382	0.386	9.6	9.7	9.8
E	0.244	0.252	0.260	6.2	6.4	6.6
E1	0.169	0.173	0.177	4.3	4.4	4.5
R	0.035	-	-	0.9	-	-

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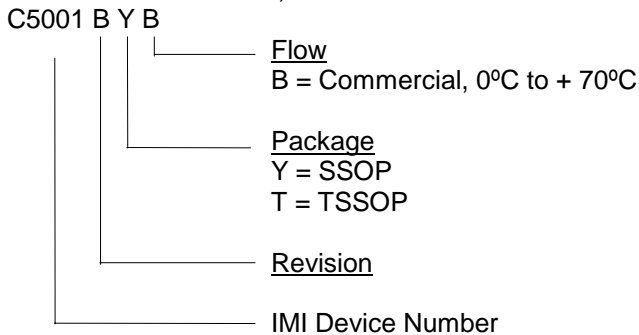
Ordering Information

Part Number	Package Type	Production Flow
C5001B	28 PIN TSSOP	Commercial, 0°C to +70°C
C5001B	28 PIN SSOP	Commercial, 0°C to +70°C

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI

C5001BYB
Date Code, Lot #



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