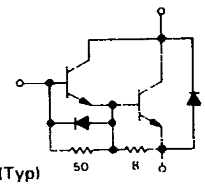
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUT35

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The BUT35 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

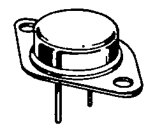
- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  550 nS Inductive Fall Time at 25°C (Typ)
  2.5 uS Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range −65 to 200°C



40 AMPERES
NPN SILICON POWER DARLINGTON TRANSISTORS
1000 VOLTS
250 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries – are given to facilitate "worst case" design.



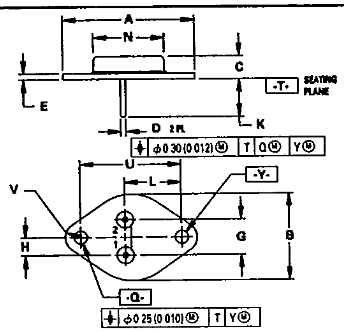
MAXIMUM RATINGS

Rating	Symbol	BUT35	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	Vdc
Collector Emitter Voltage 40°C	V_{CEV}	1000	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current Continuous Peak (1)	I_C I_{CM}	40 50	Adc
Base Current - Continuous - Peak (1)	I_B I_{BM}	10 20	Adc
Free Wheel Diode Forward current Continuous Peak	I_F I_{FM}	40 50	Adc
Total Power Dissipation @ T_C 25°C @ T_C - 100°C Derate above 25°C	P_D	250 140	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	65 to + 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purpose 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES.
1 DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982.
2. CONTROLLING DIMENSION. INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38 86 REF		1.530 REF	
B	25.15	26 67	0.990	1 050
C	6.35	8.25	0 250	0 325
D	1 45	1 60	0 057	0 063
E	1 53	1 77	0 060	0 070
G	10.92 BSC		0 430 BSC	
H	5 46 BSC		0.215 BSC	
K	11.18	12 19	0 440	0 480
L	16.89 BSC		0 665 BSC	
N	19.31	21 08	0 760	0 830
Q	3.84	4.19	0 151	0 165
U	30 15 BSC		1 187 BSC	
V	3 33	4.77	0 131	0 188

STYLE 1.
PIN 1. BASE
2 EMITTER
CASE. COLLECTOR

CASE 197A-02
TO-204AE
(TO-3)

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	700	–	–	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	–	0.2	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	–	4.0	
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)	I_{EBO}	–	–	350	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17		
ON CHARACTERISTICS (1)					
DC Current Gain	h_{FE}				
(I_C = 12 A, V_{CE} = 5 V)		30	–	–	
(I_C = 24 A, V_{CE} = 5 V)		15	–	–	
Collector Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 12 A, I_B = 0.6 A)		–	–	2.0	
(I_C = 24 A, I_B = 2.4 A)		–	–	3.0	
(I_C = 32 A, I_B = 3.2 A)		–	–	3.5	
(I_C = 40 A, I_B = 8 A)		–	–	5.0	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 12 A, I_B = 0.6 A)		–	–	2.5	
(I_C = 24 A, I_B = 2.4 A)		–	–	2.9	
(I_C = 32 A, I_B = 3.2 A)		–	–	3.3	
Diode Forward Voltage (I_F = 32 A)	V_f	–	–	4.0	Vdc

SWITCHING CHARACTERISTICS
Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	T_C 25°C	See Table 1	t_s	–	–	4.0	μs
Fall Time		I_C = 24 A	t_f	–	–	1.2	μs
Storage Time	T_C 100°C	I_{B1} = 2.4 A	t_s	–	2.8	–	μs
Fall Time		$V_{BE(off)}$ = 5 V	t_f	–	0.65	–	μs

(1) Pulse Test PW 300 μs, Duty Cycle ≤ 2%

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BUT35

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

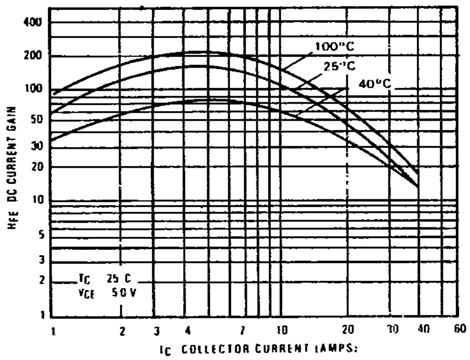

FIGURE 2 — COLLECTOR SATURATION REGION

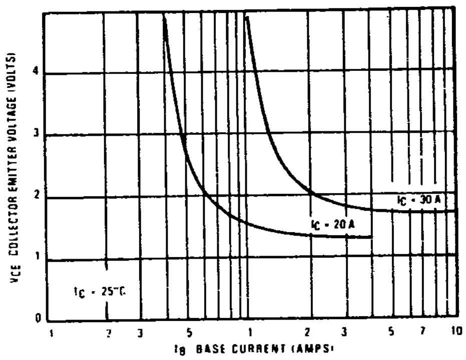

FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

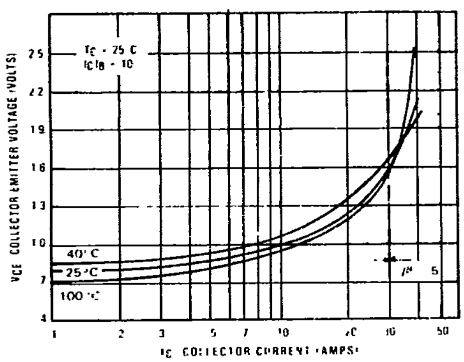

FIGURE 4 — BASE-EMITTER VOLTAGE

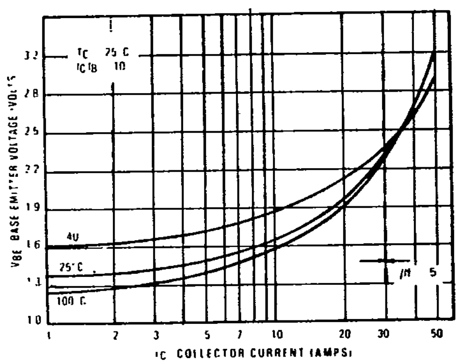

FIGURE 5 — THERMAL RESPONSE

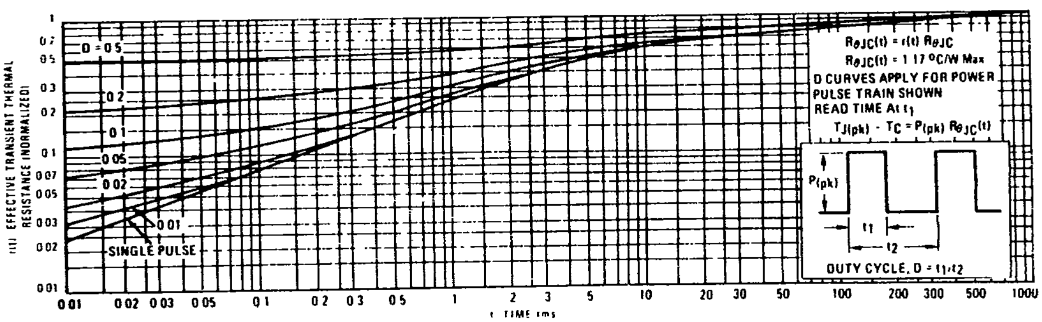

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TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

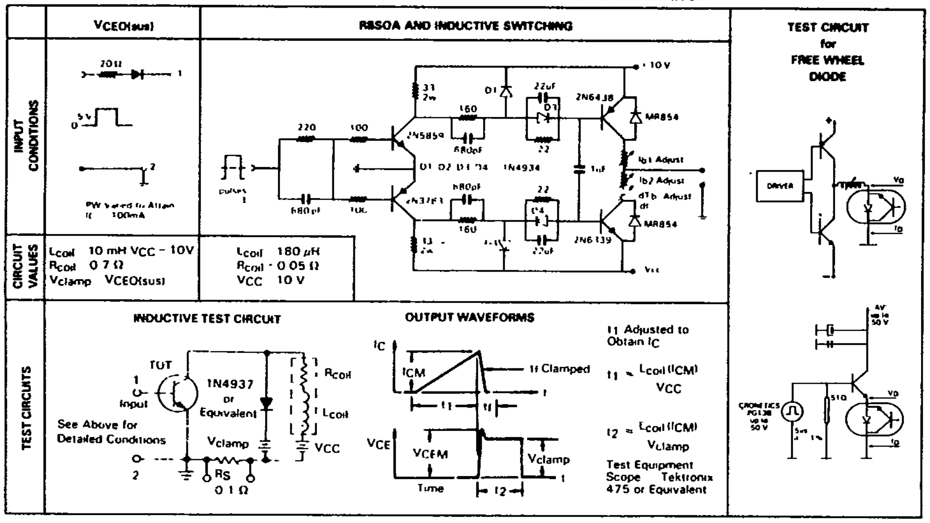


FIGURE 6 FALL TIME vs IB2/IB1

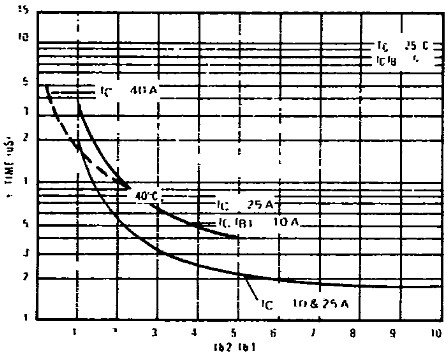


FIGURE 7 – TURN-OFF TIME vs IC

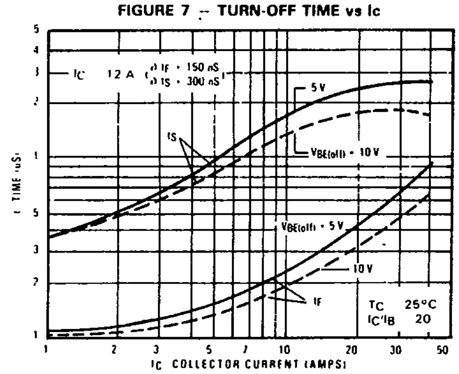


FIGURE 8 – STORAGE TIME vs FORCED GAIN

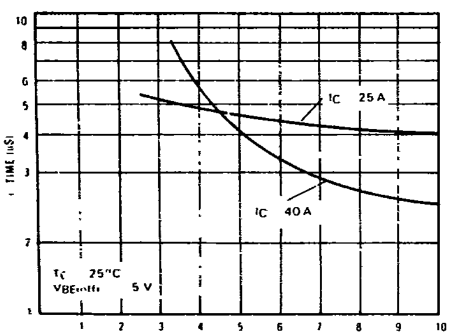
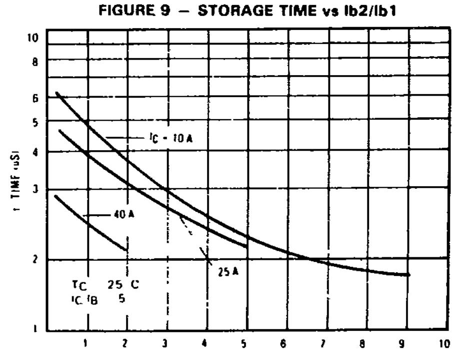


FIGURE 9 – STORAGE TIME vs Ib2/Ib1



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FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

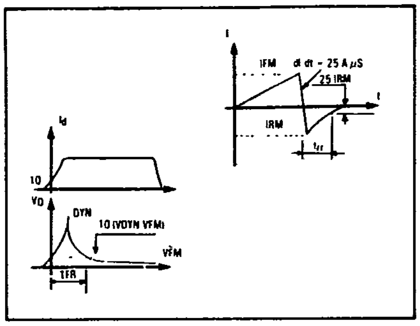

FIGURE 11 — FORWARD VOLTAGE

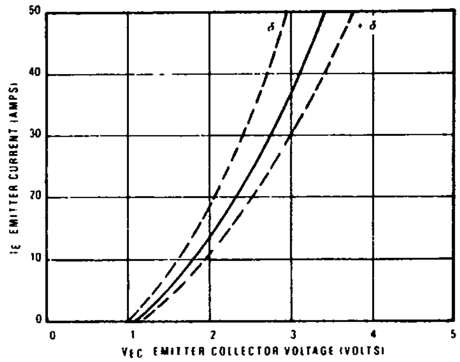

FIGURE 12 — FORWARD MODULATION VOLTAGE

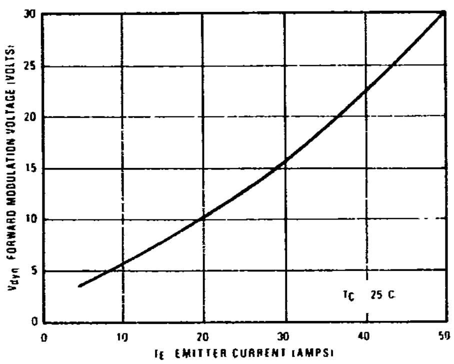

FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

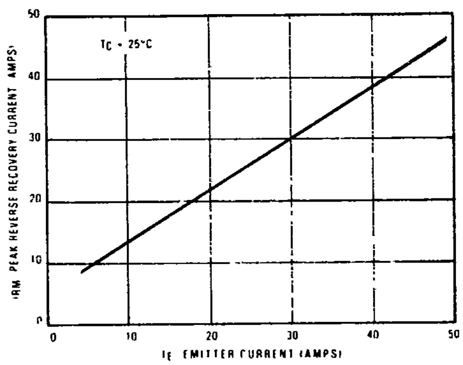

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FIGURE 14 — FORWARD RECOVERY TIME

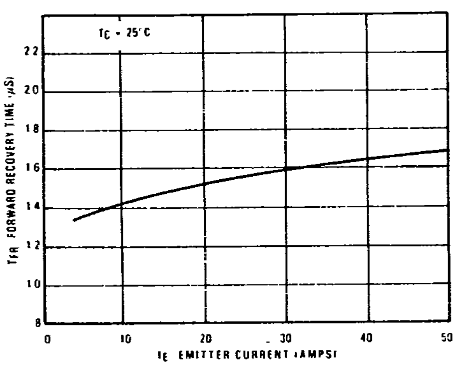
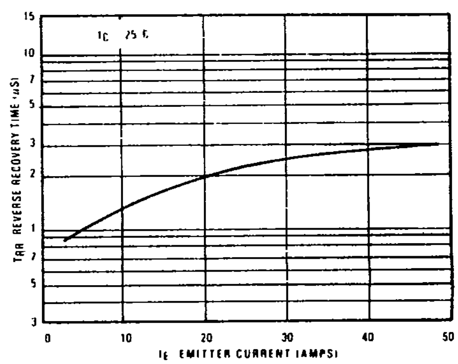


FIGURE 15 — REVERSE RECOVERY TIME



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The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

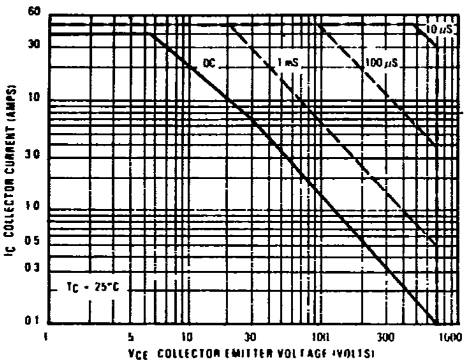
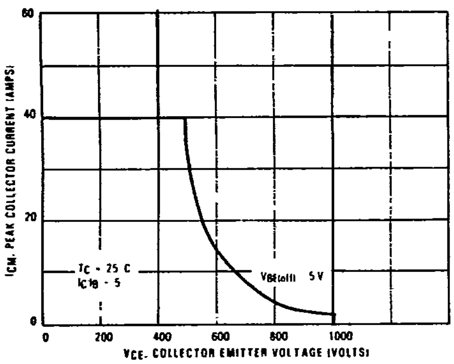


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to grater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

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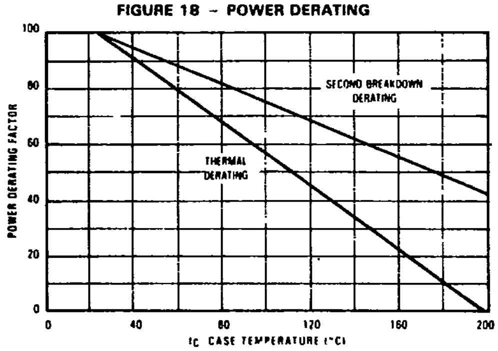
FIGURE 18 — POWER DERATING



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