

SMPS MOSFET IRFPS43N50K

HEXFET® Power MOSFET

Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

V_{DSS}	$R_{DS(on)}$ typ.	I_D
500V	0.078Ω	47A

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low $R_{DS(on)}$



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	47	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	29	
I_{DM}	Pulsed Drain Current ①	190	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	540	W
	Linear Derating Factor	4.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
	dv/dtPeak Diode Recovery dv/dt ③	9.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	910	mJ
I_{AR}	Avalanche Current①	—	47	A
E_{AR}	Repetitive Avalanche Energy①	—	54	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.23	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

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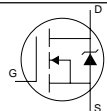
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.60	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.078	0.090	Ω	$V_{GS} = 10V, I_D = 28A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	250	μA	$V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	23	—	—	S	$V_{DS} = 50V, I_D = 28A$
Q_g	Total Gate Charge	—	—	350	nC	$I_D = 47A$ $V_{DS} = 400V$ $V_{GS} = 10V$, See Fig. 6 and 13 ④
Q_{gs}	Gate-to-Source Charge	—	—	85		
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	180		
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	$V_{DD} = 250V$ $I_D = 47A$ $R_G = 1.0\Omega$ $V_{GS} = 10V$, See Fig. 10 ④
t_r	Rise Time	—	140	—		
$t_{d(off)}$	Turn-Off Delay Time	—	55	—		
t_f	Fall Time	—	74	—		
C_{iss}	Input Capacitance	—	8310	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Output Capacitance	—	960	—		
C_{riss}	Reverse Transfer Capacitance	—	120	—		
C_{oss}	Output Capacitance	—	10170	—		
C_{oss}	Output Capacitance	—	240	—		
C_{oss}	Output Capacitance	—	240	—		
$C_{oss\ eff.}$	Effective Output Capacitance	—	440	—		

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	47	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	190		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 47A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	620	940	ns	$T_J = 25^\circ\text{C}, I_F = 47A$
Q_{rr}	Reverse Recovery Charge	—	14	21	μC	$di/dt = 100A/\mu s$ ④
I_{RRM}	Reverse Recovery Current	—	38	—	A	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.82\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 47A$ (See Figure 12a).
- ③ $I_{SD} \leq 47A$, $di/dt \leq 230A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$.
- ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss\ eff.}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

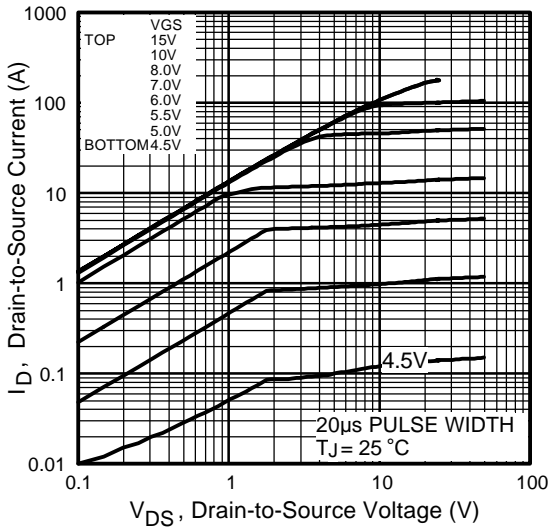


Fig 1. Typical Output Characteristics

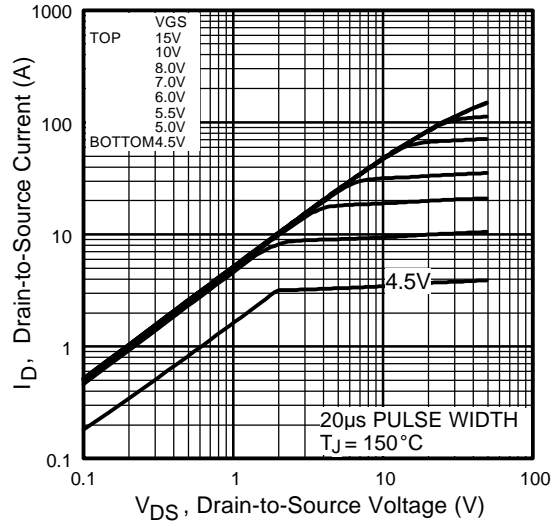


Fig 2. Typical Output Characteristics

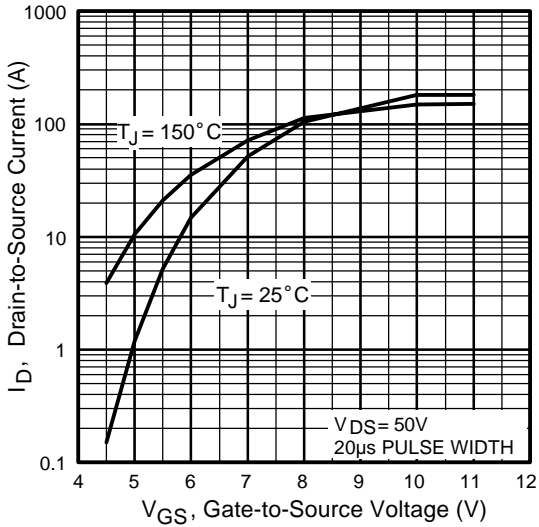


Fig 3. Typical Transfer Characteristics

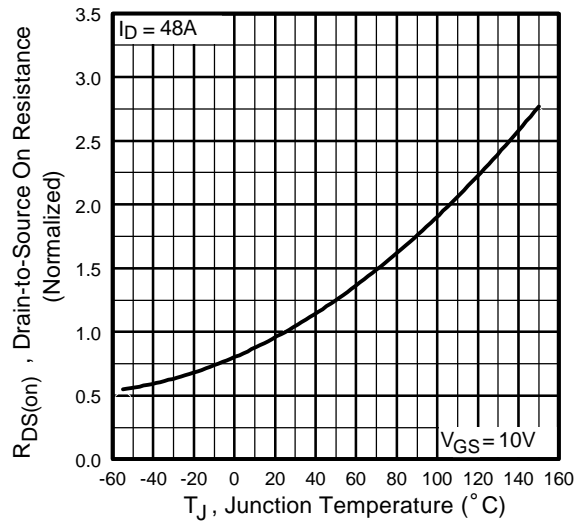


Fig 4. Normalized On-Resistance Vs. Temperature

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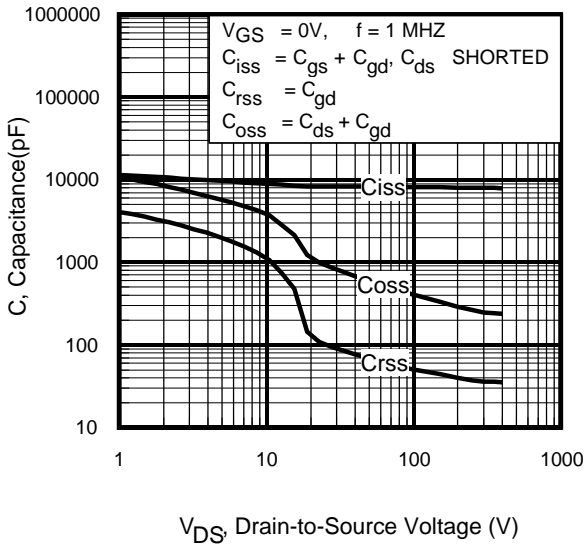


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

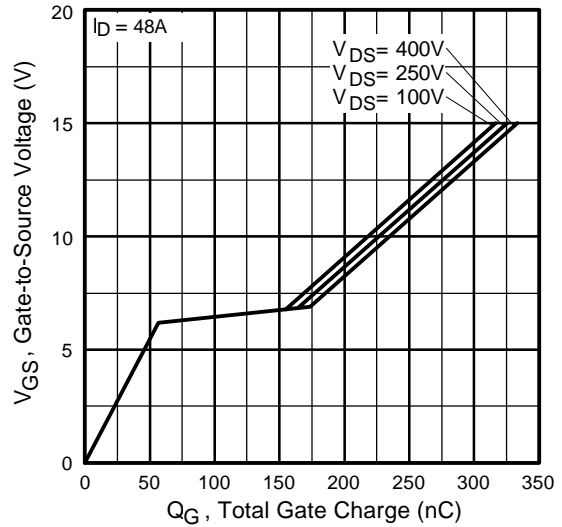


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

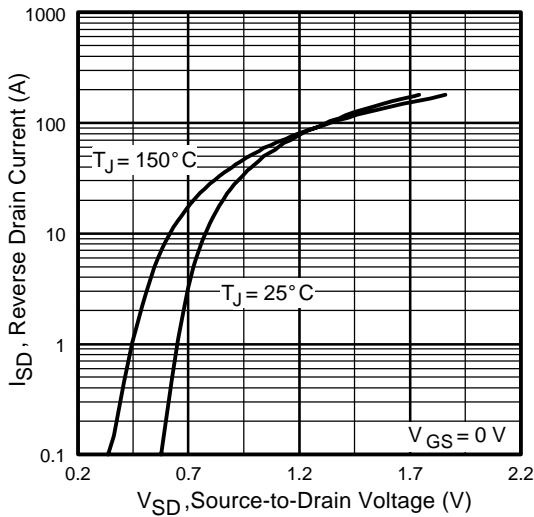


Fig 7. Typical Source-Drain Diode Forward Voltage

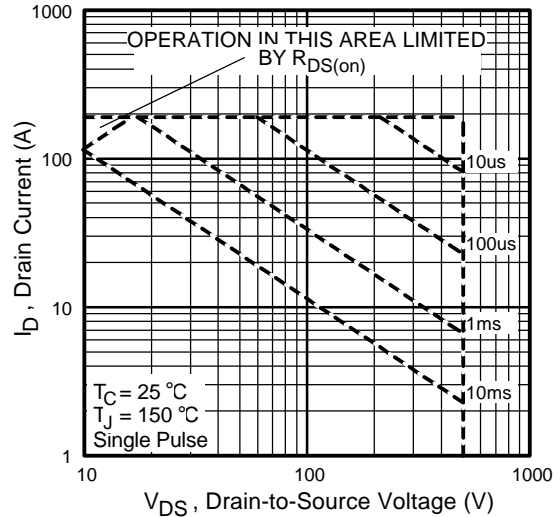


Fig 8. Maximum Safe Operating Area

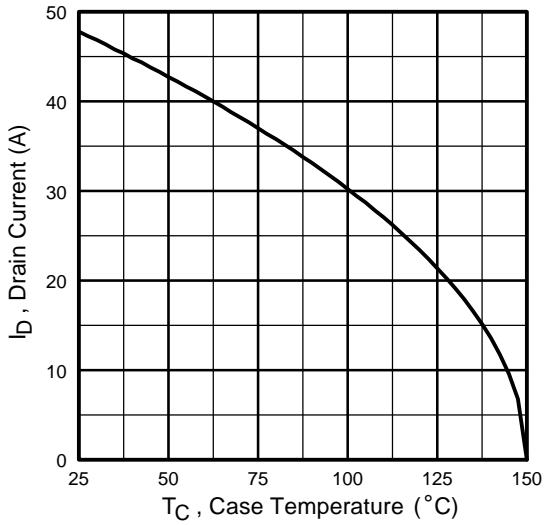


Fig 9. Maximum Drain Current Vs. Case Temperature

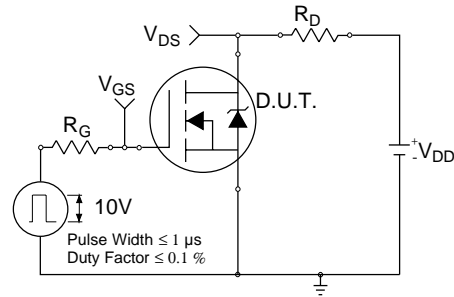


Fig 10a. Switching Time Test Circuit

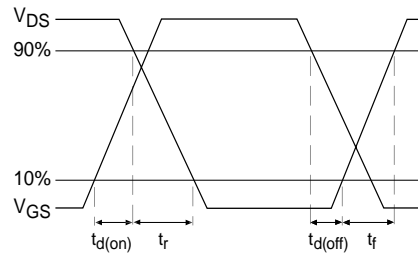


Fig 10b. Switching Time Waveforms

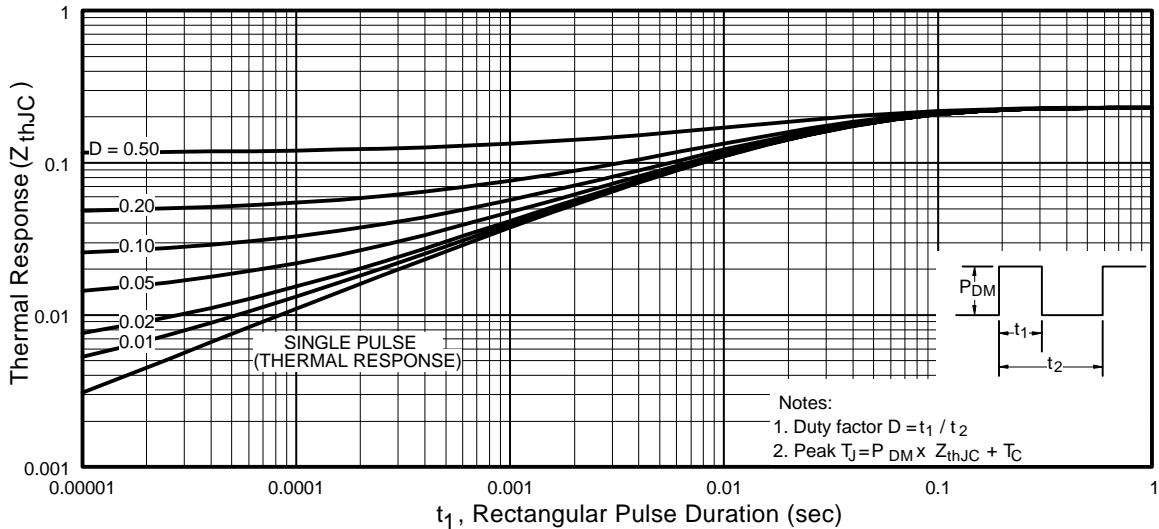


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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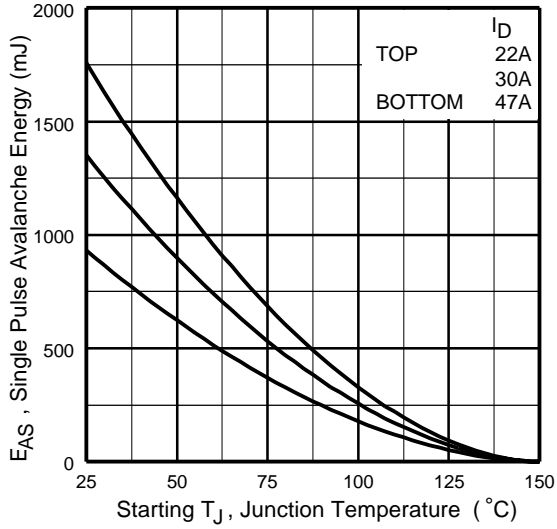


Fig 12a. Maximum Avalanche Energy Vs. Drain Current

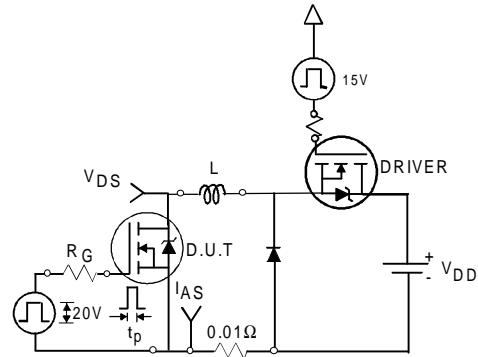


Fig 12c. Unclamped Inductive Test Circuit

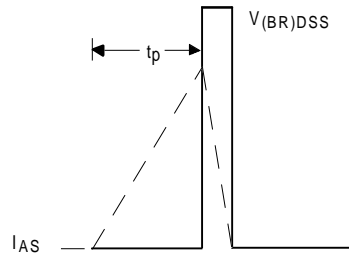


Fig 12d. Unclamped Inductive Waveforms

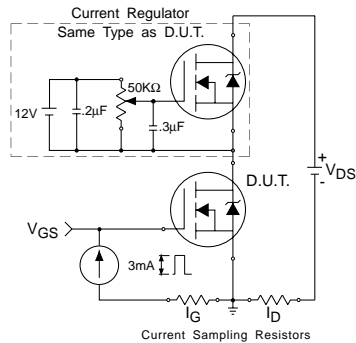


Fig 13a. Gate Charge Test Circuit

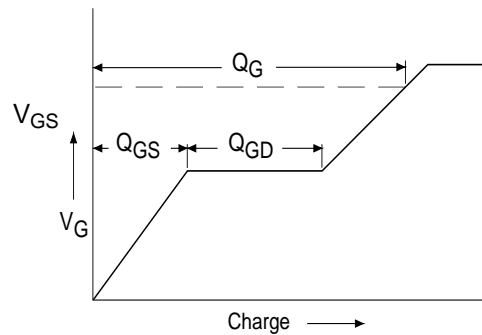
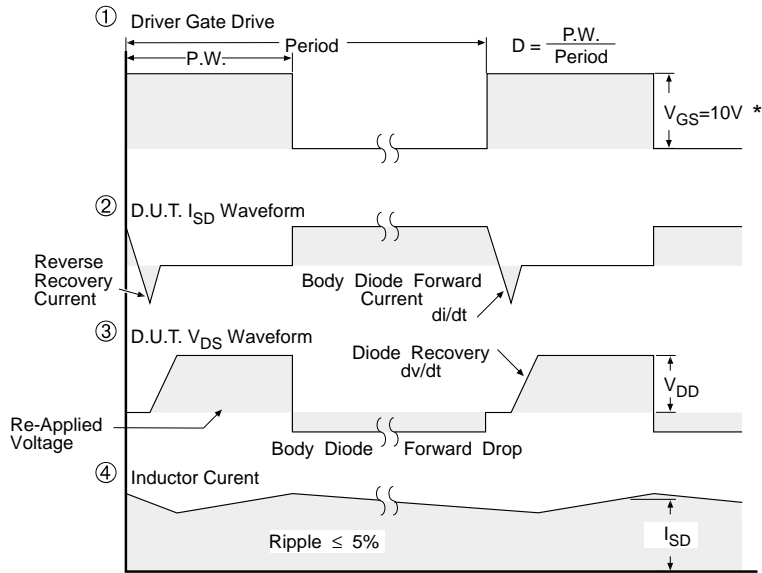
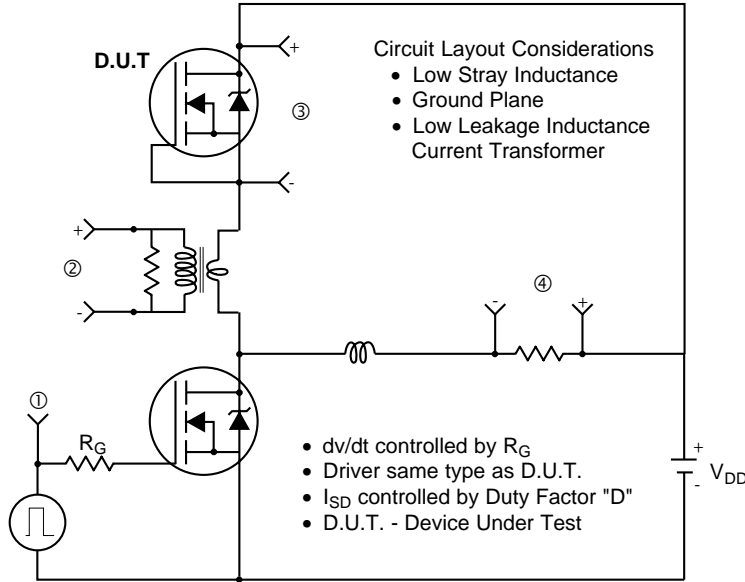


Fig 13b. Basic Gate Charge Waveform

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

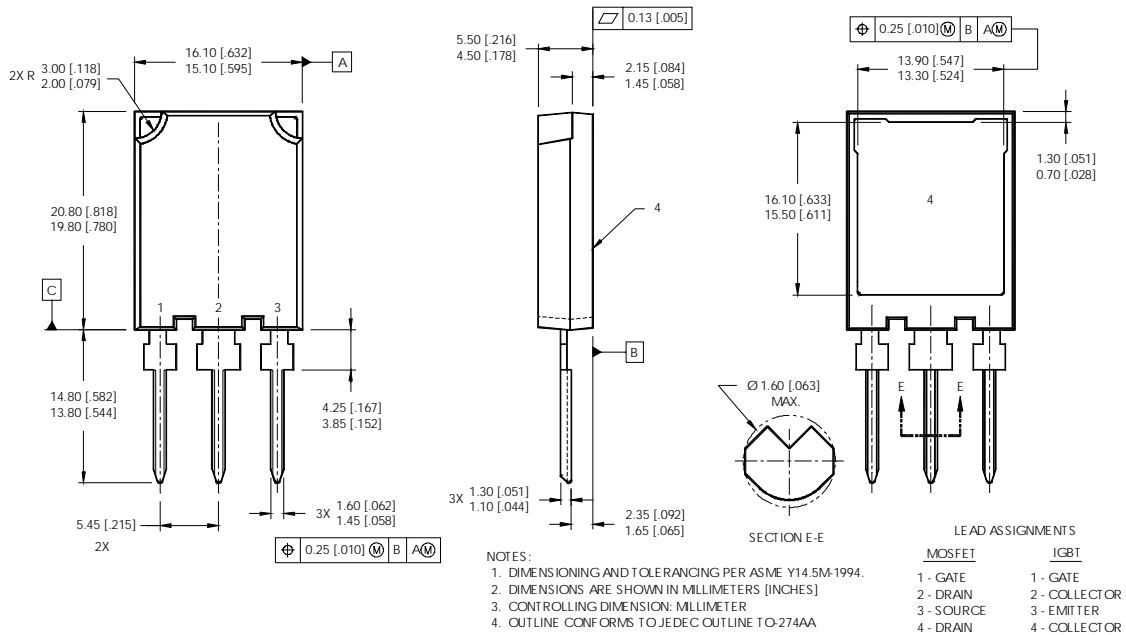
Fig 14. For N-Channel HEXFET® Power MOSFETs

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SUPER -247AC Package Outline

Dimensions are shown in millimeters (inches)



Data and specifications subject to change without notice.
 This product has been designed and qualified for the industrial market.
 Qualification Standards can be found on IR's Web site.

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