



## N-Channel Depletion-Mode Vertical DMOS FETs

### Ordering Information

BV <sub>DSX</sub> / BV <sub>DGX</sub>	R <sub>DS(ON)</sub> (max)	I <sub>DSS</sub> (min)	Order Number / Package		
			TO-92	TO-243AA*	Die
450V	20Ω	200mA	DN3545N3	DN3545N8	DN3545ND

\* Same as SOT-89. Product shipped on 2000 piece carrier tape reels.

Product marking for TO-243AA:

**DN5M\***

Where \* = 2-week alpha date code

### Features

- High input impedance
- Low input capacitance
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage

### Applications

- Normally-on switches
- Solid state relays
- Converters
- Constant current sources
- Power supply circuits
- Telecom

### Absolute Maximum Ratings

Drain-to-Source Voltage	BV <sub>DSX</sub>
Drain-to-Gate Voltage	BV <sub>DGX</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

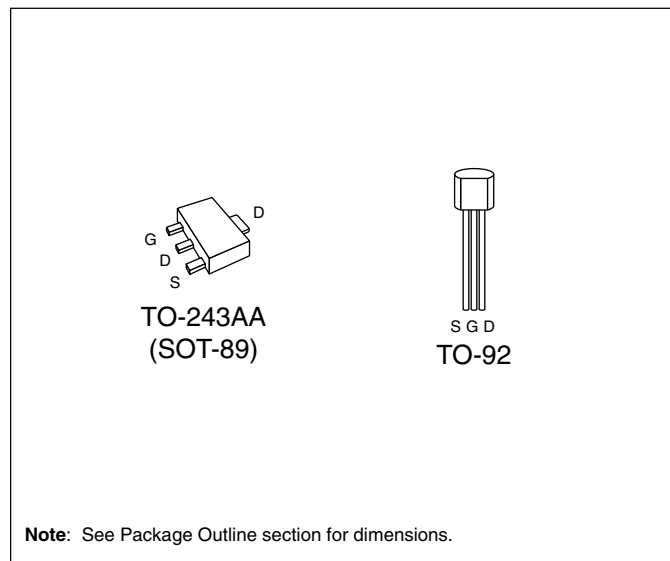
\* Distance of 1.6 mm from case for 10 seconds.

### Advanced DMOS Technology

These depletion-mode (normally-on) transistors utilize an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Options



## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)	Power Dissipation @ $T_A = 25^\circ\text{C}$	$\theta_{jc}$ $^\circ\text{C/W}$	$\theta_{ja}$ $^\circ\text{C/W}$	$I_{DR}^*$	$I_{DRM}$
TO-92	136mA	1.6A	0.74W	125	170	136mA	1.6A
TO-243AA	200mA	300mA	1.6†	15	78†	200mA	300mA

\*  $I_D$  (continuous) is limited by max rated  $T_j$ .

† Mounted on FR4 board, 25mm x 25mm x 1.57mm. Significant  $P_D$  increase possible on ceramic substrate.

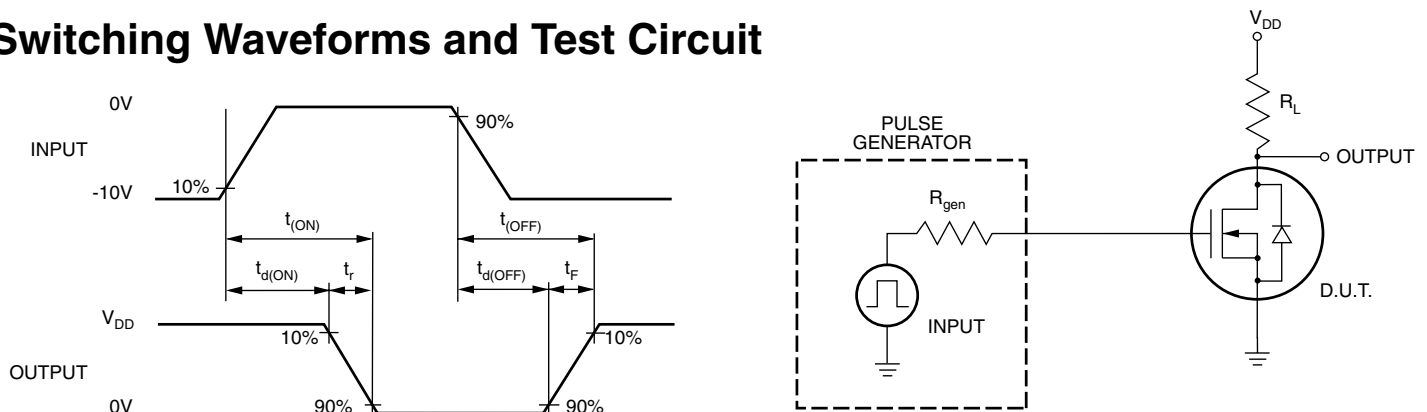
## Electrical Characteristics (@ $25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSX}$	Drain-to-Source Breakdown Voltage	450			V	$V_{GS} = -5V, I_D = 100\mu\text{A}$
$V_{GS(OFF)}$	Gate-to-Source OFF Voltage	-1.5		-3.5	V	$V_{DS} = 25V, I_D = 10\mu\text{A}$
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with Temperature			4.5	mV/ $^\circ\text{C}$	$V_{DS} = 25V, I_D = 10\mu\text{A}$
$I_{GSS}$	Gate Body Leakage Current			100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
$I_{D(OFF)}$	Drain-to-Source Leakage Current			1.0	$\mu\text{A}$	$V_{GS} = -5V, V_{DS} = \text{Max Rating}$
				1.0	mA	$V_{GS} = -5V, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{DSS}$	Saturated Drain-to-Source Current	200			mA	$V_{GS} = 0V, V_{DS} = 15V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			20	$\Omega$	$V_{GS} = 0V, I_D = 150\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.1	%/ $^\circ\text{C}$	$V_{GS} = 0V, I_D = 150\text{mA}$
$G_{FS}$	Forward Transconductance	150			$\text{m}\bar{\Omega}$	$I_D = 100\text{mA}, V_{DS} = 10V$
$C_{ISS}$	Input Capacitance			360	pF	$V_{GS} = -5V, V_{DS} = 25V$ $f = 1 \text{ MHz}$
$C_{OSS}$	Common Source Output Capacitance			40		
$C_{RSS}$	Reverse Transfer Capacitance			15		
$t_{d(ON)}$	Turn-ON Delay Time			20	ns	$V_{DD} = 25V,$ $I_D = 150\text{mA},$ $R_{GEN} = 25\Omega,$ $V_{GS} = 0V \text{ to } -10V$
$t_r$	Rise Time			30		
$t_{d(OFF)}$	Turn-OFF Delay Time			30		
$t_f$	Fall Time			40		
$V_{SD}$	Diode Forward Voltage Drop			1.8	V	$V_{GS} = -5V, I_{SD} = 150\text{mA}$
$t_{rr}$	Reverse Recovery Time		800		ns	$V_{GS} = -5V, I_{SD} = 150\text{mA}$

### Notes:

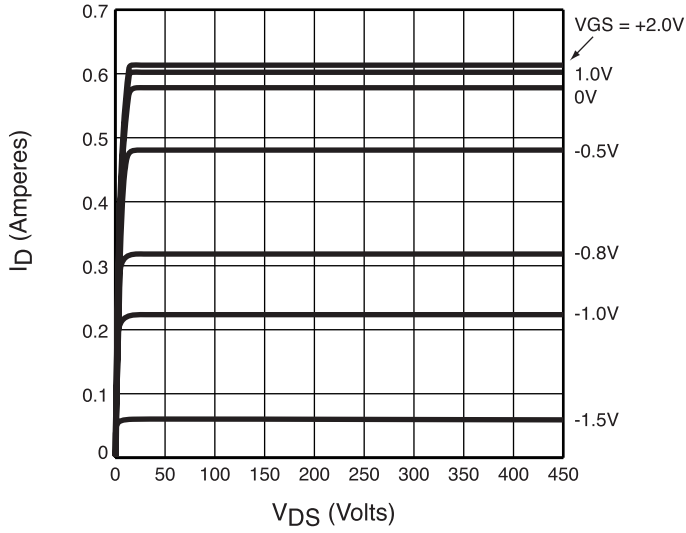
- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

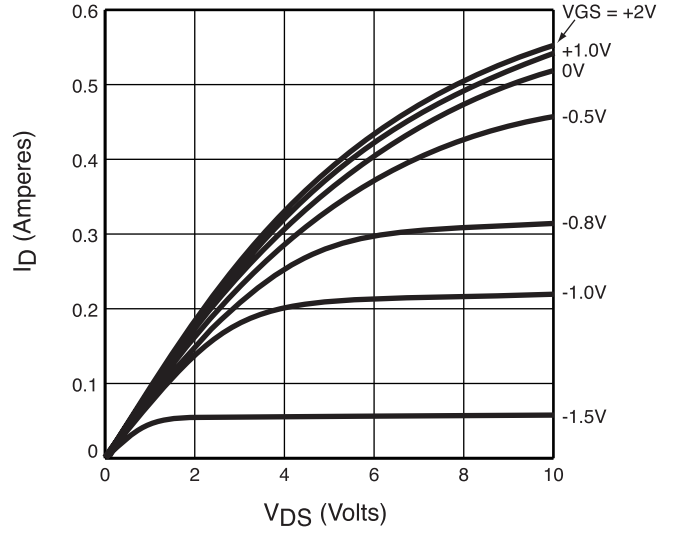


# Typical Application Curves

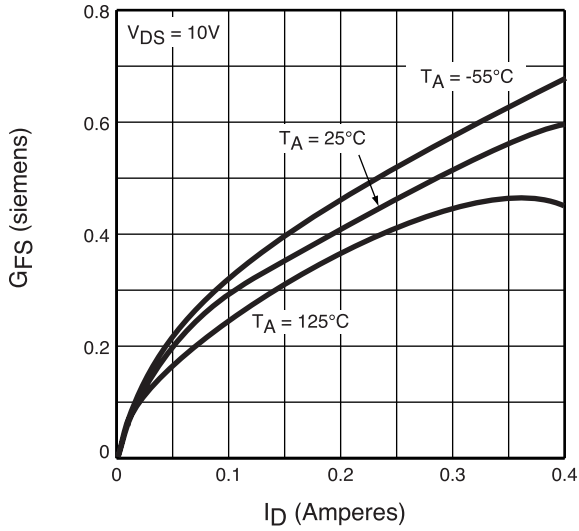
Output Characteristics



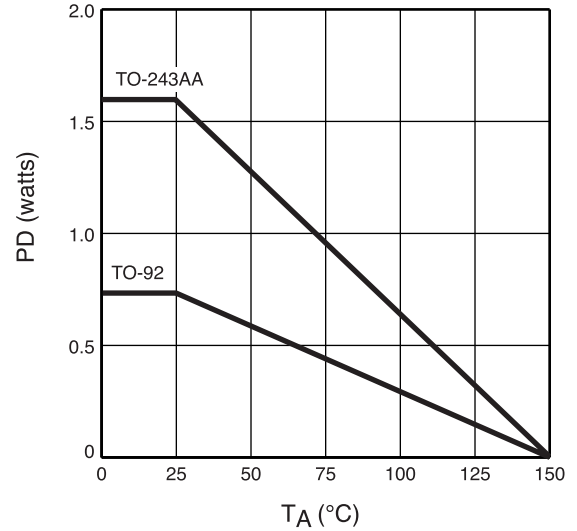
Saturation Characteristics



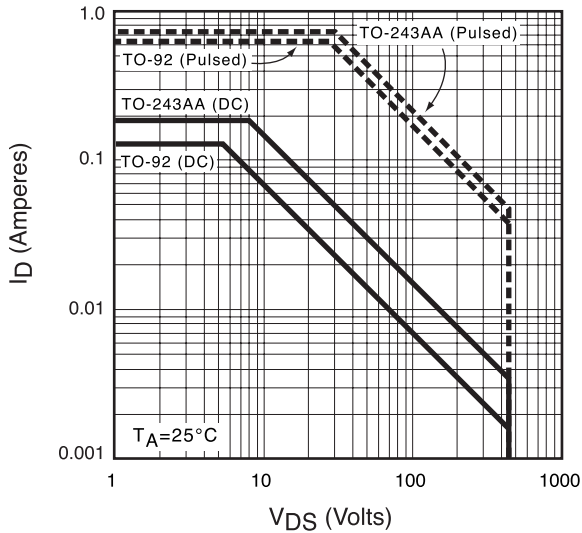
Transconductance vs. Drain Current



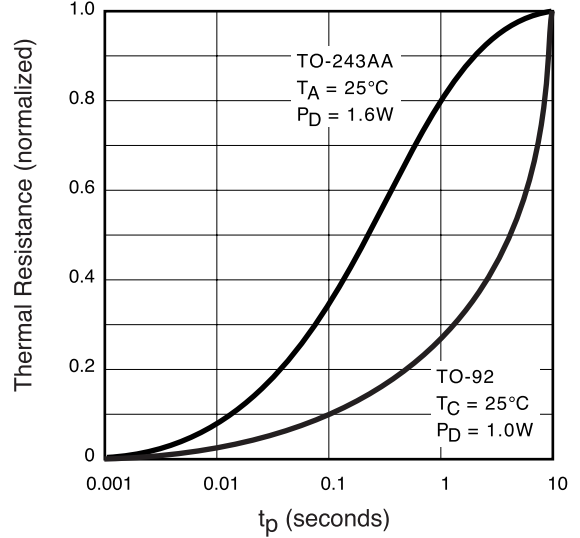
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area

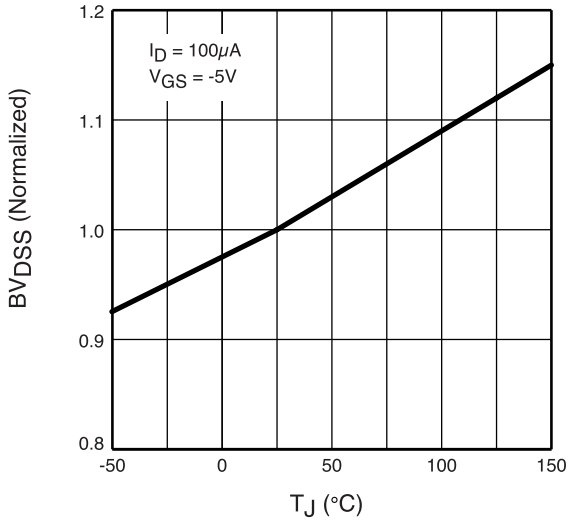


Thermal Response Characteristics

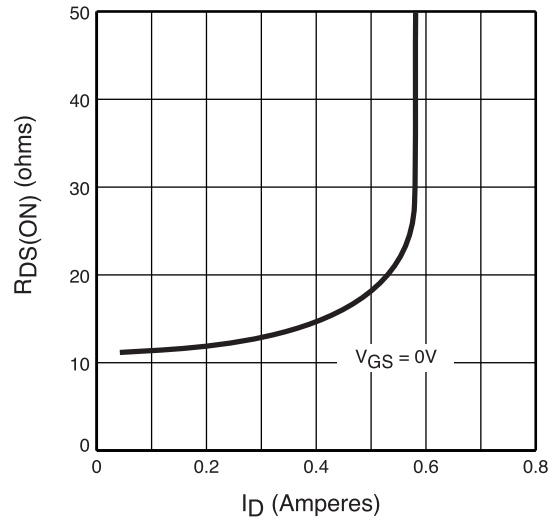


# Typical Application Curves

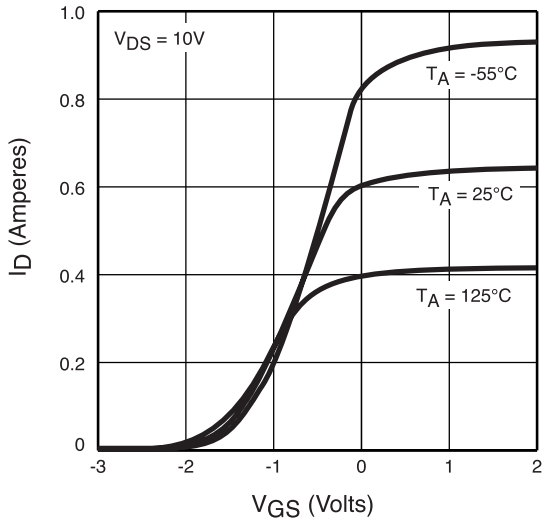
BV<sub>DSS</sub> Variation with Temperature



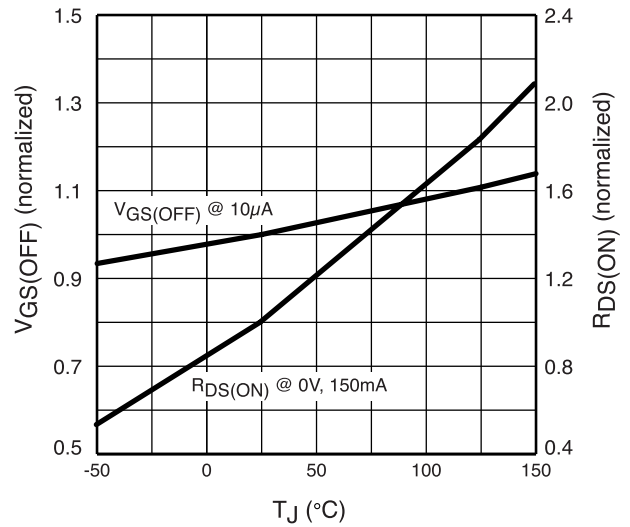
On Resistance vs. Drain Current



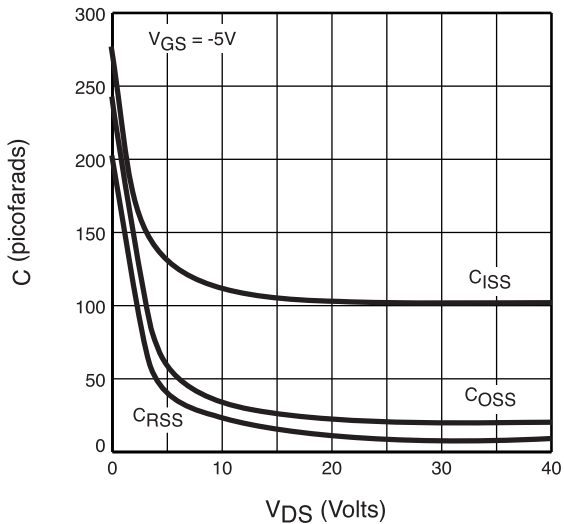
Transfer Characteristics



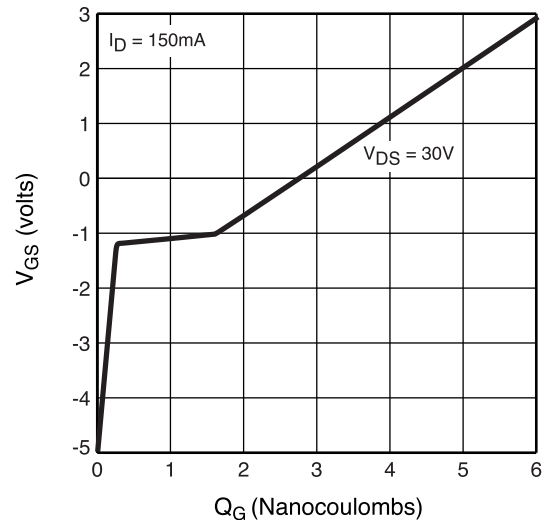
V<sub>GS(OFF)</sub> and R<sub>DS(ON)</sub> w/ Temperature



Capacitance vs. Drain Source Voltage



Gate Drive Dynamic Characteristics



12/13/010



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