PROCESS **CP147**

Central™ Semiconductor Corp.

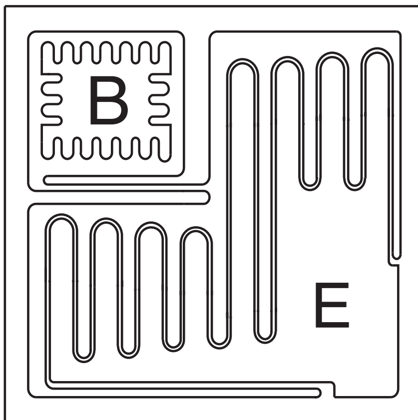
Power Transistor

NPN - Darlington Chip

PROCESS DETAILS

Process	EPITAXIAL BASE
Die Size	195 X 195 MILS
Die Thickness	12 MILS
Base Bonding Pad Area	29 X 29 MILS
Emitter Bonding Pad Area	61 X 35 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Ti/Ni/Au - Ni-6,000Å; Au-6,000Å

GEOMETRY



BACKSIDE COLLECTOR R0

GROSS DIE PER 5 INCH WAFER

280

PRINCIPAL DEVICE TYPES

MJ11012 2N6282
MJ11014 2N6283
MJ11016 2N6284

145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
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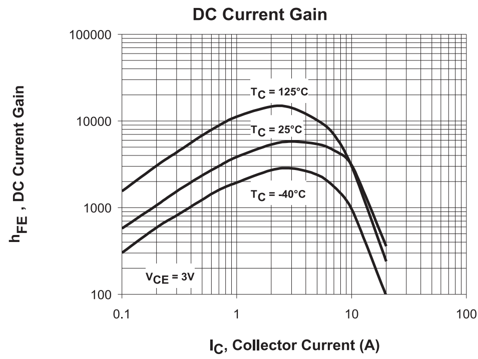
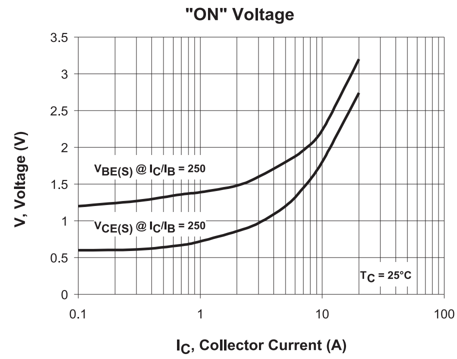
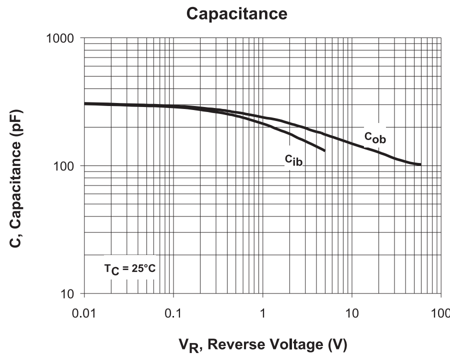
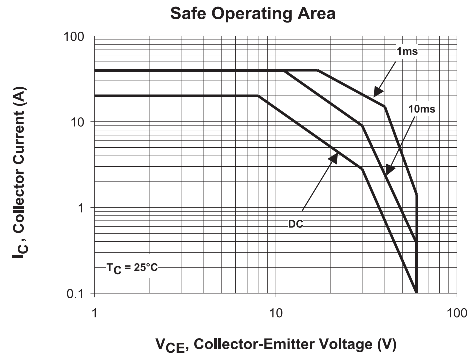
PROCESS CP147

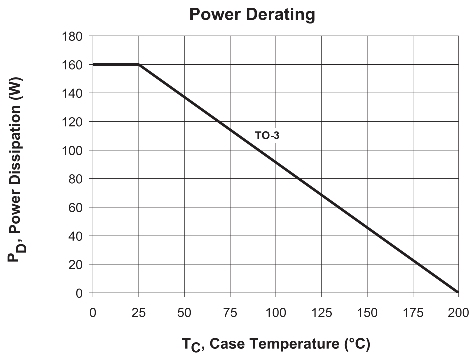
Typical Electrical Characteristics

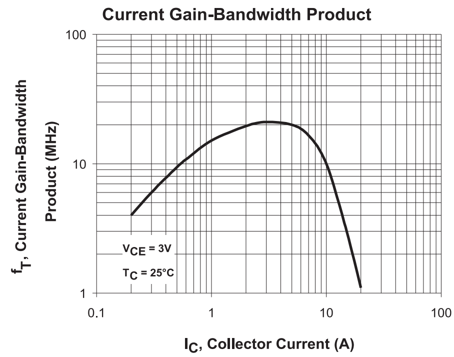












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