

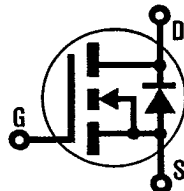
HEXFET® TRANSISTORS

IRF630

IRF631

IRF632

IRF633



N-Channel

200 Volt, 0.4 Ohm HEXFET
TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

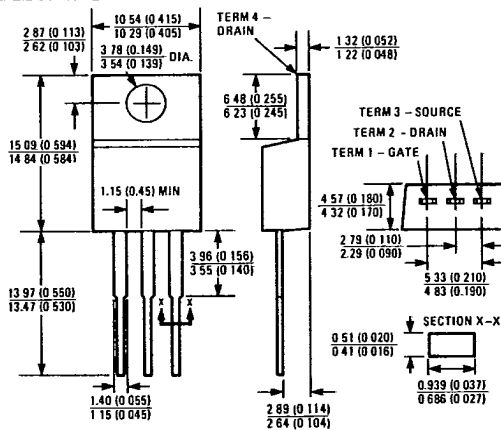
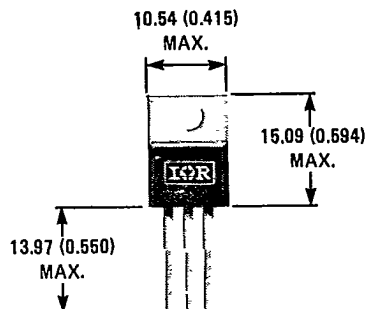
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- Excellent Temperature Stability

Product Summary

Part Number	V _{DS}	R _{DS(on)}	I _D
IRF630	200V	0.4Ω	9.0A
IRF631	150V	0.4Ω	9.0A
IRF632	200V	0.6Ω	8.0A
IRF633	150V	0.6Ω	8.0A

CASE STYLE AND DIMENSIONS


Case Style TO-220AB
Dimensions in Millimeters and (Inches)

C-241

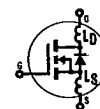
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Absolute Maximum Ratings

Parameter	IRF630	IRF631	IRF632	IRF633	Units
V_{DS} Drain - Source Voltage ①	200	150	200	150	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20\text{ k}\Omega$) ①	200	150	200	150	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	9.0	9.0	8.0	8.0	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM} Pulsed Drain Current ③	36	36	32	32	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	75 (See Fig. 14)				W
Linear Derating Factor	0.6 (See Fig. 14)				W/K ④
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
T_J Operating Junction and Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain - Source Breakdown Voltage	IRF630	200	—	—	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$
	IRF632	—	—	—	—	
	IRF631 IRF633	150	—	—	V	
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	$V_{GS} = 20\text{V}$
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	500	nA	$V_{GS} = -20\text{V}$
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0\text{V}$
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$
$I_{D(on)}$ On-State Drain Current ②	IRF630	9.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}, V_{GS} = 10\text{V}$
	IRF631	—	—	—	—	
	IRF632 IRF633	8.0	—	—	A	
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	IRF630	—	0.25	0.4	Ω	$V_{GS} = 10\text{V}, I_D = 5.0\text{A}$
	IRF631	—	—	—	—	
	IRF632 IRF633	—	0.4	0.6	Ω	
g_{fs} Forward Transconductance ②	ALL	3.0	4.8	—	S (V)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}, I_D = 5.0\text{A}$
C_{iss} Input Capacitance	ALL	—	600	800	pF	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1.0\text{ MHz}$ See Fig. 10
C_{oss} Output Capacitance	ALL	—	250	450	pF	
C_{rss} Reverse Transfer Capacitance	ALL	—	80	150	pF	
$t_{d(on)}$ Turn-On Delay Time	ALL	—	—	30	ns	$V_{DD} = 90\text{V}, I_D = 5.0\text{A}, Z_o = 15\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r Rise Time	ALL	—	—	50	ns	
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	—	50	ns	
t_f Fall Time	ALL	—	—	40	ns	$V_{GS} = 10\text{V}, I_D = 12\text{A}, V_{DS} = 0.8 \text{ Max. Rating.}$ See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	19	30	nC	
Q_{gs} Gate-Source Charge	ALL	—	10	—	nC	
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC	Measured from the contact screw on tab to center of die. Measured from the drain lead, 6mm (0.25 in.) from package to center of die. Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
L_D Internal Drain Inductance	ALL	—	3.5	—	nH	
		—	4.5	—	nH	
L_S Internal Source Inductance	ALL	—	7.5	—	nH	



Thermal Resistance

R_{thJC} Junction-to-Case	ALL	—	—	1.67	K/W ④	
R_{thCS} Case-to-Sink	ALL	—	1.0	—	K/W ④	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	80	K/W ④	Typical socket mount

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF630 IRF631	—	—	9.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF632 IRF633	—	—	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF630 IRF631	—	—	36	A	
		IRF632 IRF633	—	—	32	A	
V_{SD}	Diode Forward Voltage ②	IRF630 IRF631	—	—	2.0	V	$T_C = 25^\circ\text{C}, I_S = 9.0\text{A}, V_{GS} = 0\text{V}$
		IRF632 IRF633	—	—	1.8	V	$T_C = 25^\circ\text{C}, I_S = 8.0\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	$T_J = 150^\circ\text{C}, I_F = 9.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	3.0	—	μC	$T_J = 150^\circ\text{C}, I_F = 9.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

④ $\text{K/W} = ^\circ\text{C/W}$
 $\text{W/K} = \text{W}/^\circ\text{C}$

③ Repetitive Rating: Pulse width limited
by max. junction temperature.

See Transient Thermal Impedance Curve (Fig. 5).

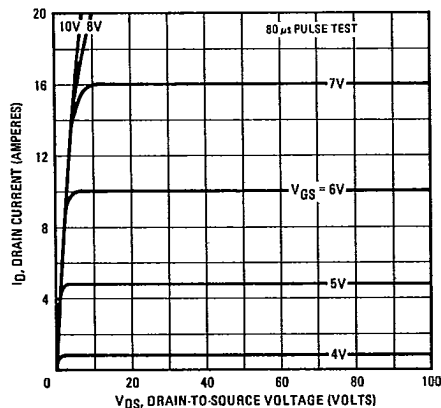


Fig. 1 — Typical Output Characteristics

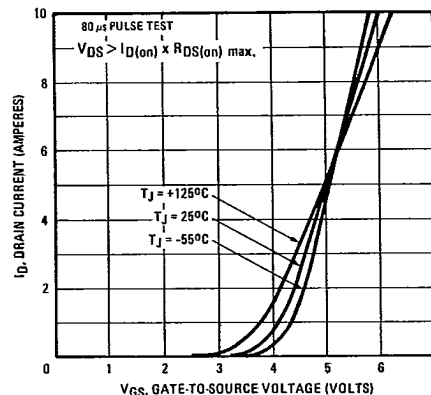


Fig. 2 — Typical Transfer Characteristics

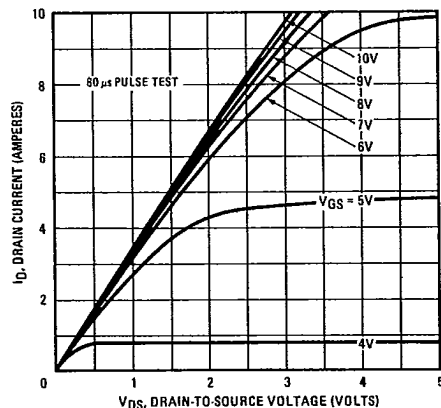


Fig. 3 — Typical Saturation Characteristics

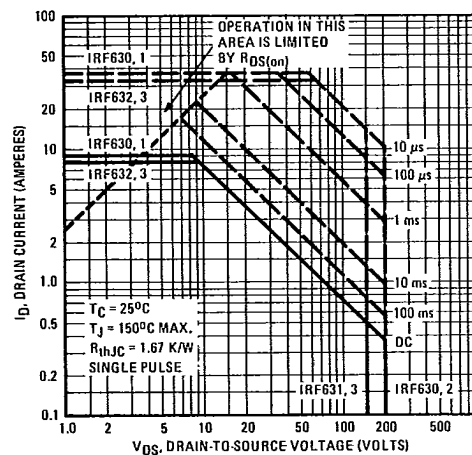


Fig. 4 — Maximum Safe Operating Area

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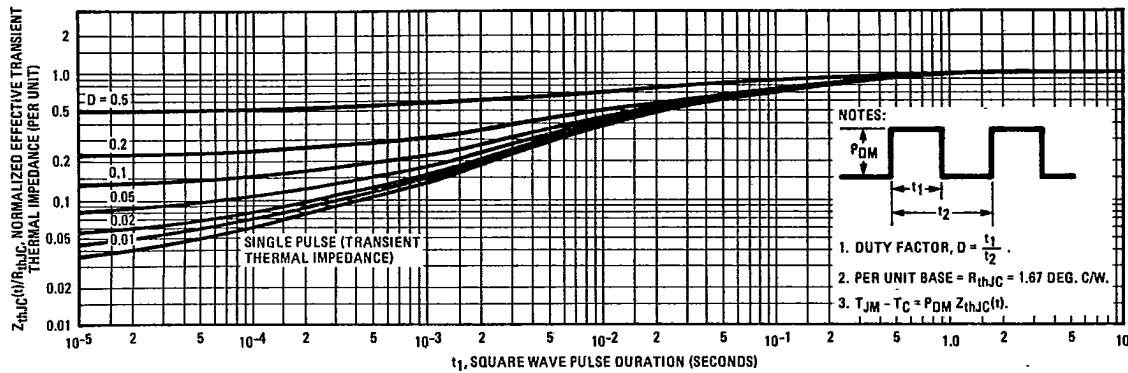


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

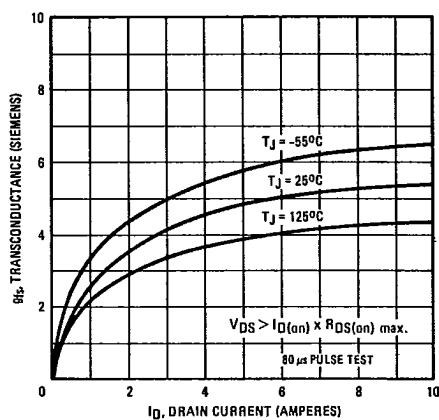


Fig. 6 — Typical Transconductance Vs. Drain Current

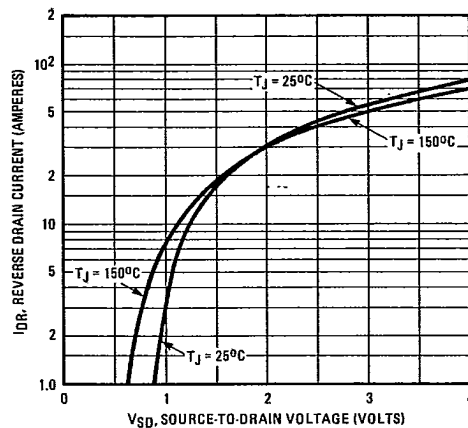


Fig. 7 — Typical Source-Drain Diode Forward Voltage

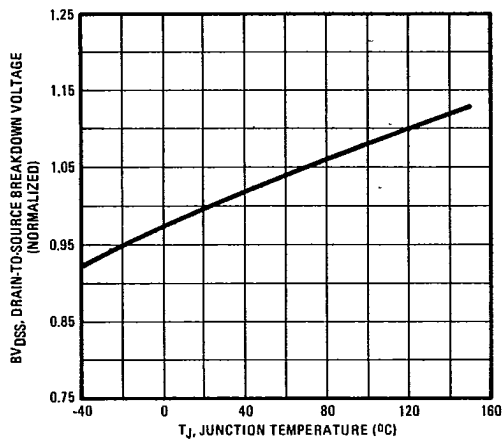


Fig. 8 — Breakdown Voltage Vs. Temperature

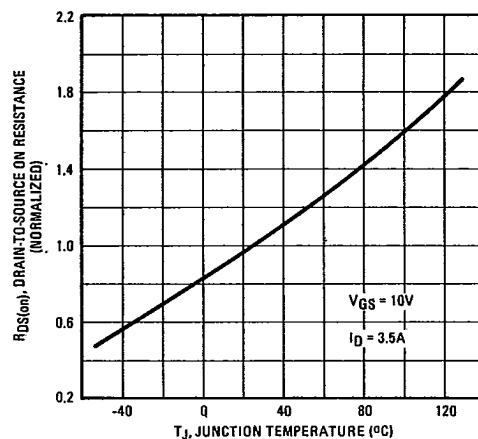


Fig. 9 — Normalized On-Resistance Vs. Temperature

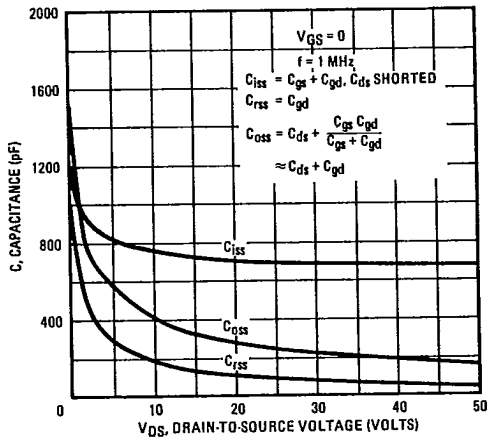


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

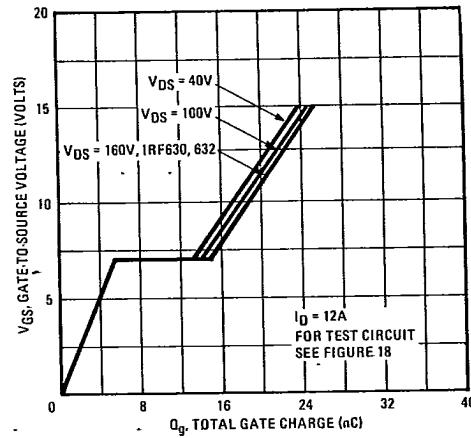


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

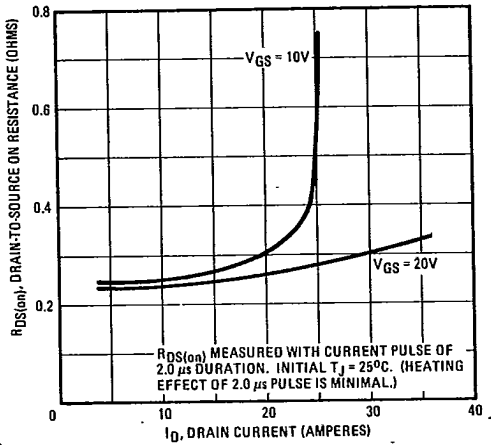


Fig. 12 - Typical On-Resistance Vs. Drain Current

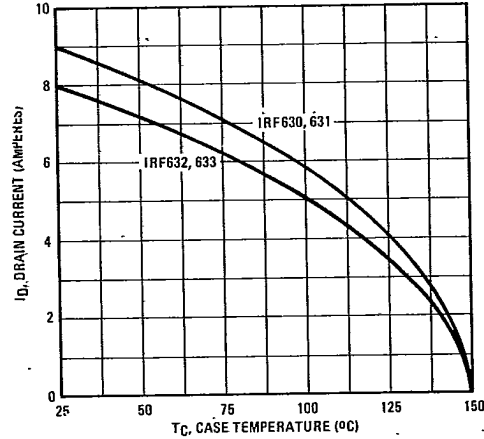


Fig. 13 - Maximum Drain Current Vs. Case Temperature

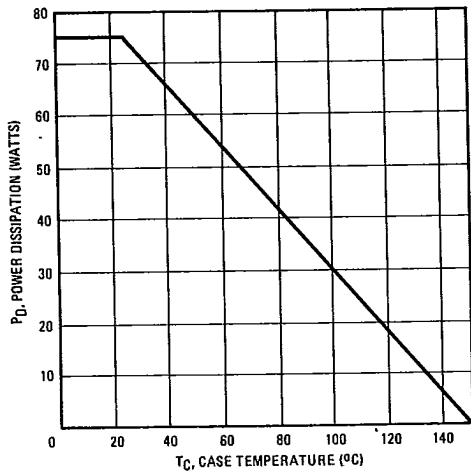


Fig. 14 - Power Vs. Temperature Derating Curve

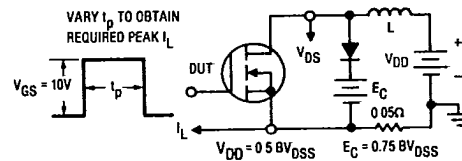


Fig. 15 - Clamped Inductive Test Circuit

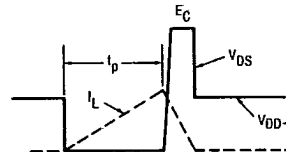


Fig. 16 - Clamped Inductive Waveforms

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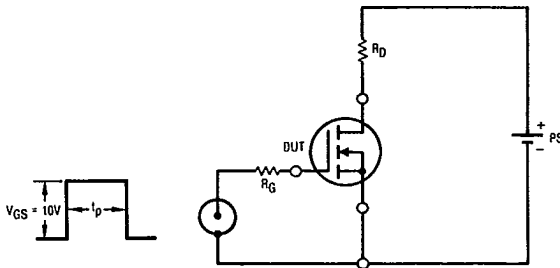


Fig. 17 - Switching Time Test Circuit

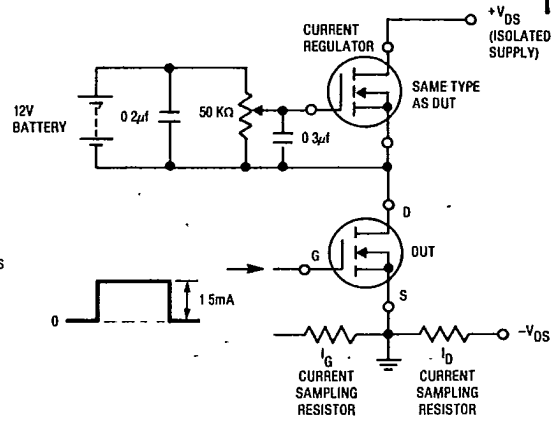
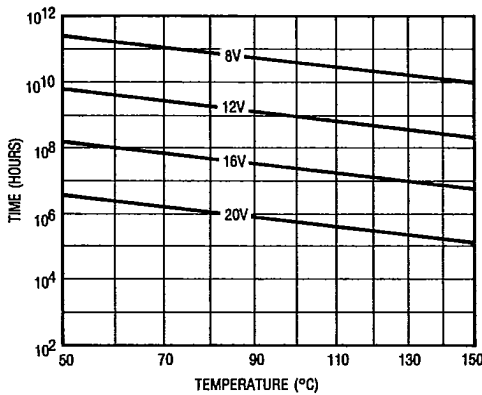
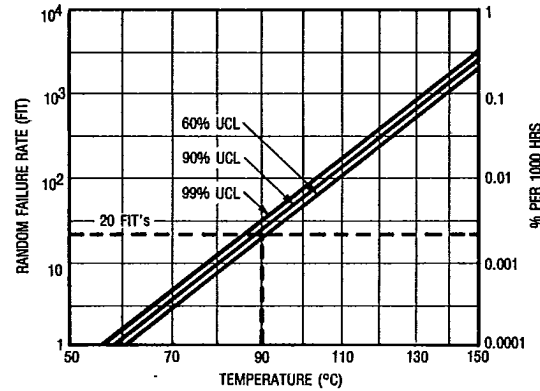


Fig. 18 - Gate Charge Test Circuit



*Fig. 19 - Typical Time to Accumulated 1% Gate Failure



*Fig. 20 - Typical High Temperature Reverse Bias (HTRB) Failure Rate

*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.