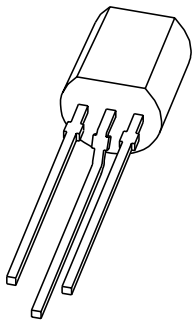
DATA SHEET



BSN304
N-channel enhancement mode vertical D-MOS transistor

Product specification
Supersedes data of 1997 Jun 17

2001 Dec 11

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N-channel enhancement mode vertical D-MOS transistor

BSN304

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interruptor in telephone sets
- Relay, high-speed and line transformer drivers.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant package.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	gate
2	drain
3	source

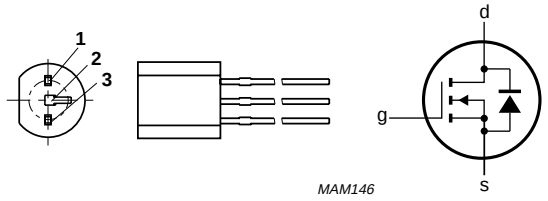


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	300	V
I_D	drain current (DC)		–	300	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	1	W
V_{GSO}	gate-source voltage	open drain	–	±20	V
R_{DSon}	drain-source on-state resistance	I_D = 250 mA; V_{GS} = 10 V	–	6	Ω
V_{GSoff}	gate-source cut-off voltage	I_D = 1 mA; $V_{GS} = V_{DS}$	0.8	2	V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	300	mA
I_{DM}	peak drain current		–	1.2	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm x 10 mm.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient; note 1	125	K/W

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm x 10 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	300	–	–	V
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	0.8	–	2	V
R_{DSon}	drain-source on-state resistance	I_D = 250 mA; V_{GS} = 10 V	–	3.7	6	Ω
		I_D = 20 mA; V_{GS} = 2.4 V	–	4.8	10	Ω
I_{DSS}	drain-source leakage current	V_{DS} = 240 V; V_{GS} = 0	–	–	100	nA
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	690	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	100	120	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	21	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	10	15	pF
Switching times (see Figs 2 **and** 3**)**						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	6	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 10 to 0 V	–	46	60	ns

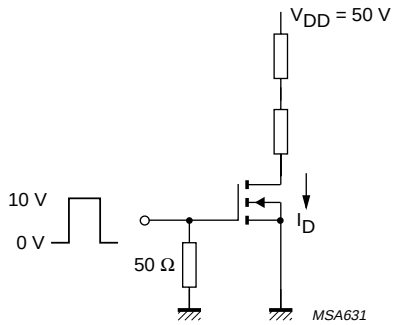


Fig.2 Switching times test circuit.

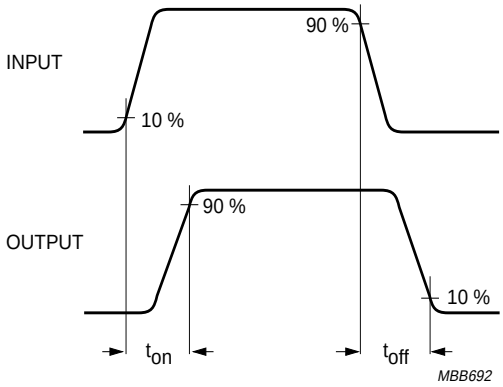


Fig.3 Input and output waveforms.

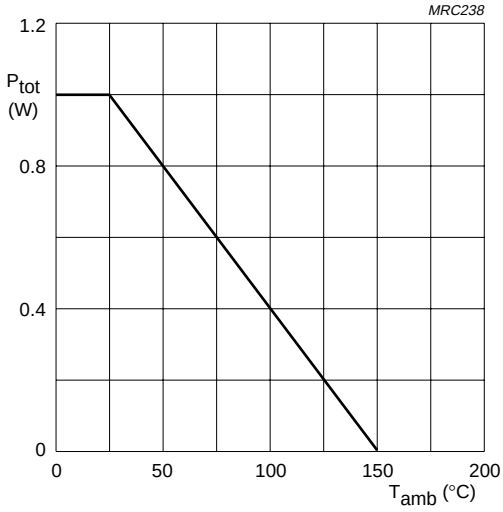
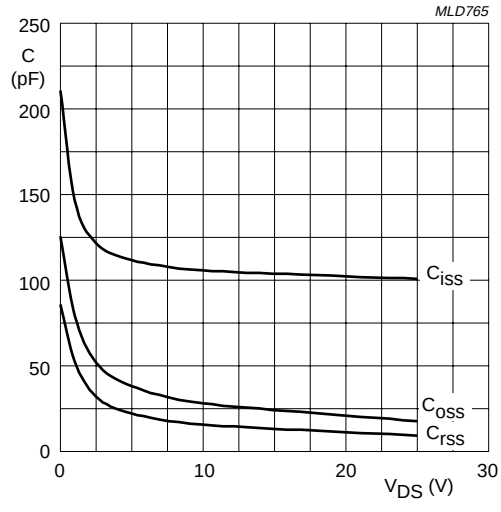
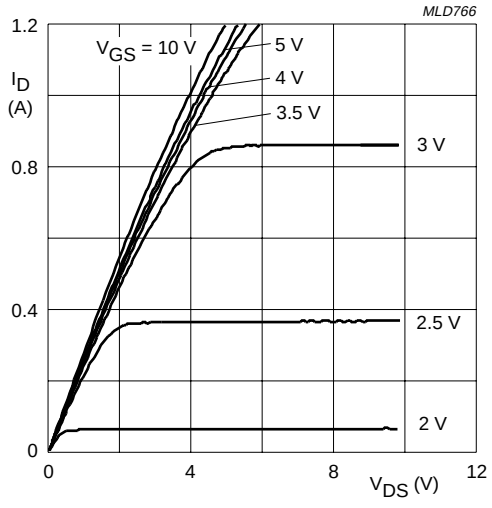


Fig.4 Power derating curve.



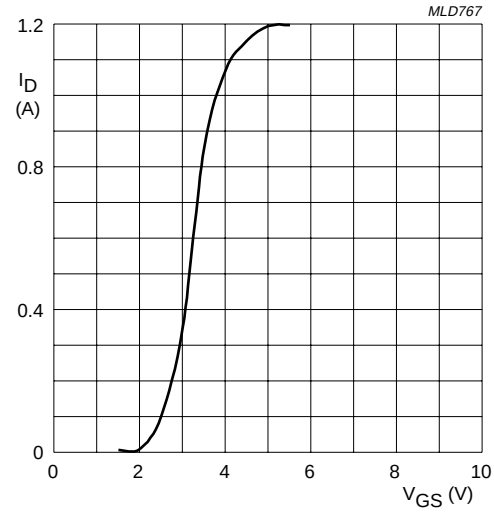
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage; typical values.



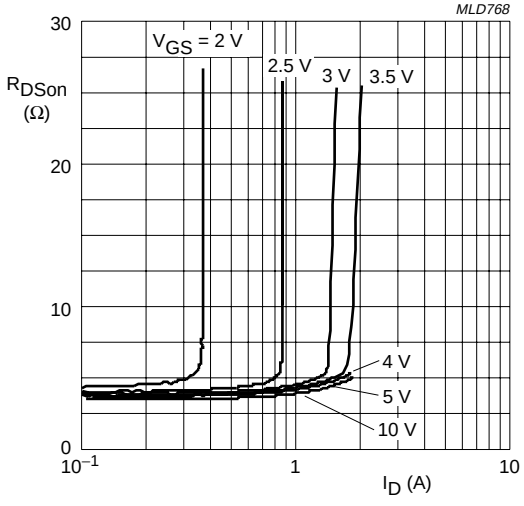
T_j = 25 °C.

Fig.6 Typical output characteristics.



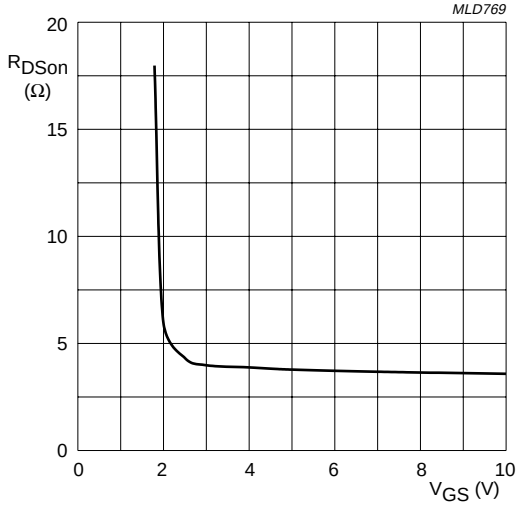
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Typical transfer characteristics.



T_j = 25 °C.

Fig.8 Drain-source on-state resistance as a function of drain current; typical values.



V_{DS} = 100 mV; T_j = 25 °C.

Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.

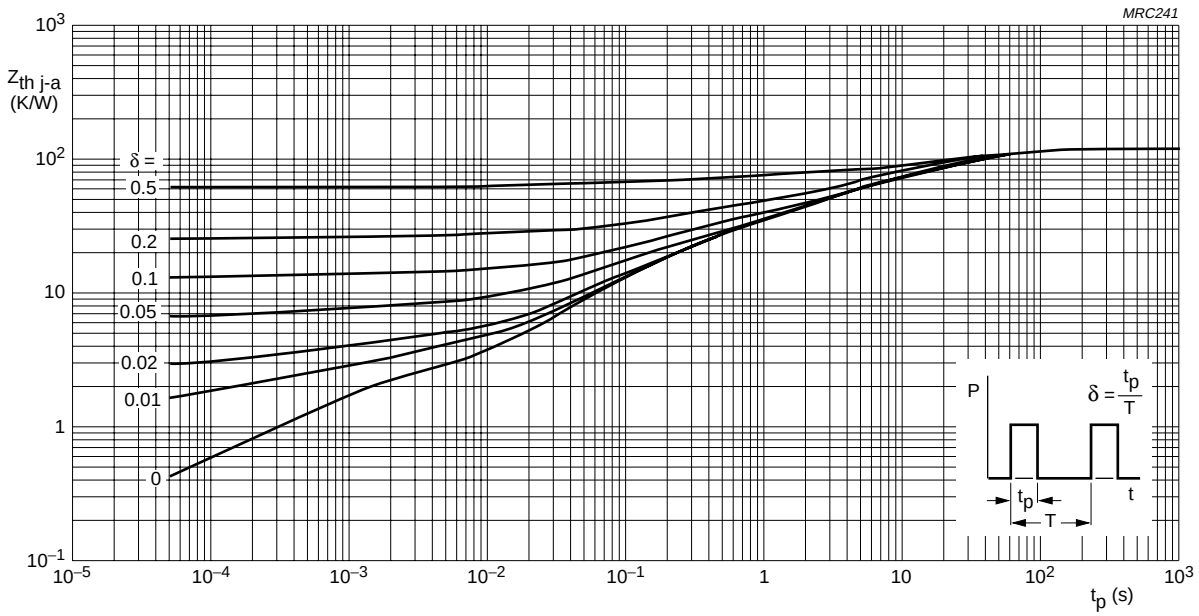
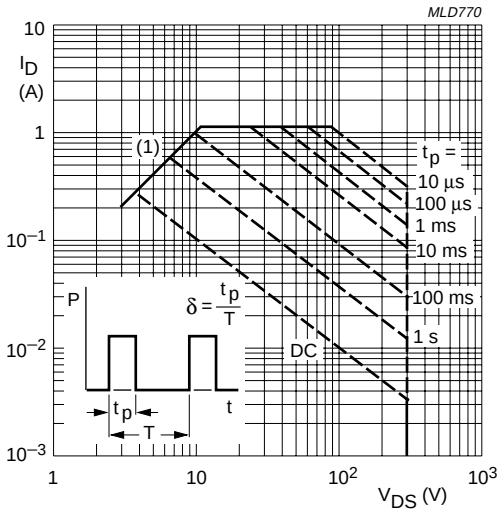
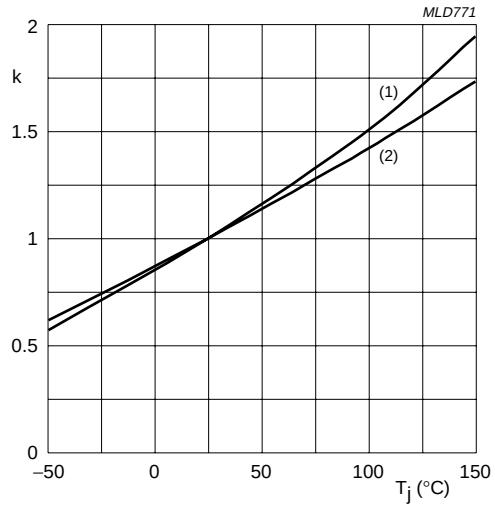


Fig.10 Transient thermal resistance from junction to ambient as a function of pulse time.



δ = 0.01; T_{amb} = 25 °C.
(1) R_{DSon} limitation.

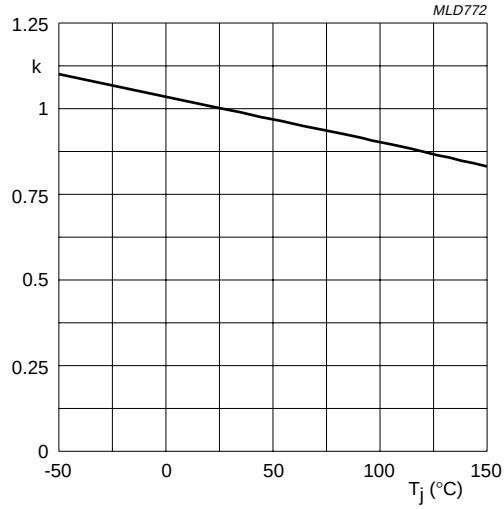
Fig.11 SOAR curve.



$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}.$$

Typical R_{DSon};
(1) I_D = 250 mA; V_{GS} = 10 V.
(2) I_D = 20 mA; V_{GS} = 2.4 V.

Fig.12 Temperature coefficient of drain-source on-state resistance; typical values.

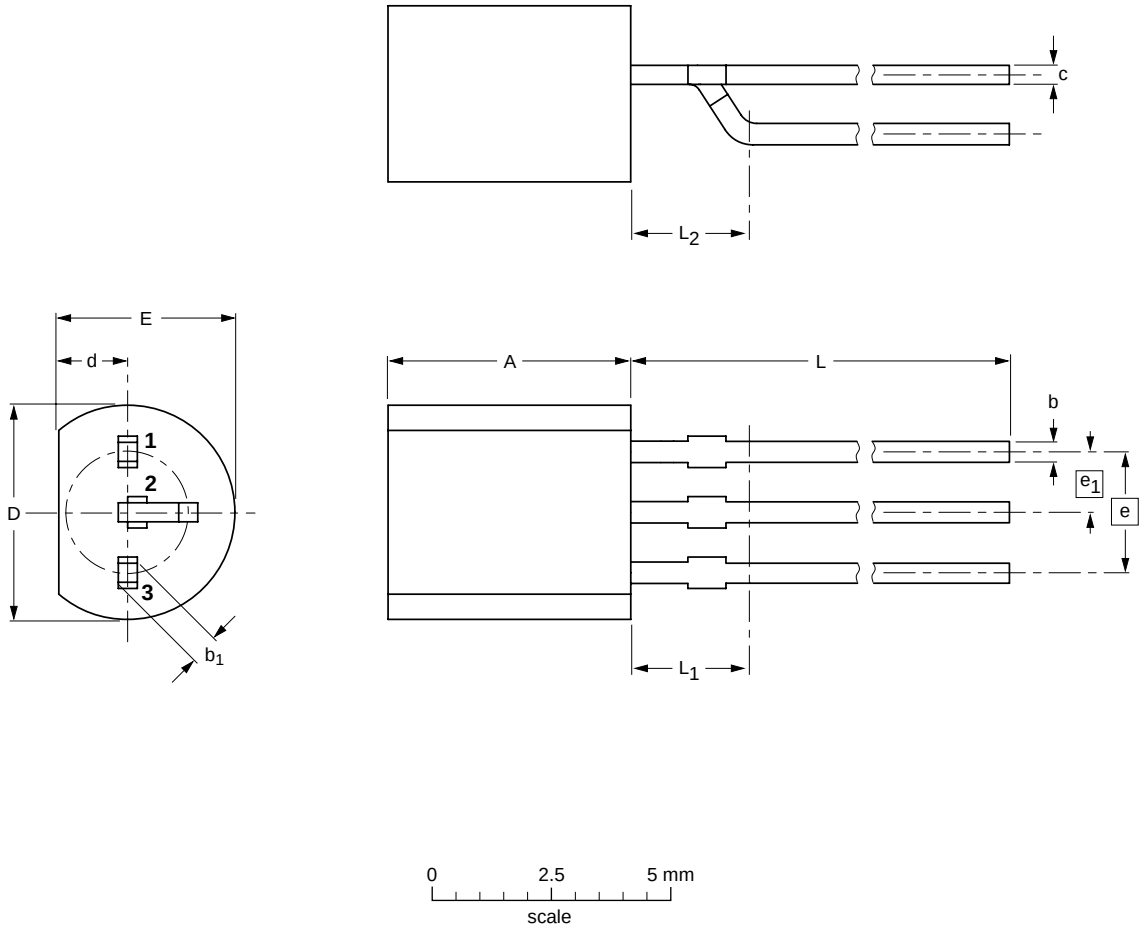


$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}.$$

Fig.13 Temperature coefficient of gate-source threshold voltage; typical values.

PACKAGE OUTLINES

Plastic single-ended leaded (through hole) package; 3 leads (on-circle) **SOT54 variant**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max	L_2 max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54 variant		TO-92 variant	SC-43			98-03-26

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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