

TOSHIBA PHOTOCOUPLER GaAlAs IRED + PHOTO-IC

TLP759

DIGITAL LOGIC GROUND ISOLATION

LINE RECEIVER

MICROPROCESSOR SYSTEM INTERFACES

SWITCHING POWER SUPPLY FEEDBACK CONTROL

TRANSISTOR INVERTOR

Unit in mm

The TOSHIBA TLP759 consists of a GaAlAs high-output light emitting diode and a high speed detector of one chip photo diode-transistor. This unit is 8-lead DIP.

TLP759 has no internal base connection, and a Faraday shield integrated on the photodetector chip provides an effective common mode noise transient immunity.

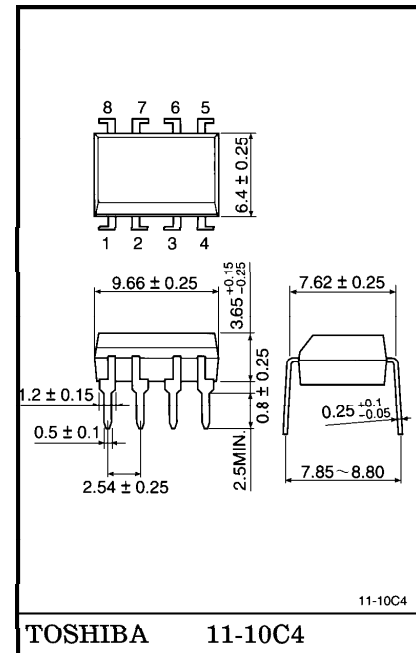
So this is suitable for application in noisy environmental condition.

- Isolation Voltage : 5000 Vrms (Min.)
- Switching Speed : $t_{pHL}=0.2\mu s$ (Typ.)
 $t_{pLH}=0.3\mu s$ (Typ.) ($R_L=1.9k\Omega$)
- TTL Compatible
- UL Recognized : UL1577, File No. E67349
- Option (D4) type
VDE Approved : DIN VDE0884 / 06.92
Certificate No. 83676

Maximum Operating Insulation Voltage : 890V_{PK}Highest Permissible Over Voltage : 6000V_{PK}

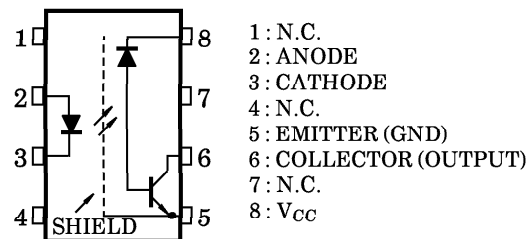
(Note) When a VDE0884 approved type is needed,
please designate the "Option (D4)"

- Creepage Distance : 7.0mm (Min.)
- Clearance : 7.0mm (Min.)
- Insulation Thickness : 0.4mm (Min.)

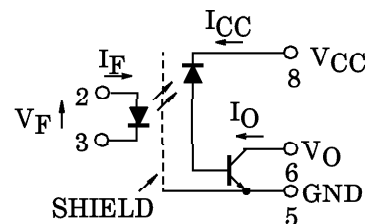


Weight : 0.54g

PIN CONFIGURATION (TOP VIEW)



SCHEMATIC



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MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
L D E	Forward Current (Note 1)	I _F	25	mA
	Pulse Forward Current (Note 2)	I _{FP}	50	mA
	Peak Transient Forward Current (Note 3)	I _{FPT}	1	A
	Reverse Voltage	V _R	5	V
	Diode Power Dissipation (Note 4)	P _D	45	mW
D E T E C T O R	Output Current	I _O	8	mA
	Peak Output Current	I _{OP}	16	mA
	Output Voltage	V _O	−0.5~20	V
	Supply Voltage	V _{CC}	−0.5~30	V
	Output Power Dissipation (Note 5)	P _O	100	mW
Operating Temperature Range		T _{opr}	−55~100	°C
Storage Temperature Range		T _{opr}	−55~125	°C
Lead Solder Temperature (10s) (Note 6)		T _{sol}	260	°C
Isolation Voltage (AC, 1min., R.H. ≤ 60%) (Note 7)		BV _S	5000	V _{rms}

(Note 1) Derate 0.8mA/°C above 70°C.

(Note 2) 50% duty cycle, 1ms pulse width.

Derate 1.6mA/°C above 70°C.

(Note 3) Pulse width ≤ 1μs, 300pps.

(Note 4) Derate 0.9mW/°C above 70°C.

(Note 5) Derate 2mW/°C above 70°C.

(Note 6) Soldering portion of lead: up to 2mm from the body of the device.

(Note 7) Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7, and 8 shorted together.

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
LDE	Forward Voltage	V_F	$I_F = 16\text{mA}$	—	1.65	1.85	V
	Forward Voltage Temperature Coefficient	$\Delta V_F / \Delta T_a$	$I_F = 16\text{mA}$	—	-2	—	mV / °C
	Reverse Current	I_R	$V_R = 5\text{V}$	—	—	10	μA
	Capacitance Between Terminals	C_T	$V_F = 0, f = 1\text{MHz}$	—	45	—	pF
DETECTOR	High Level Output Current	$I_{OH(1)}$	$I_F = 0\text{mA}, V_{CC} = V_O = 5.5\text{V}$	—	3	500	nA
		$I_{OH(2)}$	$I_F = 0\text{mA}, V_{CC} = 30\text{V}, V_O = 20\text{V}$	—	—	5	μA
		I_{OH}	$I_F = 0\text{mA}, V_{CC} = 30\text{V}, V_O = 20\text{V}$ $T_a = 70^\circ\text{C}$	—	—	50	
	High Level Supply Voltage	I_{CCH}	$I_F = 0\text{mA}, V_{CC} = 30\text{V}$	—	0.01	1	μA
COUPLED	Current Transfer Ratio	I_O / I_F	$I_F = 16\text{mA}, V_{CC} = 4.5\text{V}$ $V_O = 0.4\text{V}$	20	40	—	%
	Low Level Output Voltage	V_{OL}	$I_F = 16\text{mA}, V_{CC} = 4.5\text{V}$ $I_O = 2.4\text{mA}$	—	—	0.4	V
	Resistance (Input-Output)	R_S	R.H. $\leq 60\%$, $V_S = 500\text{V}$ (Note 7)	1×10^{12}	10^{14}	—	Ω
	Capacitance (Input-Output)	C_S	$V_S = 0, f = 1\text{MHz}$ (Note 7)	—	0.8	—	pF

SWITCHING CHARACTERISTICS (Ta = 25°C, VCC = 5V)

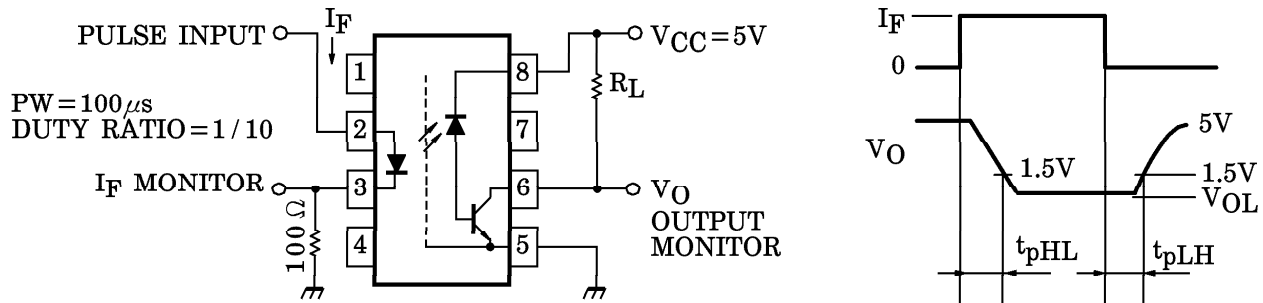
CHARACTERISTIC	SYMBOL	TEST CIR - CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (H→L)	t_{pHL}	1	$I_F = 0 \rightarrow 16\text{mA}, V_{CC} = 5\text{V}$ $R_L = 1.9\text{k}\Omega$	—	0.2	0.8	μs
Propagation Delay Time (L→H)	t_{pLH}		$I_F = 16 \rightarrow 0\text{mA}, V_{CC} = 5\text{V}$ $R_L = 1.9\text{k}\Omega$	—	0.3	0.8	μs
Common Mode Transient Immunity at Logic High Output (Note 8)	CM_H	2	$I_F = 0\text{mA}, V_{CM} = 400\text{Vp-p}$ $R_L = 4.1\text{k}\Omega$	5000	10000	—	V / μs
Common Mode Transient Immunity at Logic Low Output (Note 8)	CM_L		$I_F = 16\text{mA}$ $V_{CM} = 400\text{Vp-p}$ $R_L = 4.1\text{k}\Omega$	-5000	-10000	—	V / μs

(Note 8) CM_L is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8V$).

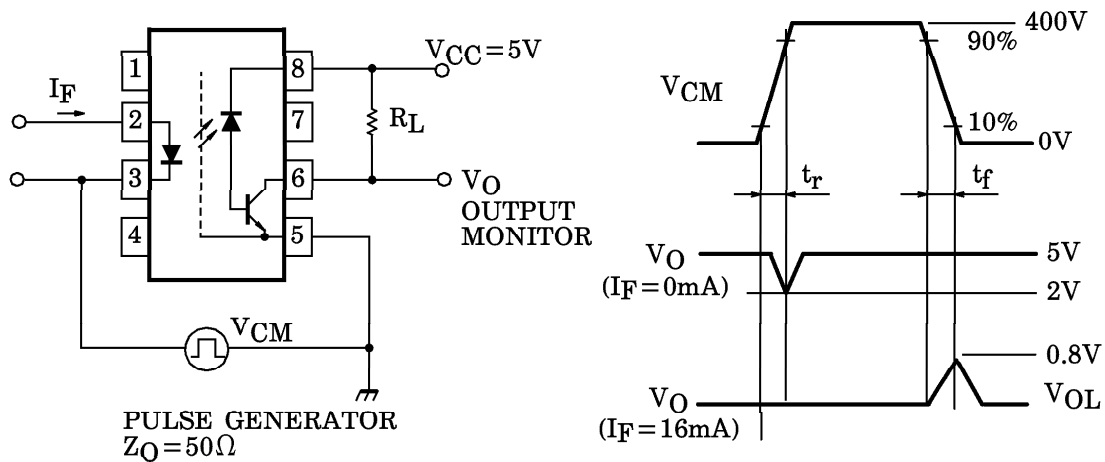
CM_H is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 2.0V$).

(Note 9) Maximum electrostatic discharge voltage for any pins: 100V (C=200pF, R=0)

TEST CIRCUIT 1: Switching Time Test Circuit



TEST CIRCUIT 2: Common Mode Noise Immunity Test Circuit



$$CM_H = \frac{320(V)}{t_r(\mu s)}, \quad CM_L = \frac{320(V)}{t_f(\mu s)}$$

