

FEATURES

- Two Matched ADCs on Single Chip
- 50 MSPS Conversion Speed
- On-Board Voltage Reference
- Low Power (<1W)
- Low Input Capacitance (10 pF)
- 65 V Power Supplies
- Flexible Input Range

APPLICATIONS

- Quadrature Demodulation for Communications
- Digital Oscilloscopes
- Electronic Warfare
- Radar

GENERAL DESCRIPTION

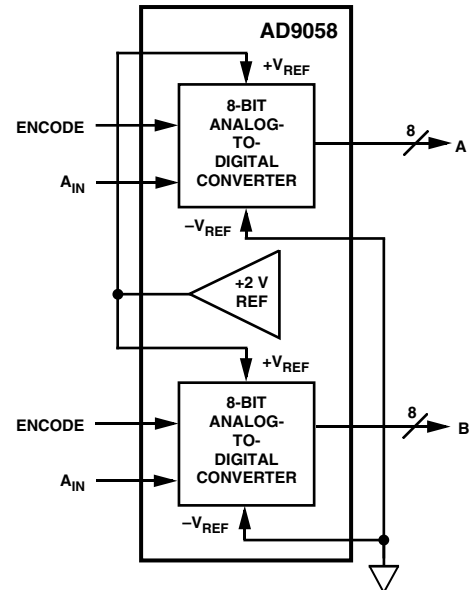
The AD9058 combines two independent high performance 8-bit analog-to-digital converters (ADCs) on a single monolithic IC. Combined with an optional onboard voltage reference, the AD9058 provides a cost effective alternative for systems requiring two or more ADCs.

Dynamic performance (SNR, ENOB) is optimized to provide up to 50 MSPS conversion rates. The unique architecture results in low input capacitance while maintaining high performance and low power (<0.5 watt/channel). Digital inputs and outputs are TTL compatible.

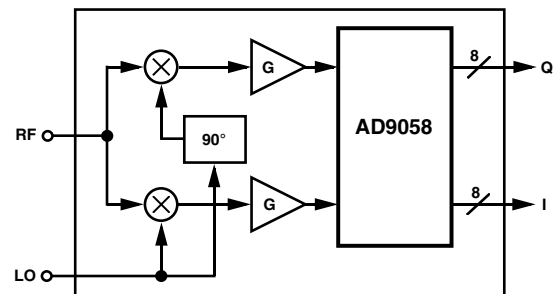
Performance has been optimized for an analog input of 2 V p-p (± 1 V; 0 V to +2 V). Using the onboard +2 V voltage reference, the AD9058 can be set up for unipolar positive operation (0 V to +2 V). This internal voltage reference can drive both ADCs.

Commercial (0°C to +70°C) and military (-55°C to +125°C) temperature range parts are available. Parts are supplied in hermetic 48-lead DIP and 44-lead "J" lead packages.

FUNCTIONAL BLOCK DIAGRAM



QUADRATURE RECEIVER



REV. B

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AD9058—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS¹

Analog Input	-1.5 V to +2.5 V
+V _S	+6 V
-V _S	+0.8 V to -6 V ²
Digital Inputs	-0.5 V to +V _S
Digital Output Current	20 mA
Voltage Reference Current	.53 mA
+V _{REF}	+2.5 V

-V _{REF}	-1.5
Operating Temperature Range	
AD9058JD/JJ/KD/KJ	0°C to +70°C
Maximum Junction Temperature ³	
AD9058JD/JJ/KD/KJ	+175°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

ELECTRICAL CHARACTERISTICS

[±V_S = ±5 V; V_{REF} = +2 V (internal); ENCODE = 40 MSPS; A_{IN} = 0 V to +2 V; -V_{REF} = GROUND, unless otherwise noted.]² All specifications apply to either of the two ADCs

Parameter (Conditions)	Temp	Test Level	AD9058JD/JJ			AD9058KD/KJ			Unit
			Min	Typ	Max	Min	Typ	Max	
RESOLUTION			8			8			Bits
DC ACCURACY									
Differential Nonlinearity	+25°C	I		0.25	0.65		0.25	0.5	LSB
	Full	VI			0.8			0.7	LSB
Integral Nonlinearity	+25°C	I		0.5	1.3		0.5	1.0	LSB
	Full	VI			1.4			1.25	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			
ANALOG INPUT									
Input Bias Current	+25°C	I		75	170		75	170	μA
	Full	VI			340			340	μA
Input Resistance	+25°C	I	12	28		12	28		kΩ
Input Capacitance	+25°C	IV		10	15		10	15	pF
Analog Bandwidth	+25°C	V		175			175		MHz
REFERENCE INPUT									
Reference Ladder Resistance	+25°C	I	120	170	220	120	170	220	Ω
	Full	VI	80		270	80		270	Ω
Ladder Tempco	Full	V		0.45			0.45		Ω/°C
Reference Ladder Offset (Top)	+25°C	I		8	16		8	16	mV
	Full	VI			24			24	mV
Reference Ladder Offset (Bottom)	+25°C	I		8	23		8	23	mV
	Full	VI			33			33	mV
Offset Drift Coefficient	Full	V		50			50		μV/°C
INTERNAL VOLTAGE REFERENCE									
Reference Voltage	+25°C	I	1.95	2.0	2.20	1.95	2.0	2.20	V
	Full	VI	1.90		2.25	1.90		2.25	V
Temperature Coefficient	Full	V		150			150		μV/°C
Power Supply Rejection Ratio (PSRR)	+25°C	I		10	25		10	25	mV/V
SWITCHING PERFORMANCE									
Maximum Conversion Rate ⁴	+25°C	I		50		50	60		MSPS
Aperture Delay (t _A)	+25°C	IV	0.1	0.8	1.5	0.1	0.8	1.5	ns
Aperture Delay Matching	+25°C	IV		0.2	0.5		0.2	0.5	ns
Aperture Uncertainty (Jitter)	+25°C	V		10			10		ps, rms
Output Delay (Valid) (t _V) ⁴	+25°C	I		8		5	8		ns
Output Delay (t _V) Tempco	Full	V		16			16		ps/°C
Propagation Delay (t _{PD}) ⁴	+25°C	I		12			12	19	ns
Propagation Delay (t _{PD}) Tempco	Full	V		-16			-16		ps/°C
Output Time Skew	+25°C	V		1			1		ns
ENCODE INPUT									
Logic "1" Voltage	Full	VI	2			2			V
Logic "0" Voltage	Full	VI			0.8			0.8	V
Logic "1" Current	Full	VI			600			600	μA
Logic "0" Current	Full	VI			1000			1000	μA
Input Capacitance	+25°C	V		5			5		pF
Pulsewidth (High)	+25°C	I		8		8			ns
Pulsewidth (Low)	+25°C	I		8		8			ns

Parameter (Conditions)	Temp	Test Level	AD9058JD/JJ			AD9058KD/KJ			Unit
			Min	Typ	Max	Min	Typ	Max	
DYNAMIC PERFORMANCE									
Transient Response	+25°C	V		2			2		ns
Overshoot Recovery Time	+25°C	V		2			2		ns
Effective Number of Bits (ENOB) ⁵									
Analog Input @ 2.3 MHz	+25°C	I		7.7		7.2	7.7		Bits
@ 10.3 MHz	+25°C	I		7.4		7.1	7.4		Bits
Signal-to-Noise Ratio ⁵									
Analog Input @ 2.3 MHz	+25°C	I		48		45	48		dB
@ 10.3 MHz	+25°C	I		46		44	46		dB
Signal-to-Noise Ratio ⁵ (Without Harmonics)									
Analog Input @ 2.3 MHz	+25°C	I		48		46	48		dB
@ 10.3 MHz	+25°C	I		47		45	47		dB
2nd Harmonic Distortion									
Analog Input @ 2.3 MHz	+25°C	I		58		48	58		dBc
@ 10.3 MHz	+25°C	I		58		48	58		dBc
3rd Harmonic Distortion									
Analog Input @ 2.3 MHz	+25°C	I		58		50	58		dBc
@ 10.3 MHz	+25°C	I		58		50	58		dBc
Crosstalk Rejection ⁶	+25°C	IV		60		48	60		dBc
DIGITAL OUTPUTS									
Logic "1" Voltage (I _{OH} = 2 mA)	Full	VI	2.4			2.4			V
Logic "0" Voltage (I _{OL} = 2 mA)	Full	VI			0.4		0.4		V
POWER SUPPLY⁷									
+V _S Supply Current	Full	VI		127	154		127	154	mA
-V _S Supply Current	Full	VI		27	38		27	38	mA
Power Dissipation	Full	VI		770	960		770	960	mW

NOTES

¹Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

²For applications in which +V_S may be applied before -V_S, or +V_S current is not limited to 500 mA, a reverse biased clamping diode should be inserted between ground and -V_S to prevent destructive latch up. See section entitled "Using the AD9058."

³Typical thermal impedances: 44-lead hermetic J-Leaded ceramic package: $\theta_{JA} = 86.4^{\circ}\text{C}/\text{W}$; $\theta_{JC} = 24.9^{\circ}\text{C}/\text{W}$; 48-lead hermetic DIP $\theta_{JA} = 40^{\circ}\text{C}/\text{W}$; $\theta_{JC} = 12^{\circ}\text{C}/\text{W}$.

⁴To achieve guaranteed conversion rate, connect each data output to ground through a 2 k Ω pull-down resistor.

⁵SNR performance limits for the 48-lead DIP "D" package are 1 dB less than shown. ENOB limits are degraded by 0.3 dB. SNR and ENOB measured with analog input signal 1 dB below full scale at specified frequency.

⁶Crosstalk rejection measured with full-scale signals of different frequencies (2.3 MHz and 3.5 MHz) applied to each channel. With both signals synchronously encoded at 40 MSPS, isolation of the undesired frequency is measured with an FFT.

⁷Applies to both A/Ss and includes internal ladder dissipation.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

- I – 100% production tested.
- II – 100% production tested at +25°C, and sample tested at specified temperatures.
- III – Sample tested only.
- IV – Parameter is guaranteed by design and characterization testing.
- V – Parameter is a typical value only.
- VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Model	Temperature Range	Description	Package Option ¹
AD9058JJ	0°C to +70°C	44-Lead J-Leaded Ceramic ²	J-44
AD9058KJ	0°C to +70°C	44-Lead J-Leaded Ceramic, AC Tested	J-44
AD9058TJ/883 ³	-55°C to +125°C	44-Lead J-Leaded Ceramic, AC Tested	J-44
AD9058JD	0°C to +70°C	48-Lead Ceramic DIP	D-48
AD9058KD	0°C to +70°C	48-Lead Ceramic DIP, AC Tested	D-48
AD9058TD/883 ³	-55°C to +125°C	48-Lead Ceramic DIP, AC Tested	D-48

NOTES

¹D = Hermetic Ceramic DIP Package; J = Leaded Ceramic Package.

²Hermetically sealed ceramic package; footprint equivalent to PLCC.

³For specifications, refer to Analog Devices Military Products Databook.

THEORY OF OPERATION

The AD9058 contains two separate 8-bit analog-to-digital converters (ADCs) on a single silicon die. The two devices can be operated independently with separate analog inputs, voltage references and clocks.

In a traditional flash converter, 256 input comparators are required to make the parallel conversion for 8-bit resolution. This is in marked contrast to the scheme used in the AD9058, as shown in Figure 1.

Unlike traditional “flash,” or parallel, converters, each of the two ADCs in the AD9058 utilizes a patented interpolating architecture to reduce circuit complexity, die size and input capacitance. These advantages accrue because, compared to a conventional flash design, only half the normal number of input comparator cells is required to accomplish the conversion.

In this unit, each of the two independent ADCs uses only 128 (2^7) comparators to make the conversion. The conversion for the seven most significant bits (MSBs) is performed by the 128 comparators. The value of the least significant bit (LSB) is determined by interpolation between adjacent comparators in the decoding register. A proprietary decoding scheme processes the comparator outputs and provides an 8-bit code to the output register of each ADC; the scheme also minimizes error codes.

Analog input range is established by the voltages applied at the voltage reference inputs ($+V_{REF}$ and $-V_{REF}$). The AD9058 can operate from 0 V to +2 V using the internal voltage reference, or anywhere between -1 V and +2 V using external references. Input range is limited to 2 V p-p when using external references. The internal resistor ladder divides the applied voltage reference into 128 steps, with each step representing two 8-bit quantization levels.

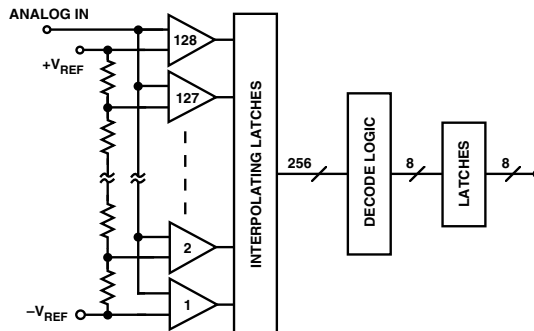


Figure 1. AD9058 Comparator Block Diagram

The onboard voltage reference, $+V_{INT}$, is a bandgap reference which has sufficient drive capability for both reference ladders. It provides a +2 V reference that can drive both ADCs in the AD9058 for unipolar positive operation (0 V to +2 V).

USING THE AD9058

Refer to Figure 2. Using the internal voltage reference connected to both ADCs as shown reduces the number of external components required to create a complete data acquisition system. The input ranges of the ADCs are positive unipolar in this configuration, ranging from 0 V to +2 V. Bipolar input signals are buffered, amplified and offset into the proper input range of the ADC using a good low distortion amplifier such as the AD9617 or AD9618.

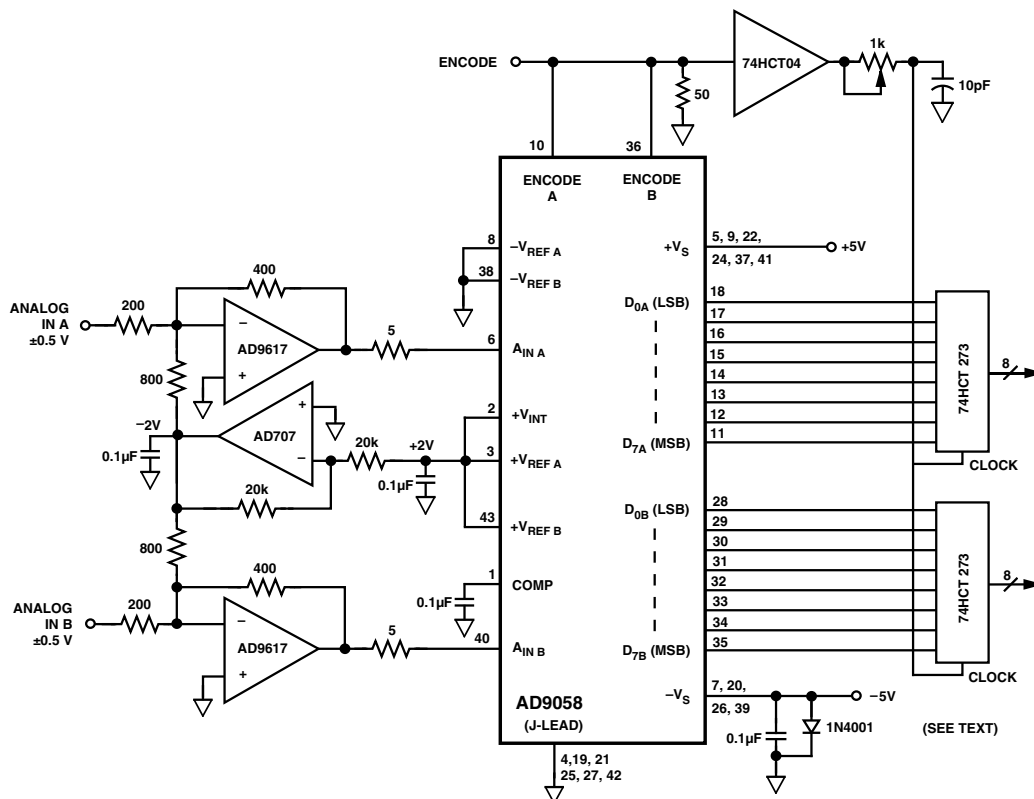


Figure 2. AD9058 Using Internal +2 V Voltage Reference

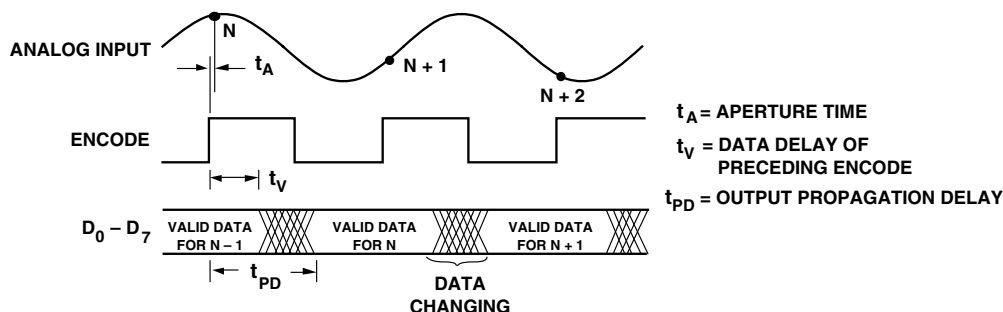


Figure 4. AD9058 Timing Diagram

Figure 5 below shows what the analog input to the AD9058 would look like when observed relative to the sample clock. Signal-to-noise ratio (SNR), transient response, and sample rate are all critical specifications in digitizing this “eye pattern.”

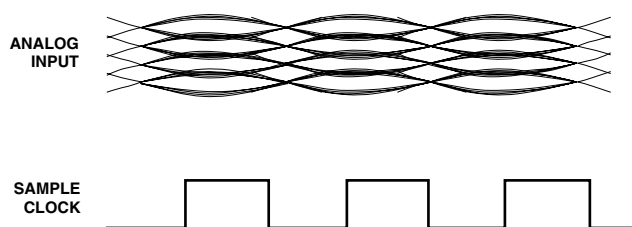


Figure 5. AD9058 I and Q Input Signals

Receiver sensitivity is limited by the SNR of the system. For the ADC, SNR is measured in the frequency domain and calculated with a Fast Fourier Transform (FFT). The *signal-to-noise ratio* equals the ratio of the fundamental component of the signal (rms amplitude) to the rms level of the noise. Noise is the sum of all other spectral components, including harmonic distortion, but excluding dc.

Although the signal being sampled does not have a significant slew rate at the instant it is encoded, dynamic performance of the ADC and the system is still critical. *Transient response* is the time required for the AD9058 to achieve full accuracy when a step function input is applied. *Overvoltage recovery time* is the interval required for the AD9058 to recover to full accuracy after an overdriven analog input signal is reduced to its input range.

Time domain performance of the ADC is also extremely important in digital oscilloscopes. When a track (sample)-and-hold is used ahead of the ADC, its operation becomes similar to that described above for receivers.

The dynamic response to high-frequency inputs can be described by the *effective number of bits (ENOB)*. The *effective number of bits* is calculated with a sine wave curve fit and is expressed as:

$$ENOB = N - \text{LOG}_2 [\text{Error (measured)} / \text{Error (ideal)}]$$

where N is the resolution (number of bits) and measured error

is actual rms error calculated from the converter’s outputs with a pure sine wave applied as the input.

Maximum conversion rate is defined as the encode (sample) rate at which SNR of the lowest frequency analog test signal drops no more than 3 dB below the guaranteed limit.

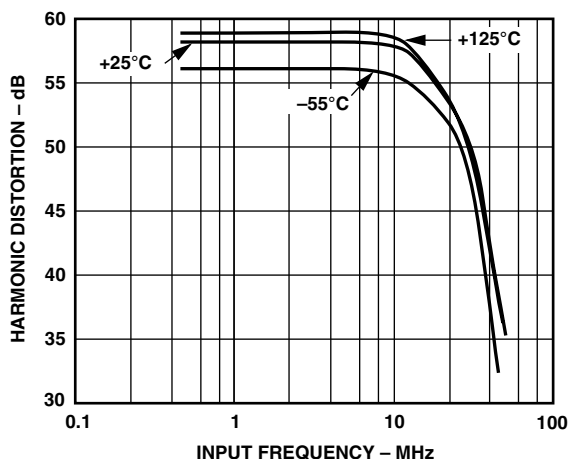


Figure 6. Harmonic Distortion vs. Analog Input Frequency

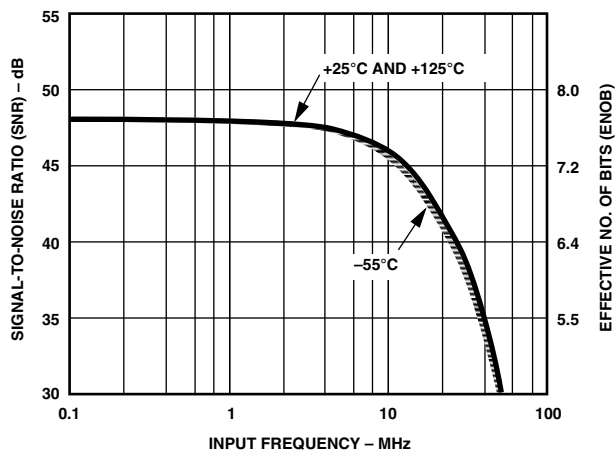
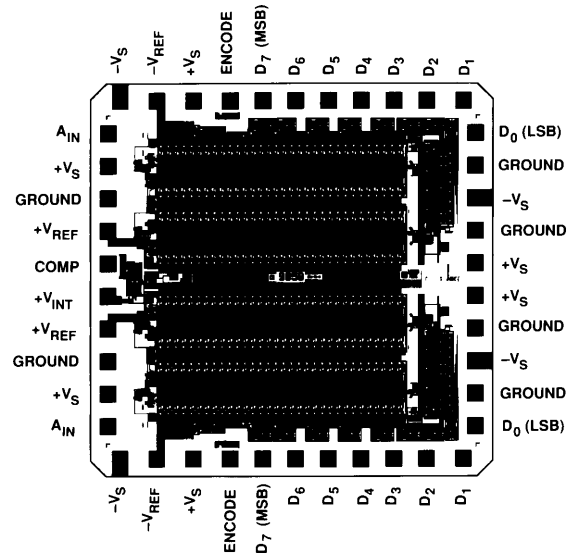


Figure 7. AD9058 Dynamic Performance vs. Analog Input Frequency

AD9058

MECHANICAL INFORMATION

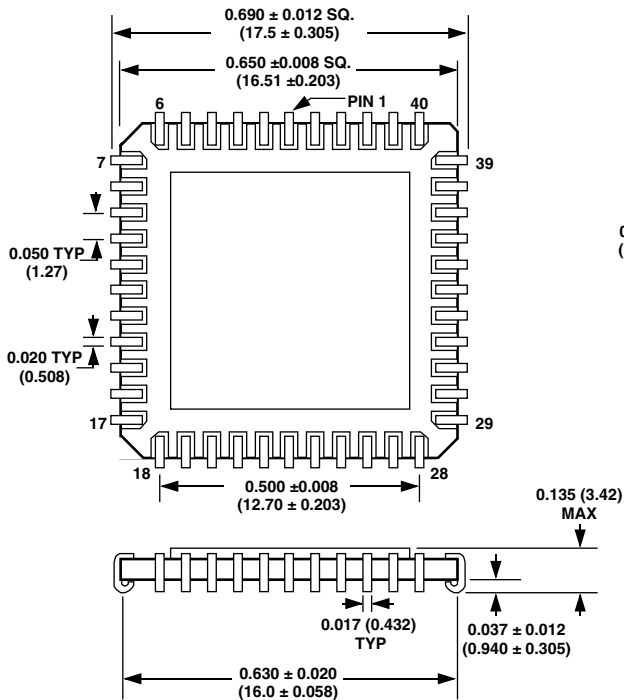
Die Dimensions 106 × 108 × 15 (±2) mils
 Pad Dimensions 4 × 4 mils
 Metalization Gold
 Backing None
 Substrate Potential -V_S
 Passivation Nitride
 Die Attach Gold Eutectic (Ceramic)
 Bond Wire 1–1.3 mil, Gold; Gold Ball Bonding



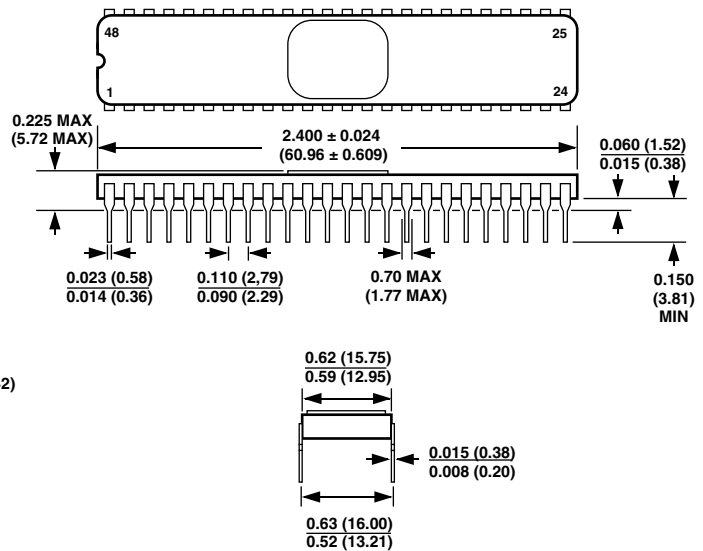
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Lead J-Leaded Ceramic (J-44) Package



48-Lead Hermetic Ceramic DIP (D-48) Package



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