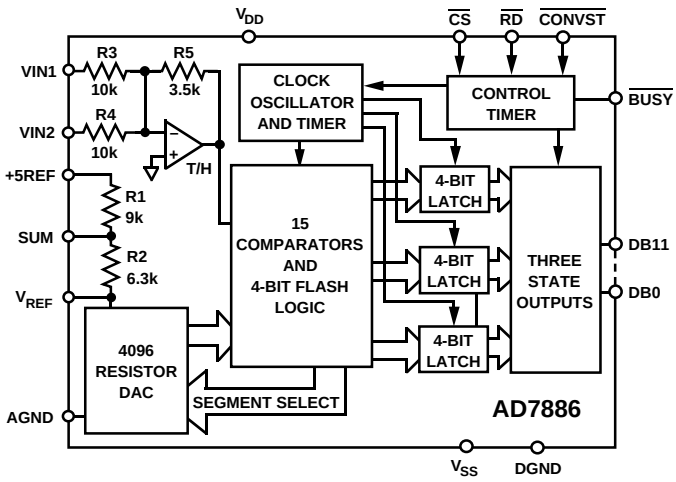
LC²MOS
12-Bit, 750 kHz/1 MHz, Sampling ADC
AD7886

FEATURES
750 kHz/1 MHz Throughput Rate
1 μs/750 ns Conversion Time
12-Bit No Missed Codes Over Temperature
67 dB SNR at 100 kHz Input Frequency
Low Power—250 mW typ
Fast Bus Access Time—57 ns max

APPLICATIONS
Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
DSP Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7886 is a 12-bit ADC with a sample-and-hold amplifier offering high speed performance combined with low power dissipation. The AD7886 is a triple pass flash ADC that uses 15 comparators in a 4-bit flash technique to achieve 12-bit accuracy in 1 μs/750 ns conversion time. An on-chip clock oscillator provides the appropriate timing for each of the three conversion stages, eliminating the need for any external clocks. Acquisition time of the sample-and-hold amplifier gives a resulting throughput rate of 750 kHz/1 MHz.*

The AD7886 operates from ±5 V power supplies. Pin-strappable inputs offer a choice of three analog input ranges: 0 V to 5 V, 0 V to 10 V or ±5 V.

In addition to the traditional dc accuracy specifications such as linearity, offset and full-scale errors, the AD7886 is also specified for dynamic performance parameters, including harmonic distortion and signal-to-noise ratio.

The AD7886 has a high speed digital interface with three-state data outputs. Conversion control is provided by a $\overline{\text{CONVST}}$ input. Data access is controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs, standard microprocessor signals. The data access time of less than 57 ns means that the AD7886 can interface directly to most modern microprocessors, including DSP processors.

***Contact your local salesperson for further information on the 1 MHz version.**

The AD7886 is fabricated in Analog Devices' Linear Compatible CMOS process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic.

The AD7886 is available in both a 28-pin DIP and a 28-pin leaded chip carrier.

PRODUCT HIGHLIGHTS

1. Fast 1.33 μs/1 μs Throughput Time.
   Fast throughput time makes the AD7886 suitable for a wide range of data acquisition applications.
2. Dynamic Specifications for DSP Users.
   The AD7886 is specified for ac parameters, including signal-to-noise ratio, harmonic distortion and intermodulation distortion. Key digital timing parameters are also tested and guaranteed over the full operating temperature range.
3. Fast Microprocessor Interface.
   Standard control signals, $\overline{\text{CS}}$ and $\overline{\text{RD}}$, and fast bus access times make the AD7886 easy to interface to microprocessors.
4. Low Power.
   LC²MOS fabrication process gives low power dissipation of 250 mW.

REV. B

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AD7886–SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, V_{REF} = –3.5 V, connected as shown in Figure 2. All Specifications T_{MIN} to T_{MAX} unless otherwise noted. Specifications apply for 750 kHz version.)

Parameter	J Version[1]	K, B Versions[1]	T Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal-to-Noise Ratio[3] (SNR)	65	67	65	dB min	VIN = 100 kHz Sine Wave, f_{SAMPLE} = 750 kHz
Total Harmonic Distortion (THD)	–75	–75	–75	dB typ	VIN = 100 kHz Sine Wave, f_{SAMPLE} = 750 kHz
Peak Harmonic or Spurious Noise	–77	–77	–77	dB typ	VIN = 100 kHz Sine Wave, f_{SAMPLE} = 750 kHz
Intermodulation Distortion (IMD)					
Second Order Terms	–80	–80	–80	dB typ	f_a = 96 kHz, f_b = 103 kHz, f_{SAMPLE} = 750 kHz
Third Order Terms	–80	–80	–80	dB typ	
ACCURACY					
Resolution	12	12	12	Bits	
Integral Linearity T_{MIN} to T_{MAX}		±2	±2	LSB max	
Minimum Resolution for Which					
No Missing Codes Are Guaranteed	12	12	12	Bits	
Unipolar Offset Error @ +25°C	±5	±5	±5	LSB max	Input Range: 0 V to 5 V or 0 V to 10 V
T_{MIN} to T_{MAX}	±5	±5	±5	LSB max	
Bipolar Offset Error @ +25°C	±5	±5	±5	LSB max	Input Range: ±5 V
T_{MIN} to T_{MAX}	±5	±5	±5	LSB max	
Unipolar Gain Error @ +25°C	±5	±5	±5	LSB max	Input Range: 0 V to 5 V or 0 V to 10 V
T_{MIN} to T_{MAX}	±5	±5	±5	LSB max	
Bipolar Gain Error @ +25°C	±5	±5	±5	LSB max	Input Range: ±5 V
T_{MIN} to T_{MAX}	±5	+5	±5	LSB max	
ANALOG INPUT					
Unipolar Input Current	1.5	1.5	1.5	mA max	Input Ranges: 0 V to 5 V or 0 V to 10 V
Bipolar Input Current	±0.75	±0.75	±0.75	mA max	Input Range: ±5 V
REFERENCE INPUT					
V_{REF}	–3.5	–3.5	–3.5	Volts	±2% For Specified Performance
Input Reference Current	–10	–10	–10	mA max	
R1, Resistance	9	9	9	kΩ nom	±25%
R2, Resistance	6.3	6.3	6.3	kΩ nom	±25%
R2/R1 Ratio	0.7	0.7	0.7	nom	±0.1%
POWER SUPPLY REJECTION					
V_{DD} Only, (FS Change)	0.5	0.5	0.5	LSB typ	V_{SS} = –5 V, V_{DD} = +4.75 V to +5.25 V
V_{SS} Only, (FS Change)	0.5	0.5	0.5	LSB typ	V_{DD} = +5 V, V_{SS} = –4.75 V to –5.25 V
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	10	pF max	
LOGIC OUTPUTS					
DB11–DB0, $\overline{BUSY}$					
Output High Voltage, V_{OH}	4	4	4	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating-State Leakage Current	±10	±10	±10	pA max	
Floating-State Output Capacitance[4]	15	15	15	pF max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	–5	–5	–5	V nom	±5% for Specified Performance
I_{DD}	35	35	35	mA max	Typically 25 mA, $\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = V_{DD}
I_{SS}	–35	–35	–35	mA max	Typically 25 mA, $\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = V_{DD}
Power Dissipation	250	250	250	mW typ	$\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = V_{DD}
	350	350	350	mW max	

NOTES

[1]Temperature ranges are as follows: J, K Versions: 0°C to +70°C; B Version: –40°C to +85°C; T Version: –55°C to + 125°C.

[2]Applies to all three input ranges, V_{IN} = 0 to FS, pk-to-pk V.

[3]SNR calculation includes distortion and noise components.

[4]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V)

Parameter	Limit at T_{MIN}, T_{MAX} (J, K Versions)	Limit at T_{MIN}, T_{MAX} (B Version)	Limit at T_{MIN}, T_{MAX} (T Version)	Units	Conditions/Comments
t_1	50	50	50	ns min	$\overline{CONVST}$ Pulse Width
	1	1	1	Fs max	
t_2	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_3	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_4	**60**	**60**	**75**	ns min	$\overline{RD}$ Pulse Width
t_5	100	100	100	ns max	$\overline{CONVST}$ to $\overline{BUSY}$ Propagation Delay, (C_L = 10 pF)
t_6	**57**	**57**	**70**	ns max	Data Access Time After $\overline{RD}$
t_7[3]	**10**	**10**	**10**	ns min	Bus Relinquish Time After $\overline{RD}$
	50	**50**	**60**	ns max	
t_8	20	20	14	ns min	Data Setup Time Prior to $\overline{BUSY}$, (C_L = 20 pF)
	10	10	0	ns min	Data Setup Time Prior to $\overline{BUSY}$, (C_L = 100 pF)
t_9[3]	10	10	10	ns min	Bus Relinquish Time After $\overline{CONVST}$
	100	100	100	ns max	
t_{10}	0	0	0	ns min	$\overline{CS}$ High to $\overline{CONVST}$ Low
t_{11}	0	0	0	ns min	$\overline{BUSY}$ High to $\overline{RD}$ Low
t_{12}	250	250	250	ns typ	$\overline{BUSY}$ High to $\overline{CONVST}$ Low, SHA Acquisition Time
t_{13}	1.333	1.333	1.333	µs min	Sampling Interval
t_{CONV}	950	950	950	ns typ	Conversion Time
	1000	**1000**	**1000**	ns max	

NOTES
[1]Timing specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]t_6 is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[3]t_7 and t9 are derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the load capacitor, C_L. This means that the times, t_7 and t_9, quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

Specifications subject to change without notice.

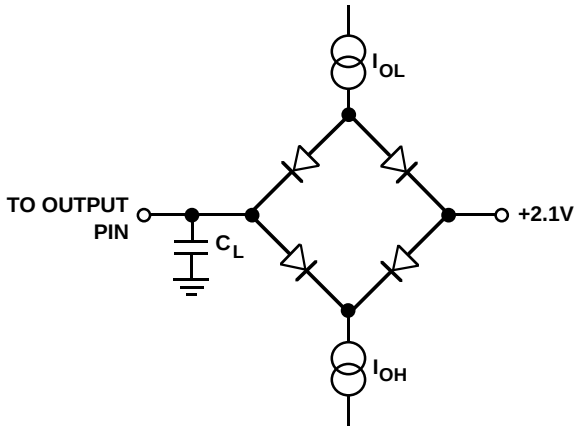


Figure 1. Load Circuit for Bus Access and Relinquish Time

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A= +25°C unless otherwise noted)

V_{DD} to AGND . . . . . –0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to –7 V
AGND to DGND . . . . . –0.3 V to V_{DD} +0.3 V
VIN1, VIN2, SUM, +5REF to AGND . . . . . –15 V to +15 V
V_{REF} to AGND . . . . . V_{SS} –0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND
CS, RD, CONVST . . . . . –0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND
DB0 to DB11, BUSY . . . . . –0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Commercial (J, K Versions) . . . . . 0°C to +70°C
Industrial (B Version) . . . . . –40°C to +85°C
Extended (T Version) . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to + 150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]If V_{SS} is open circuited with V_{DD} and AGND applied, the V_{SS} pin will be pulled positive, exceeding the Absolute Maximum Ratings. If this possibility exists, a Schottky diode from V_{SS} to DGND (cathode end to GND) ensures that the

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7886 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model[1, 2]	Temperature Range	SNR (dBs)	Integral Nonlinearity (LSBs)	Package Option[3]
AD7886JD	0°C to +70°C	65		D-28
AD7886KD	0°C to +70°C	67	±2.0	D-28
AD7886JP	0°C to +70°C	65		P-28A[2]
AD7886KP	0°C to +70°C	67	±2.0	P-28A[2]
AD7886BD	–40°C to +85°C	67	±2.0	D-28
AD7886TD	–55°C to +125°C	65	±2.0	D-28

NOTES
1Contact your sales office for availability of AD7886BD, AD7886TD and 1 MHz version.
[2]Analog Devices reserves the right to ship J-Leaded Ceramic Chip Carrier (JLCCC) in lieu of PLCC packages.
[3]D = Ceramic DIP; P = Plastic Leaded Chip Carrier.

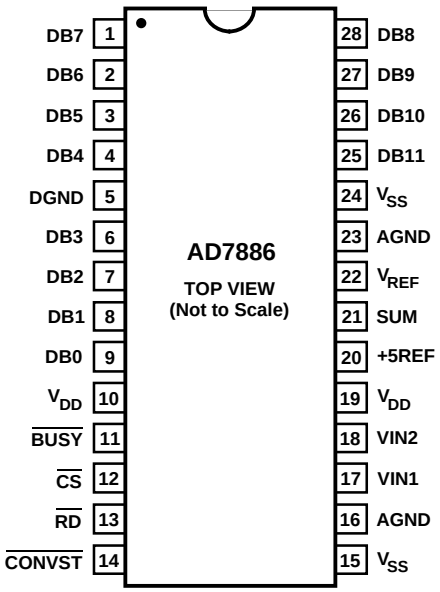
PIN FUNCTION DESCRIPTION

DIP Pin Number	Mnemonic	Description
Power Supply		
10 & 19	V_{DD}	Positive Power Supply, +5 V ± 5%. Both V_{DD} pins must be tied together.
15 & 24	V_{SS}	Negative Power Supply, –5 V ± 5%. Both V_{SS} pins must be tied together.
16 & 23	AGND	Analog Ground. Both AGND pins must be tied together.
5	DGND	Digital Ground.
Analog and Reference Inputs		
17 & 18	VIN	Analog Inputs, VIN1 and VIN2. The part can be pin strapped for any one of three analog input ranges;
20	+5REF	+5 V Reference input. This input is used in conjunction with SUM and V_{REF} inputs to scale an external +5 V reference to –3.5 V, the required reference for the part (see Figure 2).
21	SUM	Summing Point. This input is used in conjunction with +5REF and V_{REF} inputs to scale an external +5 V reference to –3.5 V, the required reference for the part (see Figure 2).
22	V_{REF}	Voltage Reference Input. The AD7886 is specified with V_{REF} = –3.5 V.
Interface and Control		
1–4,	DB7–DB4	Three-state data outputs.
6–9,	DB3–DB0	These outputs are controlled by $\overline{CS}$ and $\overline{RD}$. DB11 is the Most Significant Bit (MSB).
25–28	DB11–DB8	
11	$\overline{BUSY}$	$\overline{BUSY}$ Output indicates converter status. $\overline{BUSY}$ is low during conversion.
12	$\overline{CS}$	Chip Select Input. The device is selected when this input is low.
13	$\overline{RD}$	Read Input. This active low signal, in conjunction with $\overline{CS}$, is used to enable the output data three-state drivers.
14	$\overline{CONVST}$	Conversion Start Input. This input is used to start conversion.

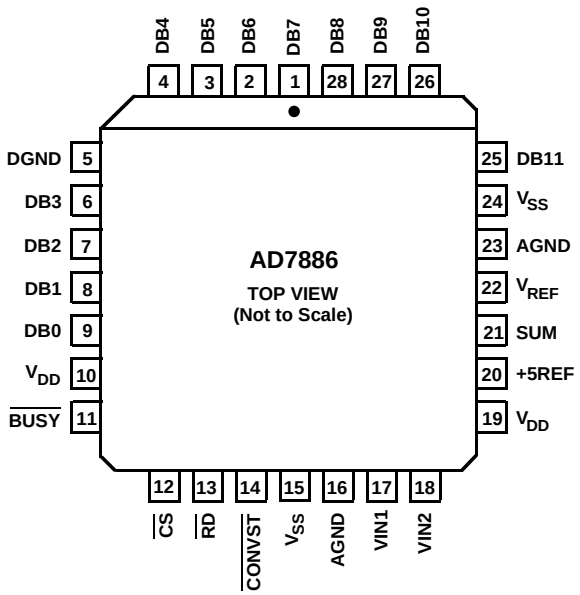
Range	Pin Strap	Signal Input
0 V to 5 V	Connect VIN2 to VIN1	VIN1 & VIN2
0 V to 10 V	Connect VIN2 to GND	VIN1
±5 V	Connect VIN2 to +5 V	VIN1

PIN CONFIGURATIONS

DIP



PLCC



TERMINOLOGY

Unipolar Offset Error

The ideal first code transition should occur when the analog input is 1 LSB above AGND. The deviation of the actual transition from that point is termed the offset error.

Bipolar Zero Error

The ideal midscale transition (i.e., 0111 1111 1111 to 1000 0000 0000) for the +5 V range should occur when the analog input is at zero volts. Bipolar zero error is the deviation of the actual transition from that point.

Gain Error

In the unipolar mode, gain error is measured with respect to the first and last code transition points. The ideal difference between these points is FS–2 LSBs. For bipolar applications, the gain error is measured from the midscale transition to both the first and last code transitions. The ideal difference in this case is FS/2–1 LSB. The gain error is defined as the deviation between the ideal difference, given above, and the measured difference. For the bipolar case, there are two gain errors; the figure in the specification page represents the worst case. Ideal FS depends on the +5REF input; for the 0 V to 5 V input, ideal FS = +5REF and for the 0 V to 10 V and +5 V ranges, ideal FS = 2 × + 5REF.

CONVERTER DETAILS

The AD7886 is a triple-pass flash ADC that uses 15 comparators in a 4-bit flash technique to perform the 12-bit conversion procedure. Each of the 4096 quantization levels is realized internally with a precision resistor DAC.

The fifteen comparators first compare the analog input voltage to the V_{REF}/16 voltages of the resistor array. This determines the four most significant bits and selects 1 out of 16 voltage segments. The comparators are then switched to 15 subvoltages on that segment to determine the next four bits and select 1 out of 256 voltage segments. A further switching of the comparators to another 15 subvoltages produces the complete 12-bit conversion result. The 12 bits of data are then stored internally in a three-state output latch.

REFERENCE INPUT

The AD7886 operates from a 3.5 V reference, which must be provided at the V_{REF} input. Two on-chip resistors for use with an external amplifier can be used for deriving 3.5 V from standard 5 V references. Figure 2 shows an example with the AD586 which a is a high performance voltage reference exhibiting excellent stability performance, 5 ppm/°C max. The external amplifier serves a second function of force/sensing the V_{REF} input. Force/sensing minimizes error contributions from

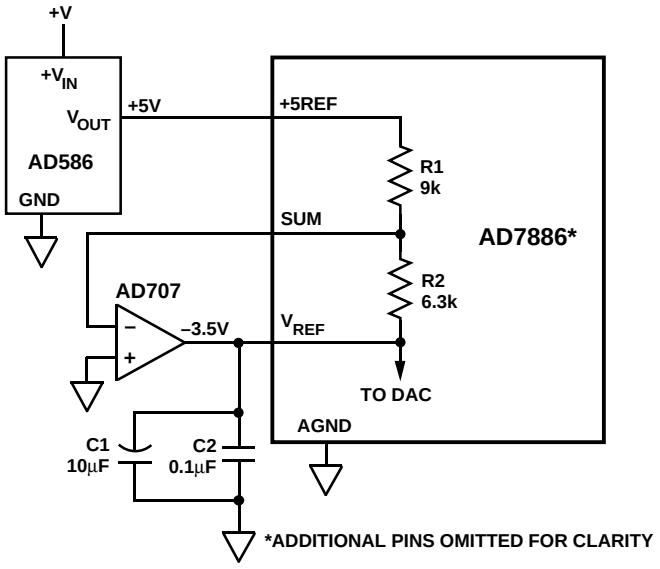


Figure 2. Typical Reference Circuitry

this amplifier typically by 20 MHz which is much greater than the Nyquist limit of the ADC; as a result, it can be used for undersampling applications. The track-and-hold amplifier acquires the input signal to 12-bit accuracy in less than 333 ns. The overall throughput time is equal to the conversion time plus the track/ hold amplifier acquisition time, which is 1.333 μs for the AD7886.

The operation of the track/hold amplifier is essentially transparent to the user. The track-to-hold transition occurs at the start of conversion on the falling edge of $\overline{\text{CONVST}}$. The conversion procedure does not start until the rising edge of $\overline{\text{CONVST}}$. The width of the $\overline{\text{CONVST}}$ pulse low time determines the track-to hold settling time. The track/hold reverts back to the track mode at the end of conversion when $\overline{\text{BUSY}}$ has returned high.

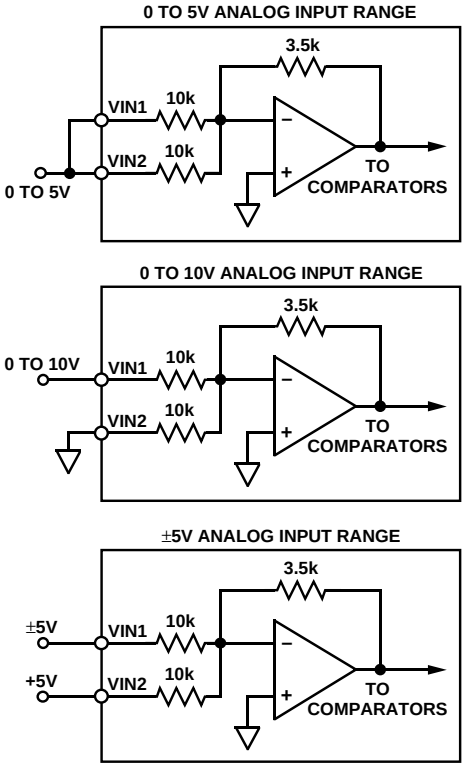


Figure 3. Analog Input Range Configurations

ANALOG INPUT RANGES

The AD7886 has three user selectable analog input ranges: 0 V to 5 V, 0 V to 10 V and ±5 V. Figure 3 shows how to configure the two analog inputs (VIN1 and VIN2) for these ranges.

UNIPOLAR OPERATION

Figure 4 shows a typical unipolar circuit for the AD7886. The ideal input/output characteristic is shown in Figure 5. The designed code transitions occur on integer multiples of 1 LSB.

The output code is natural binary with 1 LSB = FS/4096. FS is either +5 V or +10 V, depending on how the analog inputs are configured.

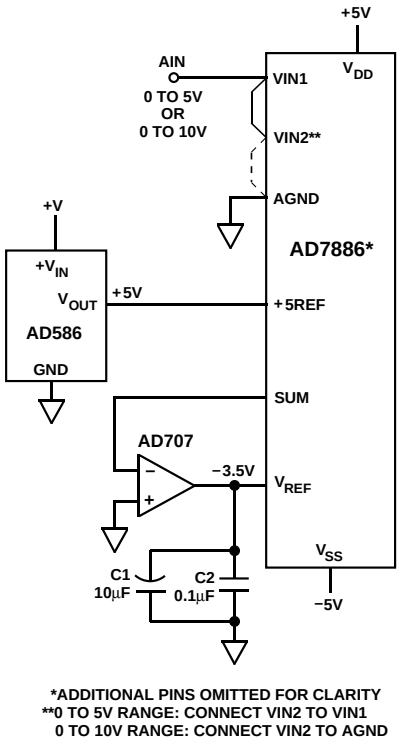


Figure 4. Unipolar Operation

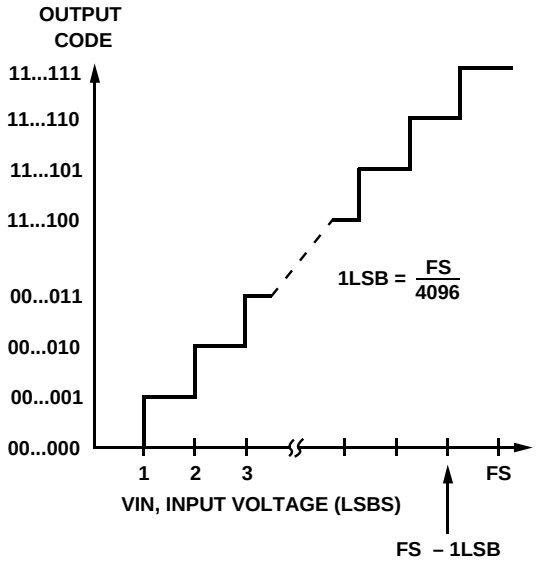


Figure 5. Ideal Input/Output Transfer Characteristic for Unipolar Operation

OFFSET AND GAIN ADJUSTMENT

In most digital signal processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can usually be eliminated in the analog domain by ac coupling. Full-scale errors do not cause problems as long as the input signal is within the full dynamic range of the ADC. For applications requiring that the input signal range match the full analog input dynamic range of the ADC, offset and full-scale errors must be adjusted to zero.

UNIPOLAR OFFSET AND GAIN ERROR ADJUSTMENT

If absolute accuracy is an application requirement, offset and gain can be adjusted to zero. Offset error must be adjusted before gain error. Zero offset is achieved by adjusting the offset of the op amp driving the analog input (i.e., A1 in Figure 6). For zero offset error, apply a voltage of 1 LSB to AIN and adjust the op amp offset until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

0 V to 5 V Range: 1 LSB = 1.22 mV
0 V to 10 V Range: 1 LSB = 2.44 mV

For zero gain, error apply an analog input voltage equal to FS–1 LSB (last code transition) at AIN and adjust R3 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

0 V to 5 V Range: FS–1 LSB = 4.99878 V

0 V to 10 V Range: FS–1 LSB = 9.99756 V

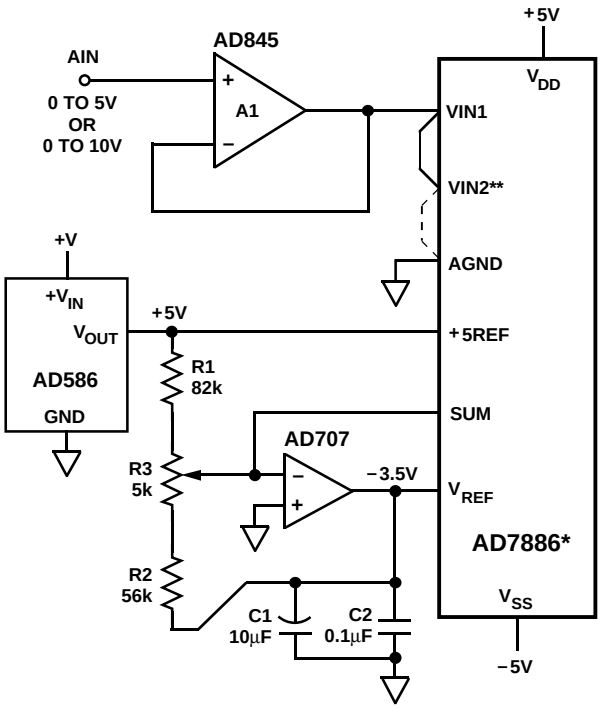


Figure 6. Unipolar Operation with Gain Error Adjust

BIPOLAR OPERATION

Bipolar operation is achieved by providing a +10 V span on the VIN1 input while offsetting the VIN2 input by +5 V. A typical circuit is shown in Figure 7. The output code is offset binary. The ideal input/output transfer characteristic is shown in Figure 8. The LSB size is (10/4096) V = 2.44 mV.

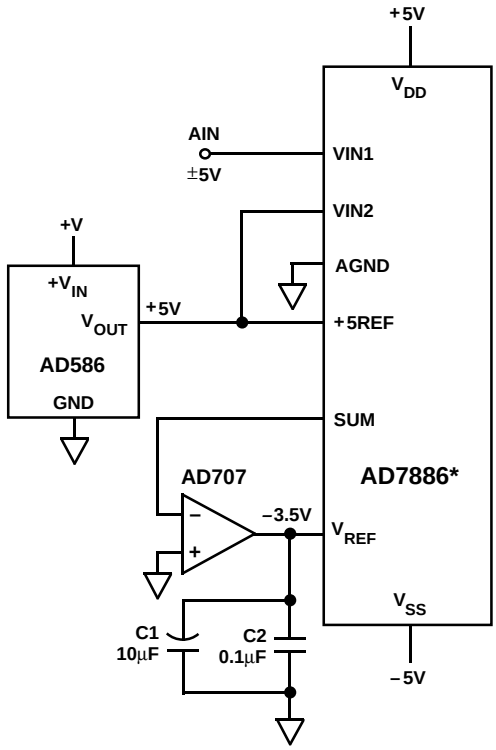


Figure 7. Bipolar Operation

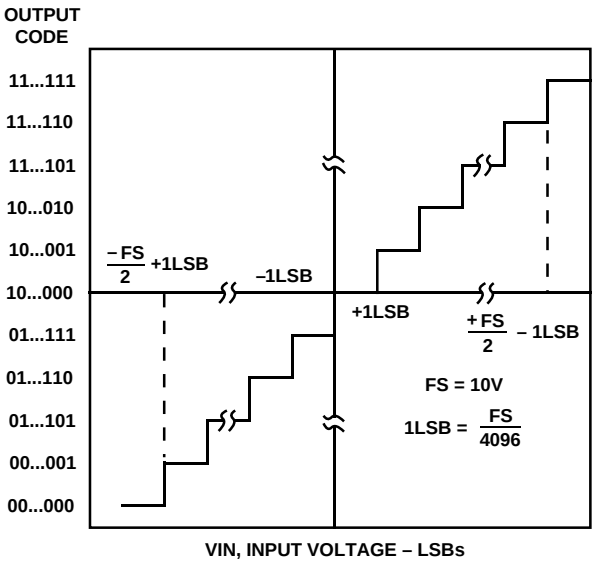


Figure 8. Ideal Input/Output Characteristics for Bipolar Operation

BIPOLAR OFFSET AND GAIN ADJUSTMENT

In applications where absolute accuracy is important, offset and gain error can be adjusted to zero. Offset is adjusted by trimming the voltage at the VIN1 or VIN2 input when the analog input is at zero volts. This can be achieved by adjusting the offset of an external amplifier used to drive either of these inputs (see A1 in Figure 9). The trim procedure is as follows:

Apply zero volts at AIN and adjust the offset of A1 until the ADC output code flickers between 0111 1111 1111 and 1000 0000 0000.

Gain error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). Adjusting the reference, as in Figure 9, will trim the positive gain error only. The trim procedure is as follows:

Apply a voltage of 4.99756 V, (FS/2–1 LSB) at AIN and adjust R3 until the output code flickers between 1111 1111 1110 and 1111 11111111.

If the first code transition needs adjusting, a gain trim must be included in the analog signal path. The trim procedure will then consist of applying an analog signal of –4.99756 V (–FS/2+1 LSB) and adjusting the trim until the output code flickers between 0000 0000 0000 and 0000 0000 0001.

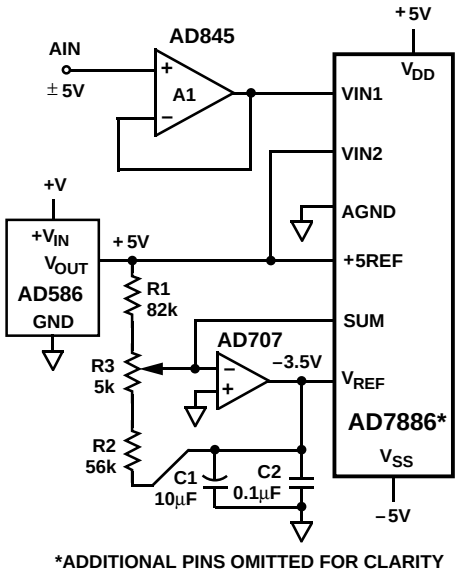


Figure 9. Bipolar Operation with Gain Error Adjust

TIMING AND CONTROL

Conversion start is controlled by the $\overline{\text{CONVST}}$ input (see Figures 10 and 11). A high to low going edge on the $\overline{\text{CONVST}}$ input puts the track/hold amplifier into the hold mode. The ADC conversion procedure does not begin until a rising $\overline{\text{CONVST}}$ pulse edge occurs. The width of the $\overline{\text{CONVST}}$ pulse low time determines the track-to-hold settling time. The $\overline{\text{BUSY}}$ output, which indicates the status of the ADC, goes low while conversion is in progress. At the end of conversion $\overline{\text{BUSY}}$ returns high, indicating that new data is available on the AD7886's output latches. The track/hold amplifier returns to the track mode at the end of conversion and remains there until the next $\overline{\text{CONVST}}$ pulse. Conversion starts must not be attempted while conversion is in progress as this will cause erroneous results.

Data read operations are controlled by the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs. These digital inputs, when low, enable the AD7886's three-state output latches. Note, these latches cannot be enabled during conversion. In applications where $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are tied permanently low, as in Figure 11, the data bus will go into the three-state condition at the start of conversion and return to its active state when conversion is complete. Tying $\overline{\text{CS}}$ and $\overline{\text{RD}}$ permanently low is useful when external latches are used to store the conversion results. The data bus becomes active before $\overline{\text{BUSY}}$ returns high at the end of conversion, so that $\overline{\text{BUSY}}$ can be used as a clocking signal for the external latches.

A typical DSP application would have a timer connected to the $\overline{\text{CONVST}}$ input for precise sampling intervals. $\overline{\text{BUSY}}$ would be connected to the interrupt of a microprocessor that would be asserted at the end of every conversion. The microprocessor would then assert the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs and read the data from the ADC. For applications where both data reading and conversion control need to be managed by a microprocessor, a $\overline{\text{CONVST}}$ pulse can be decoded from the address bus. One decoding possibility is that a write instruction to the ADC address starts a conversion, and a read instruction reads the conversion result.

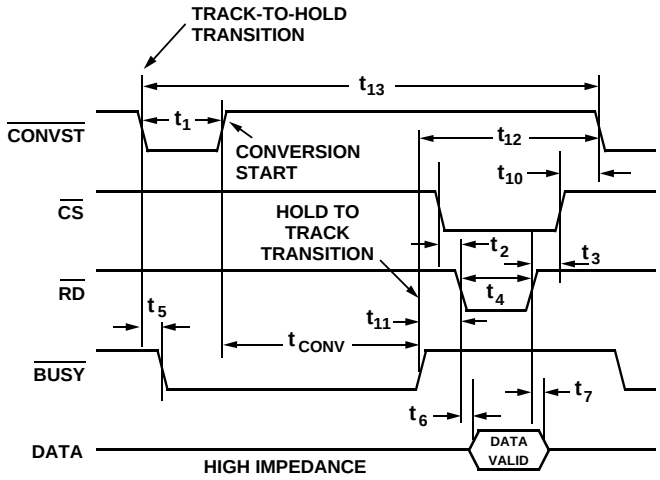


Figure 10. Conversion Start and Data Read Timing Diagram

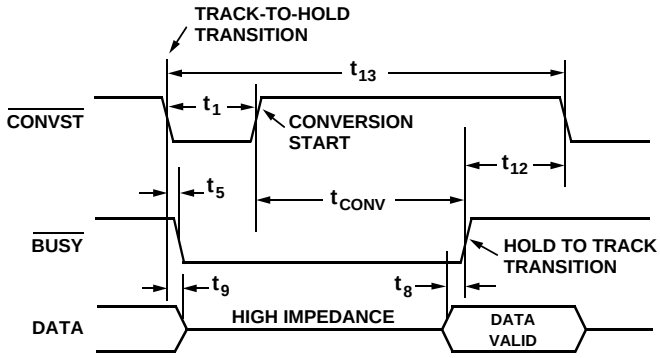


Figure 11. Conversion Start and Data Read Timing Diagram, ($\overline{\text{CS}}$ = $\overline{\text{RD}}$ = 0 V)

AD7886 DYNAMIC SPECIFICATIONS

The AD7886 is specified for dynamic performance specifications as well as traditional dc specifications such as integral and differential nonlinearity. These ac specifications are required for signal processing applications such as speech recognition, spectrum analysis and high speed modems. These applications require information on the ADC's effect on the spectral content of the input signal. Hence, the parameters for which the AD7886 is specified include SNR, harmonic distortion, intermodulation distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (FS/2), excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave input is given by

$$SNR = (6.02N + 1.76)\ dB \quad (1)$$

where N is the number of bits. Thus, for an ideal 12-bit converter, SNR = 74 dB.

The output spectrum from the ADC is evaluated by applying a sine wave signal of very low distortion to the VIN input, which is sampled at a 750 kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 12 shows a typical 2048 point FFT plot with an input signal of 100 kHz and a sampling frequency of 750 kHz.

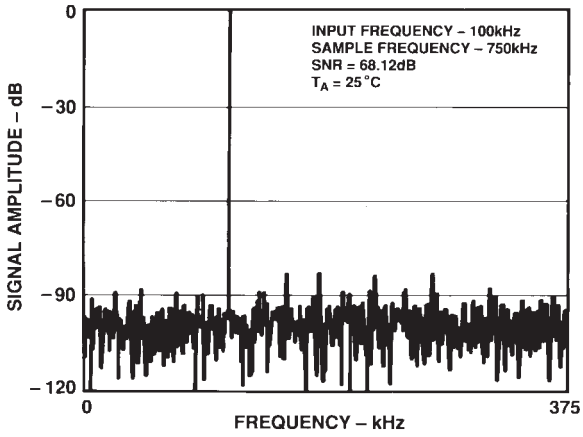


Figure 12. AD7886 FFT Plot

The SNR obtained from this graph is 68 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

Effective Number of Bits

The formula given in Equation 1 relates the SNR to the number of bits. Rewriting the formula, as in Equation 2, it is possible to obtain a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \quad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Figure 13 shows a typical plot of effective number of bits versus frequency for a sampling frequency of 750 kHz. Input frequency range for this particular graph was limited by the test equipment to FS/4. The effective number of bits typically falls between 10.9 and 11.2, corresponding to SNR figures of 67.38 dB and 69.18 dB.

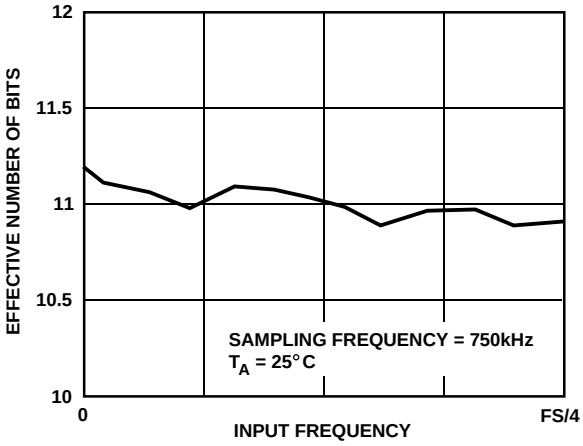


Figure 13. Effective Number of Bits vs. Frequency

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7886, THD is defined as

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1} \quad (3)$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic. The *THD* is also derived from the FFT plot of the ADC output spectrum.

Intermodulation Distortion (IMD)

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb) while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

Using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental, expressed in dBs. In this case, the input consists of two, equal amplitude, low distortion sine waves. Figure 14 shows a typical IMD plot for the AD7886.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to FS/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be

determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, the peak will be a noise peak.

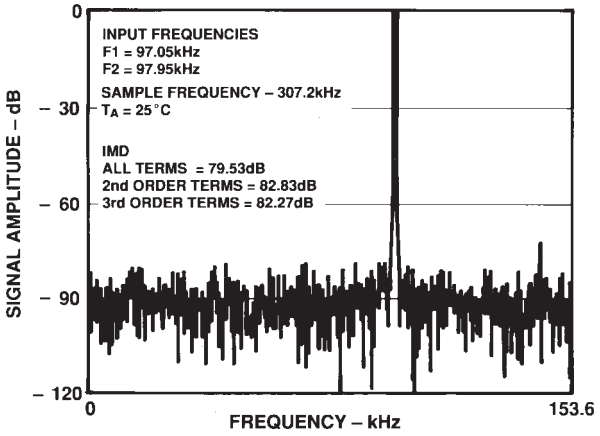


Figure 14. AD7886 IMD Plot

MICROPROCESSOR INTERFACING

The AD7886 is designed to interface to microprocessors as a memory mapped device. Its $\overline{CS}$ and $\overline{RD}$ control inputs are common to all memory peripheral interfacing. Figures 15 to 21 demonstrate typical interfaces for the AD7886.

AD7886–TMS320C10/TMS32020

Figures 15 and 16 show typical interfaces for the TMS320C10 and the TMS32020 DSP processors. An external timer controls conversion start to the processor. At the end of each conversion, the ADC's $\overline{BUSY}$ output interrupts the microprocessor. The conversion result can then be read from the ADC with the following instruction:

IN D,ADC (ADC = ADC address)

AD788S ADSP-2100/TMS320C25/DSP56000

Some of the faster DSP processors have data access times outside the capabilities of the AD7886. Interfacing to such processors requires the use of either a single WAIT state or external latches. Examples are shown in Figures 17, 18 and 19.

The use of a single WAIT state for the TMS320C25 and the ADSP-2100 interfaces extends the read instruction to the ADC by one processor CLK OUT cycle. In the DSP56000 example, the ADC's data is first clocked into 74HC374 latches before being read by the processor. The AD7886's $\overline{CS}$ and $\overline{RD}$ inputs are tied permanently low, and the rising edge of $\overline{BUSY}$ updates the latches at the end of conversion. Both methods of overcoming the very fast data access time required by these processors are interchangeable, i.e., a WAIT state can be used for the DSP56000, eliminating the need for latches or vice or versa, for the other two interfaces.

For all three interfaces, an external timer controls conversion start; the processor is interrupted at the end of each conversion by the ADC's $\overline{BUSY}$ output. The following instruction then reads data from the ADC:

ADSP-2100 – MR = DM(ADC)
TMS320C25 – IN D,ADC
DSP56000 – MOVEP Y:ADC,XO
Assuming the ADC is memory mapped into the top 64 locations in Y memory space. (ADC = ADC address)

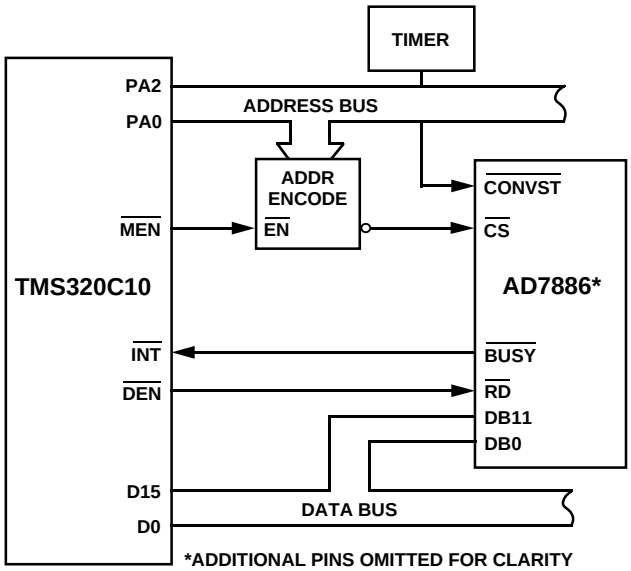


Figure 15. AD7886-TMS320C10 Interface

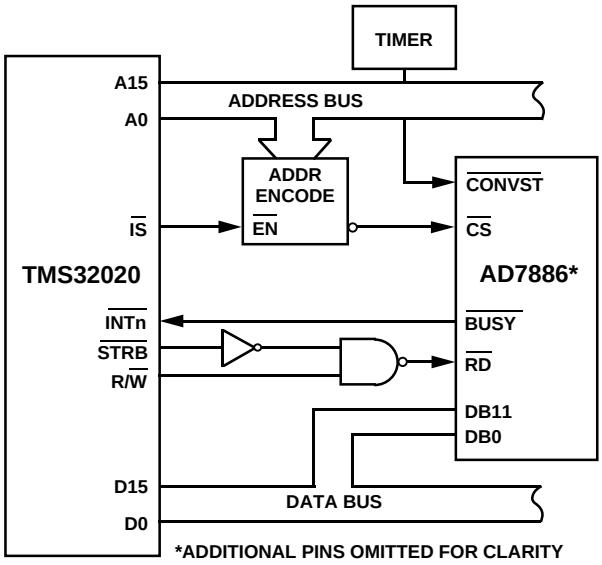


Figure 16. AD7886-TMS32020 Interface

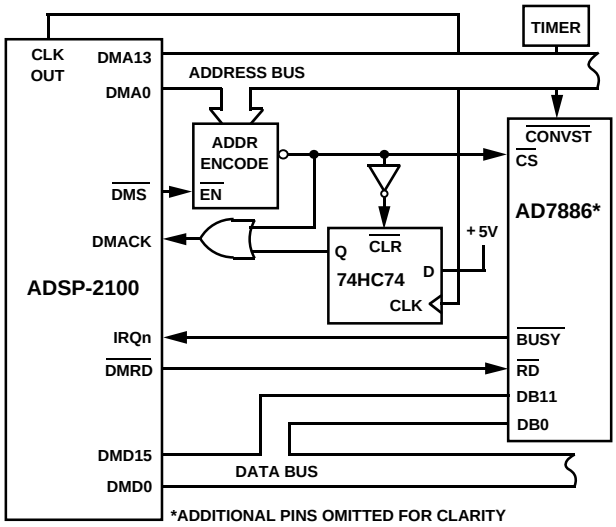


Figure 17. AD7886–ADSP-2100 Interface

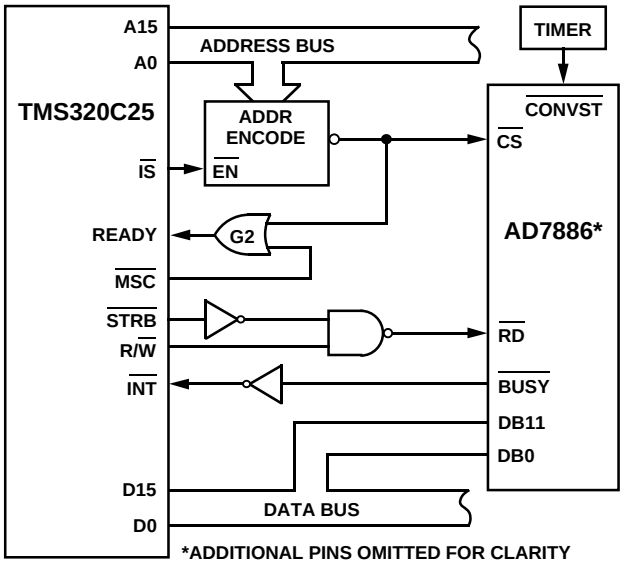


Figure 18. AD7886–TMS320C25 Interface

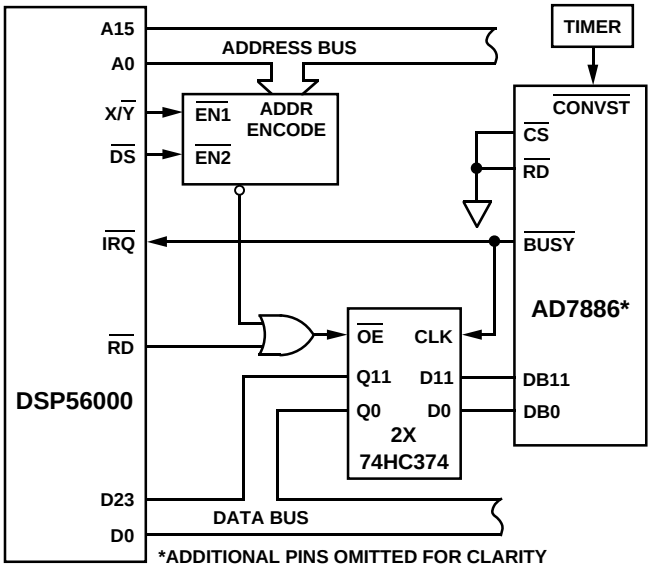


Figure 19. AD7886–DSP56000 Interface

AD7886–MC68000

Applications requiring conversions to be initiated by the microprocessor rather than an external timer may decode a $\overline{\text{CONVST}}$ signal from the address bus. An example is given in Figure 20 with the MC68000 processor. A write instruction starts conversion while a read instruction reads the data when conversion is complete. A delay at least as long as the ADC conversion time must be allowed between initiating a conversion and reading the ADC data into the processor. In Figure 20, $\overline{\text{BUSY}}$ is used to drive the processor into a WAIT state if the processor attempts to read data before conversion is complete.

Conversion is initiated with a write instruction to the ADC:

Move.W D0,ADC (ADC = ADC address)

Data is transferred to the processor with a read instruction; $\overline{\text{BUSY}}$ will force the processor to WAIT for the end of conversion if a conversion is in progress.

Move.W ADC,DO (ADC = ADC address)

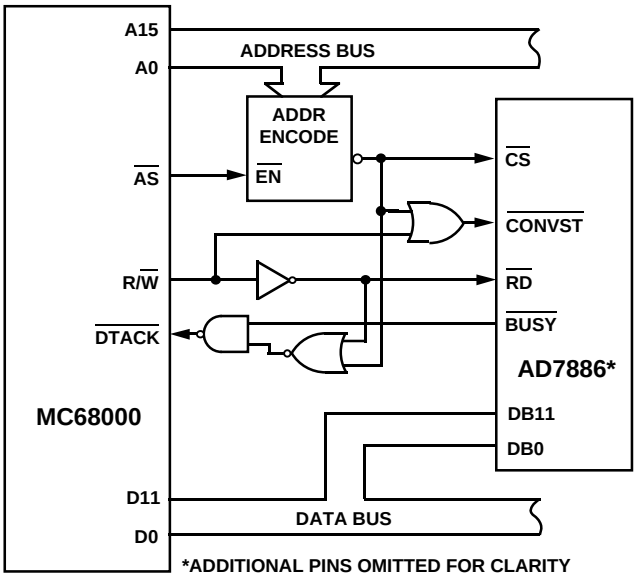


Figure 20. AD7886–MC68000 Interface

AD7886–Z-80/8085A

For 8-bit processors, an external latch is required to store four bits of the conversion result (4 LSBs in Figure 21). The data is then read in two bytes: one read from the ADC and a second from the latch.

Figure 21 shows a typical interface suitable for the Z-80 or the 8085A. Not shown in the Figure is the 8-bit latch needed to demultiplex the 8085A common address/data bus. The following LOAD instruction reads the conversion result into the HL register pair:

For the 8085A–LHLD (ADC) (ADC = ADC address)
For the Z-80–LDHL (ADC) (ADC = ADC address)

This is a two byte read instruction. The first byte to be read has to be the high byte (DB11 to DB4). At the end of the first read operation, the rising edge of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ clocks the 4 LSBs into 74HC374 latches. The second byte (4 LSBs) is then read from these latches.

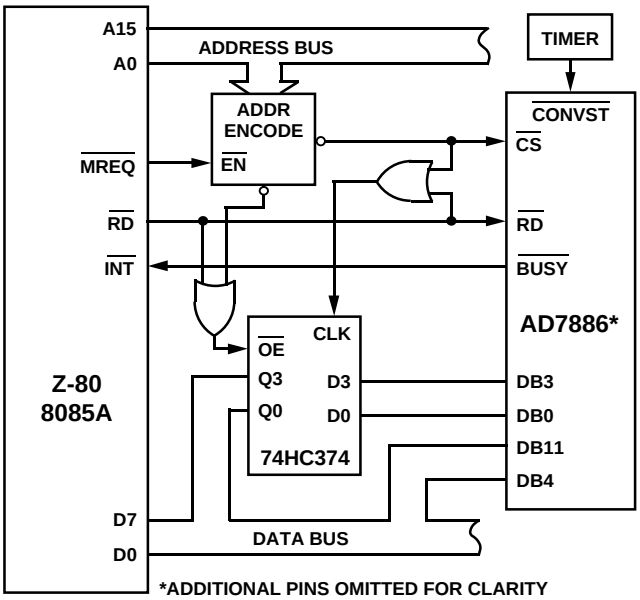


Figure 21. AD7886–Z-80/8085A Interface

APPLICATION HINTS

Good printed circuit (PC) board layout is as important as the circuit design itself in achieving high speed A/D performance. The AD7886's comparators are required to make bit decisions on an LSB size of 1.22 mV. To achieve this, the designer has to be conscious of noise in both the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator, causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors that influence any ADC, and a proper PC board layout that minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at the AD7886 AGND or as close as possible to the AD7886. Connect all other grounds and the AD7886 DGND to this single analog ground point. Do not connect any other digital grounds to this analog ground point.

Because low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layout of Figures 25 and 26 have both analog and digital ground planes that are kept separated and only joined together at the AD7886 AGND.

NOISE

Keep the input signal leads to VIN and signal return leads from AGND as short as possible to minimize input noise coupling. In applications where this is not possible, use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

DATA ACQUISITION BOARD

Figure 23 shows a typical data acquisition circuit designed for a microprocessor environment. The corresponding PC board layout and silkscreen are shown in Figures 24 to 26.

The analog input to the AD7886 is buffered with an AD845 op amp. A component grid is provided near the analog input on the PC board that may be used for an antialiasing filter or any other conditioning circuitry. To facilitate this option, a link (labeled LK4) is required on the analog input.

An AD586 voltage reference and an AD707 op amp provide the appropriate reference biasing required by the AD7886. The ADC's data outputs are buffered with 74HC374 latches. These provide data bus isolation and improve data access time. Data access time is reduced to under 30 ns, allowing interfacing to virtually any microprocessor, including the high speed DSP processors. Data format can be either a complete parallel load for 16-bit processors or a two-byte load for 8-bit processors.

INTERFACE CONNECTIONS

There are two connectors labeled SKT3 and SKT4. SKT3 is a 96-contact (3-row) connector, which is directly compatible with the ADSP-2100 evaluation board prototype expansion connector. The expansion connector on the ADSP-2100 board has eight decoded chip enable outputs labeled $\overline{ECE1}$ to $\overline{ECE8}$. $\overline{ECE6}$ is used to select the AD7886 data acquisition board. To avoid selecting on-board RAM sockets at the same time, LK6 on the ADSP-2100 board must be removed. In addition, the ADSP-2100 expansion connector has four interrupts labeled $\overline{EIRQ0}$ to $\overline{EIRQ3}$. The AD7886's $\overline{BUSY}$ output connects to $\overline{EIRQ0}$. SKT3 pinout is shown in Figure 23.

Data format to the ADSP-2100 connector is left justified, i.e., DB11 of the conversion result is connected to DMD15 of the connector. DMD3 to DMD0 are always zero.

SKT4 is a 22-way (2 row) pin-header connector. This connector contains all the signal contacts as SKT3 with the exception of EDMACK and the 4 trailing zeros of the 16-bit data word. Only the 12-bit conversion results go to SKT4. The pinout is shown in Figure 22.

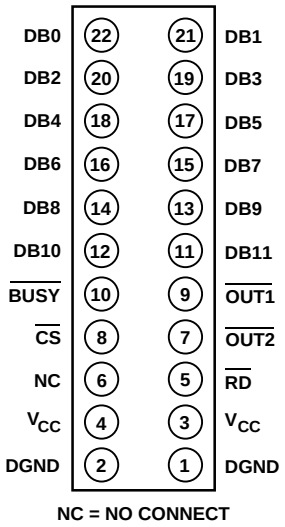


Figure 22. SKT4 Pinout

POWER SUPPLY CONNECTIONS

The PC board requires two analog power supplies and one 5 V digital supply. Connections to the analog supply are made directly to the PC board as shown on the silkscreen in Figure 24. The connections are labeled V+ and V–, and the range for both of these supplies is 12 V to 15 V. Connection to the 5 V digital supply is made through either of the two connectors (SKT3 or SKT4). The +5 V analog supplies required by the AD7886 are generated from voltage regulators on the V– and V+ power supplies.

LINK OPTIONS

There are five link options, labeled LK1 to LK5, which must be set before using the board.

LK1 Input Range Select

The AD7886 can accommodate three possible analog input ranges: 0 V to 5 V, 0 to 10 V and +5 V. The link options are as follows:

0 V to 5 V	Use Link C
0 V to 10 V	Use Link B
±5 V	Use Link A

LK2 and LK3 Control Input Options

The evaluation board includes two latches to increase the data access time when interfacing to the faster DSP machines. If these latches are not required, they may be removed and the data digital paths shorted out, i.e., latch inputs Dx shorted to outputs Qx using wire links in the latch sockets. When using the latches, the AD7886 control inputs, $\overline{CS}$ and $\overline{RD}$, must be tied low via links 2 and 3. The latches are updated by the rising edge of the $\overline{BUSY}$ signal at the end of every conversion. Data is then read by asserting the latch output enable signals. The alternative is to remove the latches and assert the ADC's control inputs from either of the connectors, SKT3 or SKT4, as outlined in the data sheet.

Latches Included	Latches Removed
Insert Link 2	Remove Link 2
Insert Link 3	Remove Link 3

LK4 Analog Input Option

LK4 connects the analog input to a component grid or to a buffer amplifier that drives the ADC input.

LK5

Data format can be 16-bits parallel or two bytes for 8-bit processors. There are two data enable controls for the 74HC374 latches, labeled $\overline{OUT1}$ and $\overline{OUT2}$. $\overline{OUT1}$ enables the 8 MSBs (IC8), and $\overline{OUT2}$ enables the 4 LSBs (IC9). Link options are: for 16-bit format, include LK5, for a two byte read format, remove LK5.

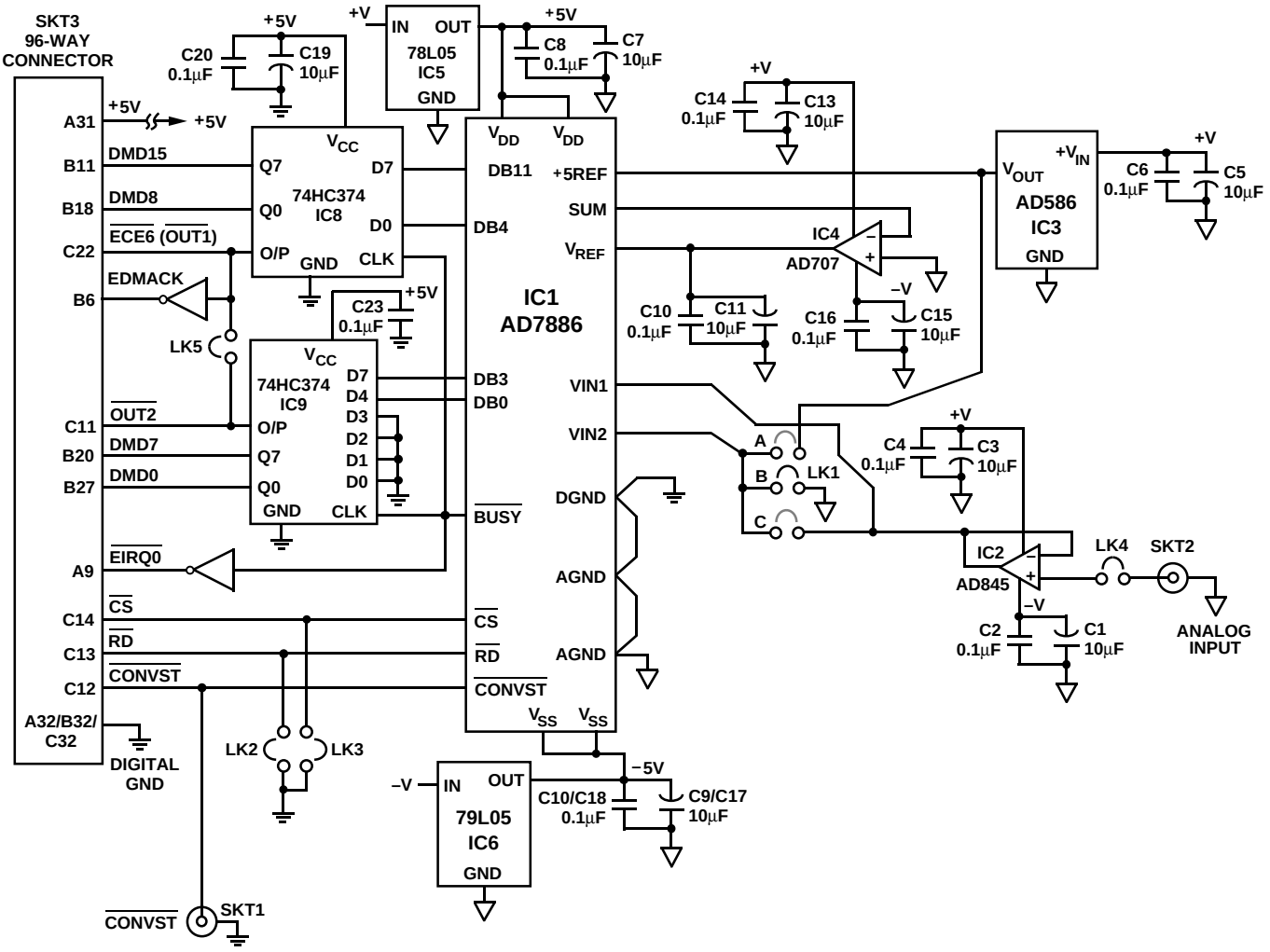


Figure 23. Data Acquisition Circuit Using the AD7886

COMPONENT LIST

IC1	AD7886, 12-Bit Sampling ADC
IC2	AD845, Op Amp
IC3	AD586, Precision Voltage Reference
IC4	AD707, Op Amp
IC5	MC78L05, + 5 V Regulator
IC6	MC79L05, –5 V Regulator
IC7	74HC04, Hex Inverter
IC8, IC9	74HC374, Octal Latches with Three-State Outputs
C1, C3, C5, C7, C9, C11, C13, C15 C17, C19, C21	10 µF Capacitors
C2, C4, C6, C8, C10, C12, C14, C16, C18, C20, C22, C23	0.1 µF Capacitors
SKT1, SKT2	BNC Sockets
SKT3	96-Contact (3 Row) Eurocard Connector
SKT4	22-Way (2 Row) Pin Header and Socket

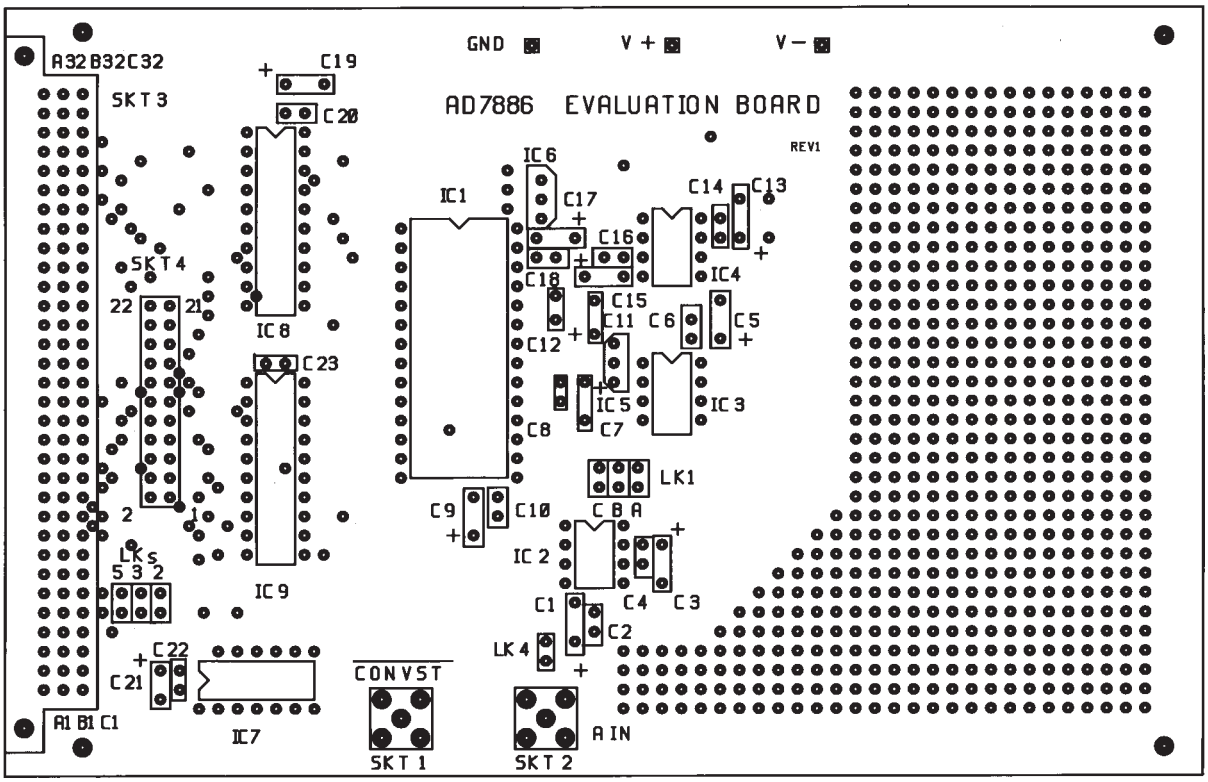


Figure 24. PC Board Silkscreen for Figure 23

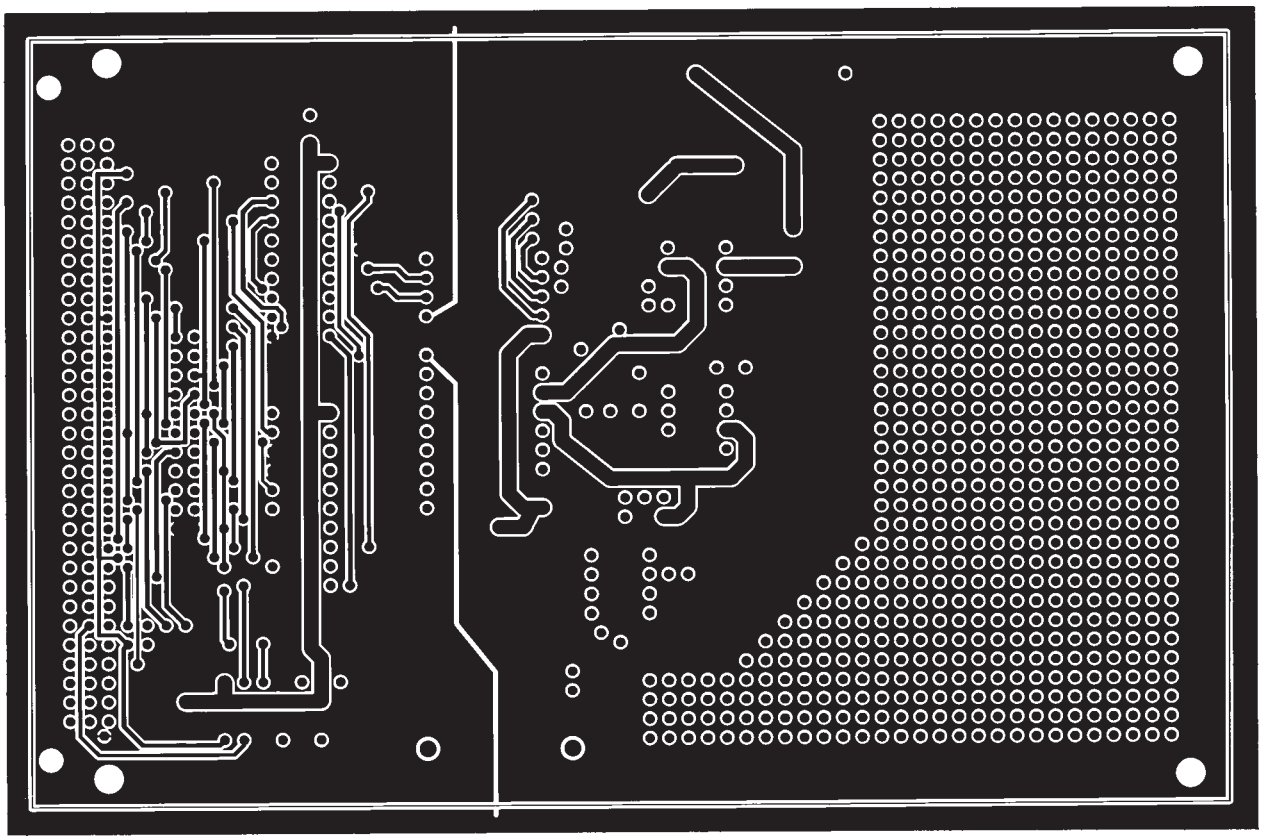


Figure 25. PC Board Component Side Layout for Figure 23

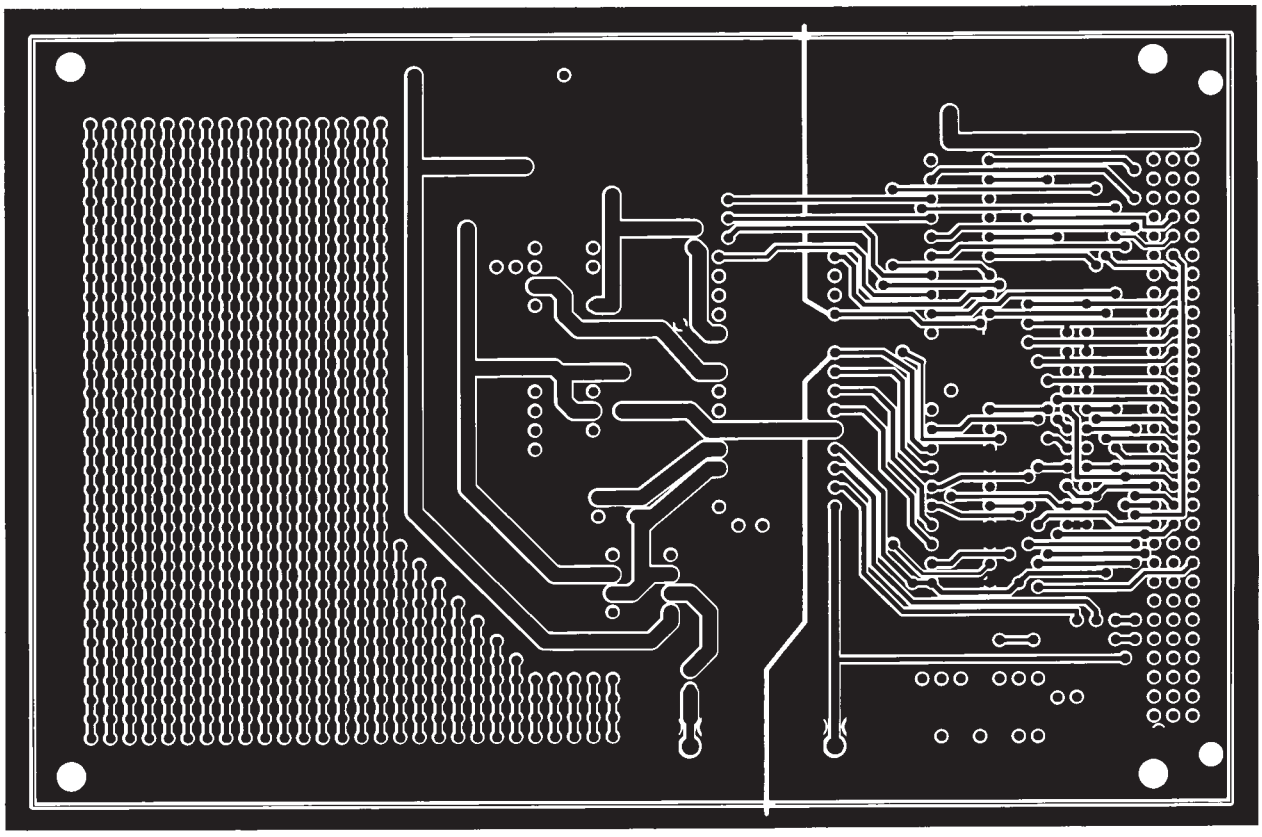
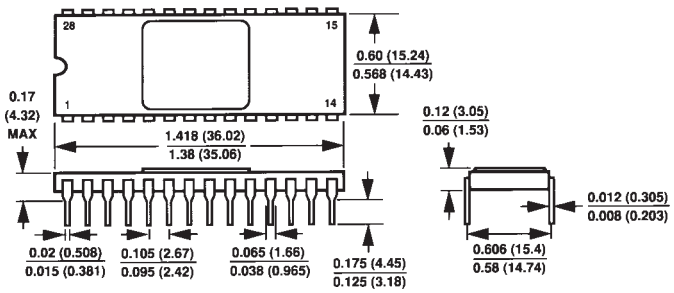


Figure 26. PC Board Solder Side Layout for Figure 23

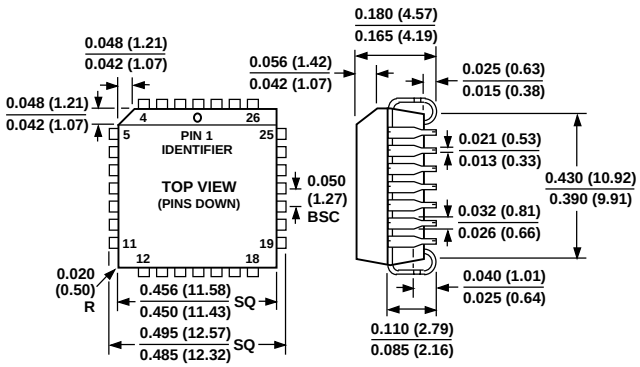
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Pin Ceramic DIP (D-28)



28-Pin PLCC (P-28A)



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