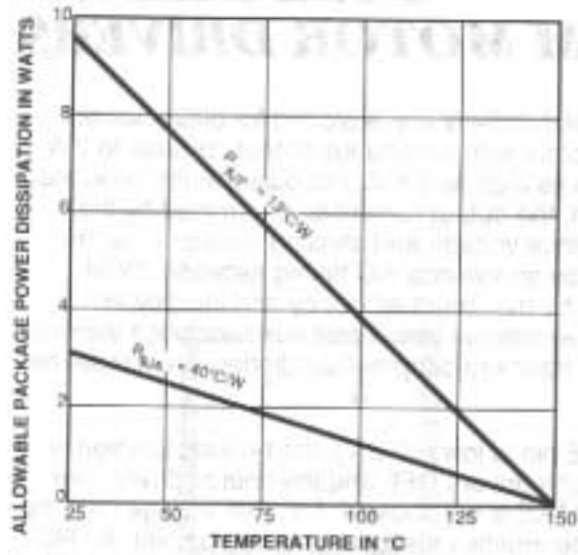


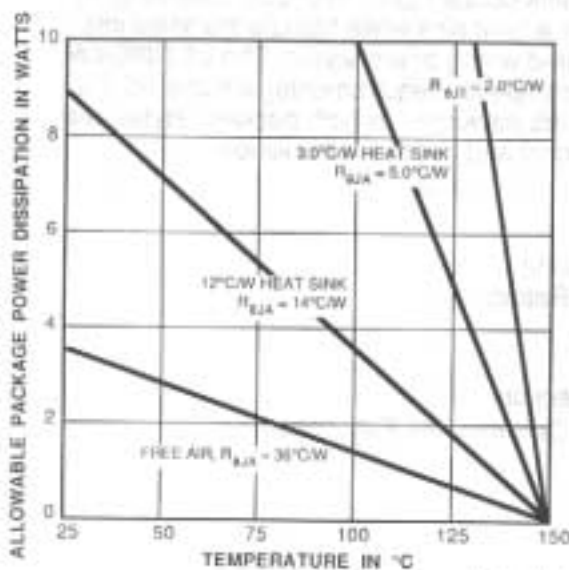
2953 AND 2954 FULL-BRIDGE PWM MOTOR DRIVERS

UDN2953B



Dwg. GP-004-1

UDN2954W



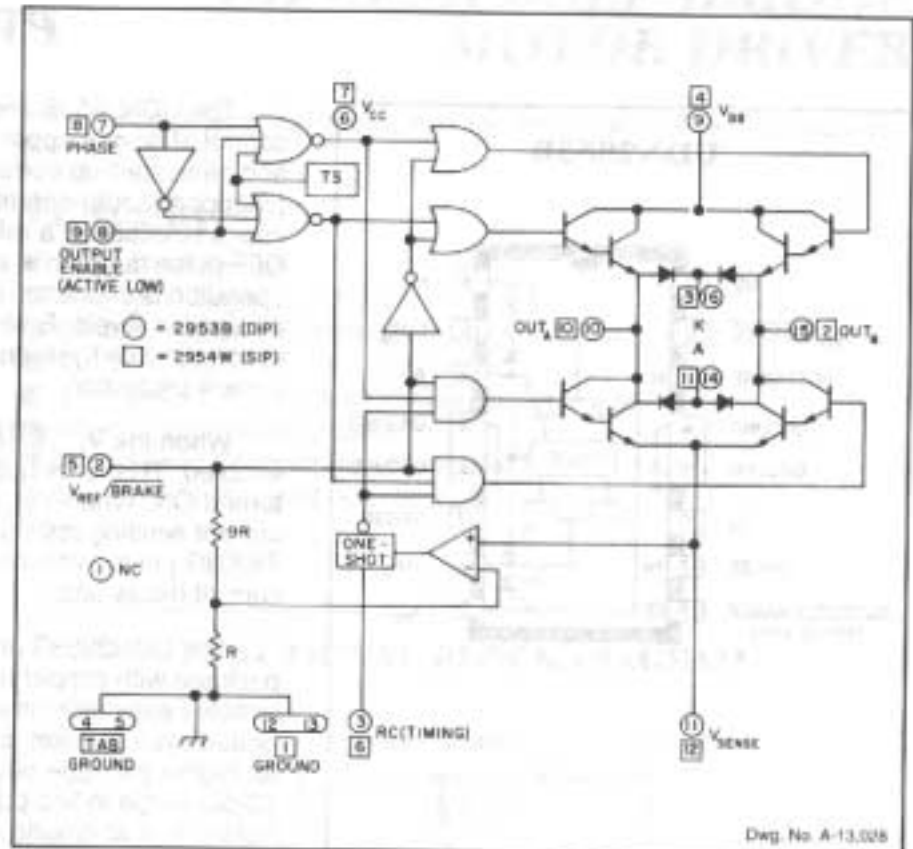
Dwg. GP-010A

TRUTH TABLE

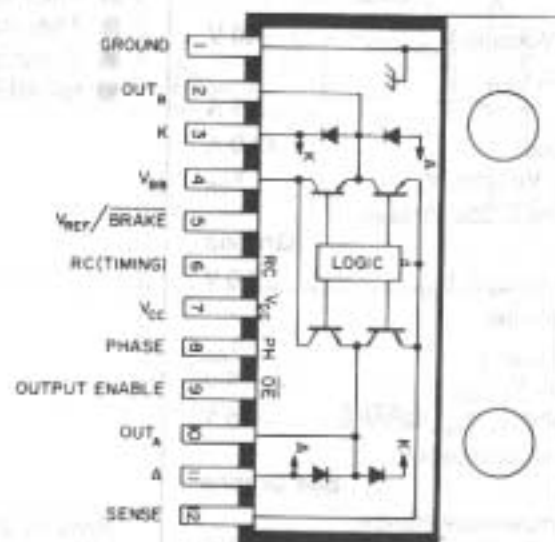
Output Enable	Phase	$V_{REF}/BRAKE$	Out _A	Out _B
Low	High	> 2.4 V	High	Low
Low	Low	> 2.4 V	Low	High
High	X	> 2.4 V	Open	Open
X	X	< 0.8 V	High	High

X = Irrelevant

FUNCTIONAL BLOCK DIAGRAM



UDN2954W



Dwg. No. A-13,023

2953 AND 2954

FULL-BRIDGE PWM MOTOR DRIVERS

ELECTRICAL CHARACTERISTICS at $T_A = +25^\circ\text{C}$, $T_J \leq +150^\circ\text{C}$, $V_{BB} = 50\text{ V}$, $V_{CC} = 5\text{ V}$,
 $V_{SENSE} = 0\text{ V}$, $R_C = 20\text{ k}\Omega/470\text{ pF}$ to Ground.

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Drivers (OUT _A or OUT _B)						
Output Supply Range	V _{BB}		6.5	—	50	V
Output Leakage Current	I _{CEX}	V _{ENABLE} = 5 V, V _{OUT} = V _{BB} , (note)	—	—	50	μA
		V _{ENABLE} = 5 V, V _{OUT} = 0 V, (note)	—	—	-50	μA
Output Sustaining Voltage	V _{CE(sus)}	I _{OUT} = ±2 A, L = 2 mH	50	—	—	V
Output Saturation Voltage	V _{CE(SAT)}	V _{ENABLE} = 0 V, I _{OUT} = ±0.5 A	—	1.0	1.2	V
		V _{ENABLE} = 0 V, I _{OUT} = ±1.0 A	—	1.2	1.4	V
		V _{ENABLE} = 0 V, I _{OUT} = ±2.0 A	—	1.5	1.8	V
Clamp Diode Leakage Current	I _R	V _R = 50 V	—	—	50	μA
Clamp Diode Forward Voltage	V _F	I _F = 2 A	—	1.8	2.2	V
Motor Supply Current	I _{BB(ON)}	V _{ENABLE} = 0.8 V, V _{REF} = 2.4 V, No Load	—	20	30	mA
	I _{BB(OFF)}	V _{ENABLE} = V _{REF} = 2.4 V, No Load	—	2.5	3.5	mA
		V _{ENABLE} = 5 V, V _{REF} = 0.8 V, No Load	—	40	60	mA

Control Logic

Logic Supply Range	V_{CC}		4.5	5.0	5.5	V
Logic Input Current	$I_{IN(1)}$	All Inputs = 2.4 V	—	<-1.0	-10	μA
	$I_{IN(2)}$	All Inputs = 0.8 V	—	-50	-200	μA
Logic Input Voltage	$V_{IN(1)}$	All Inputs	2.4	—	—	V
	$V_{IN(2)}$	All Inputs	—	—	0.8	V
V_{REF} Open-Circuit Voltage	$V_{REF(OPEN)}$	$I_{REF} = 0$	—	$V_{CC}/2$	—	V
Current Limit Threshold		V_{REF}/V_{SENSE} at Trip Point	9.5	10	10.5	—
Turn-On Delay	t_{on}	All Drivers	—	1.0	—	μs
Turn-Off Delay	t_{off}	All Drivers	—	1.0	—	μs
Thermal Shutdown Temp.	T_J		—	165	—	$^\circ\text{C}$
Logic Supply Current	I_{CC}	$V_{ENABLE} = V_{REF} = 2.4\text{ V}$	—	15	20	mA
		$V_{ENABLE} = 0.8\text{ V}$, $V_{REF} = 2.4\text{ V}$	—	22	30	mA

NOTE: Tests performed at OUT_B with $V_{PHASE} = 0.8\text{ V}$ and at OUT_A with $V_{PHASE} = 2.4\text{ V}$