

Dual 16 bit, 88 kHz, Multiplexed D/A

Evaluation Board Available — CX20152PCB

Description

CX20152 is a 16-bit D/A converter IC for PCM audio. It uses an integration system consisting of the following circuits.

- Clock signal generator
- TTL-ECL interface circuit
- Discharge drive circuit
- Analog switch drive circuit
- 1/4 frequency divider output circuit

By adding an integrator, analog switch and low pass filter externally to the IC, analog signal is reproduced from the 16-bit digital data.

Features

- Conversion frequency 88.2kHz
- Serial data input
- Low distortion factor 0.003% (typ.)

Structure

Bopolar Sillicon Monolithic IC

Absolute Maximum Rating

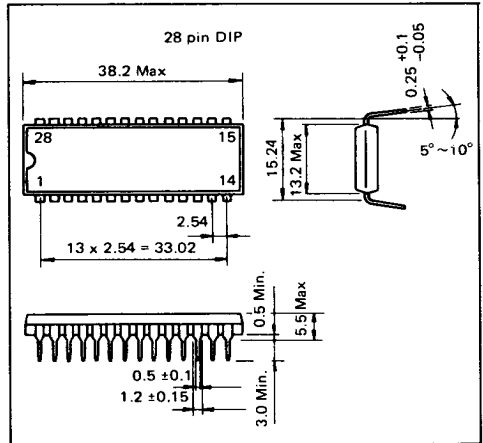
● Supply voltage	VCC to VEE	12	V
● Operating temperature	Topr	-20 to +75	°C
● Storage temperature	Tstg	-55 to +150	°C
● Allowable power dissipation	PD	2.1	W

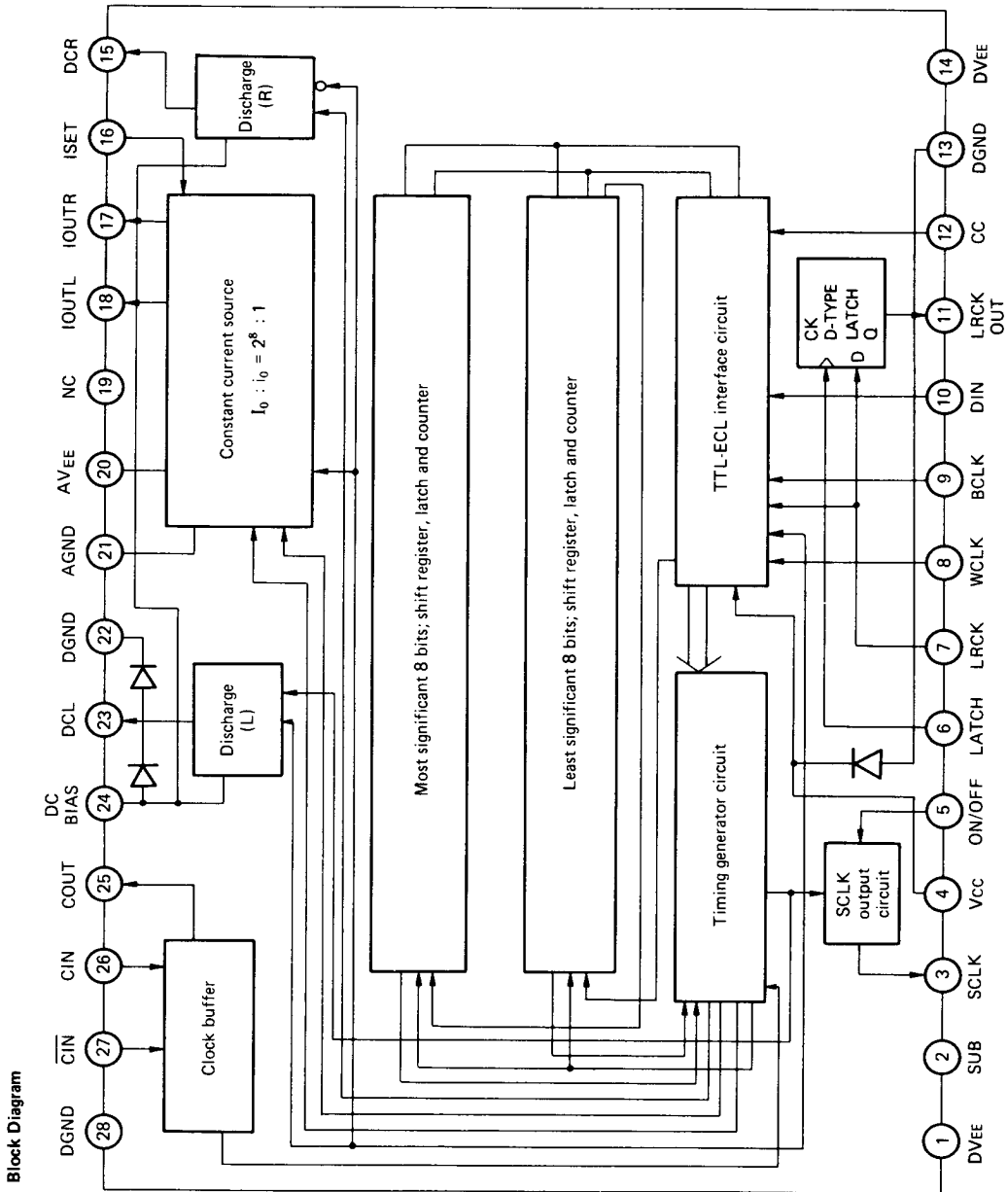
Recommended Operating Conditions

● Supply voltage	VCC	5 ±0.25	V
	VEE	-5 ±0.25	V

Package Outline

Unit: mm





Pin Description

No.	Symbol	Description
1	DVEE	Digital VEE: -5V
2	SUB	IC substrate: Be sure to connect to Pin 1.
3	SCLK	System clock output pin
4	Vcc	Digital Vcc: +5V
5	ON/OFF	Pin to determine the system clock on/off
6	LATCH	Clock pin of D type latch
7	LRCK	LRCK input pin
8	WCLK	WCLK input pin
9	BCLK	BCLK input pin
10	DIN	DIN (data input pin): MSB first
11	LRCK OUT	LRCK output pin
12	CC	CC input pin
13	DGND	Digital ground
14	DVEE	Digital VEE: -5V
15	DCR	Right channel discharge drive signal output pin
16	ISET	Integration current setting pin
17	IOUTR	Right channel current output pin
18	IOUTL	Left channel current output pin
19	NC	No connection
20	AVEE	Analog VEE
21	AGND	Analog GND
22	DGND	Digital GND
23	DCL	Left channel discharge drive signal output pin
24	DC BIAS	Discharge circuit bias pin
25	COUT	Clock generator output pin
26	CIN	Clock generator positive input pin
27	CIN	Clock generator negative input pin
28	DGND	Digital GND

CX20152 Input/Output Pin Equivalent Circuits

No.	Symbol	Equivalent Circuits
1	DVEE	
2	SUB	
3	SCLK	
4	Vcc	
5	ON/OFF	
6	LATCH	
7	LRCK	

No.	Symbol	Equivalent Circuit
8	WCLK	
9	BCLK	
10	DIN	
12	CC	
11	LRCK OUT	
13	DGND	
14	DVEE	
15	DCR	
23	DCL	
24	DC BIAS	

No.	Symbol	Equivalent Circuits
22	DGND	
16	ISET	
17	IOUTR	
18	IOUTL	
19	NC	
20	AVEE	
21	AGND	
25	COUT	
26	CIN	
27	$\overline{\text{CIN}}$	
28	DGND	

Electrical Characteristics

(Ta = 25°C, V_{EE} = -5.0V, V_{CC} = 5.0V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Circuit current	IEE	1, 2, 14, 20	Pins 4, 5 = 5V	-125	-95		mA
Circuit current	ICC1	4	Pin 5 = 5V (6, 7, 8, 9, 10, 12, GND)		12.6	15.5	mA
Circuit current	ICC2	4	Pin 5 = 0V (6, 7, 8, 9, 10, 12, GND)		5.9	10.0	mA
Input threshold voltage	V _{TH}	6, 7, 8, 9, 10, 12			2.1		V
High level input voltage	V _{IH}	6, 7, 8, 9, 10, 12		2.9			V
Low level input voltage	V _{IL}	6, 7, 8, 9, 10, 12				0.9	V
High level input current 1	I _{IH1}	5	V _{IH} = 5V		0.7	1.3	mA
High level input current 2	I _{IH2}	6, 7, 8, 9, 10, 12	V _{IH} = 5V		250	550	μA
Low level input current 1	I _{IL1}	5	V _{IL} = 0V		0.35	0.8	mA
Low level input current 2	I _{IL2}	6, 7, 8, 9, 10, 12	V _{IL} = 0V		120	550	μA
High level output voltage	V _{LROCKH}	11	With Pin 7 at 4.5V, set I _{OH} = -100μA and input a clock of 0V-5V-0V to Pin 6.	2.7	4.2		V
Low level output voltage	V _{LROCKL}	11	With Pin 7 at 0V, set I _{OL} = 100μA and input a clock of 0V-5V-0V to Pin 6.		-3.1	-2.7	V
SCLK output, high level	V _{SCLKH}	3	I _{OH} = -10μA	3.4	4.2		V
SCLK output, low level	V _{SCLKL}	3	I _{OL} = 400μA		0.5	1.6	V
Discharge circuit power dissipation current	I _{DCBIAS}	24	V _{DCBIAS} = 0V		1.9	2.5	mA
Discharge circuit high level output voltage	V _{DCH}	15, 23	Pin 24 voltage = 1.3V Load current = 1.2mA	0	0.4	0.65	V
Discharge circuit low level output voltage	V _{DCL}	15, 23	Pin 24 voltage = 1.3V Load current = 1.2mA		-4.2	-3.4	V
I _{SET} current	I _{SET}	16			0.5	1.0	mA
I _{OUT} output current	I _{OUT}	17, 18	Pins 17, 18: Voltage = 0V Pin 16: I _{SET} = 500μA (I _{OUT} = I _O + I _{IO})		2.008		mA
Clock input bias voltage	V _{CIN}	26, 27			-1.3		V
Clock high level output voltage	V _{COH}	25			-0.8		V
Clock low level output voltage	V _{COL}	25			-1.6		V
Current output pin leakage	I _O LEAK	17, 18	Pins 17, 18: Voltage = 0V when the current output is off.			1.5	μA
Current ratio	I _O /I _{IO}	17, 18	Pin 16: I _{SET} = 500μA	255.0	256.0	257.5	—
Distortion factor	THD1	Both right and left;	0dB (full scale) when reproduced.		0.003	0.005	%
	THD2	Both right and left;	-20dB when reproduced.		0.02	0.025	%
Operation clock frequency	f _{CLK1}	Both self-drive & external-drive	Ta = -20 ~ +70°C		68	80	MHz
Operation clock frequency	f _{CLK2}	Both self-drive & external-drive	Ta = -20 ~ +75°C		68	75	MHz

Description of Conversion Operation

(1) Data pickup (BCLK, DIN, WCLK, LRCK)

Data consist of 16-bit serial signals in 2's complement. They are transmitted into the IC sequentially from the MSB in synchronization with the rise edge of the bit clock (BCLK). (The BCLK delay will change the data. The falling edge changes the data.)

When the word clock (WCLK) is changed from high level to low level at the 17th BCLK, the 16-bit data is transferred from the shift register to the latch with the decay signal. When CX20152 is used in the stereo mode, other-channel data are transmitted from the 17th BCLK.

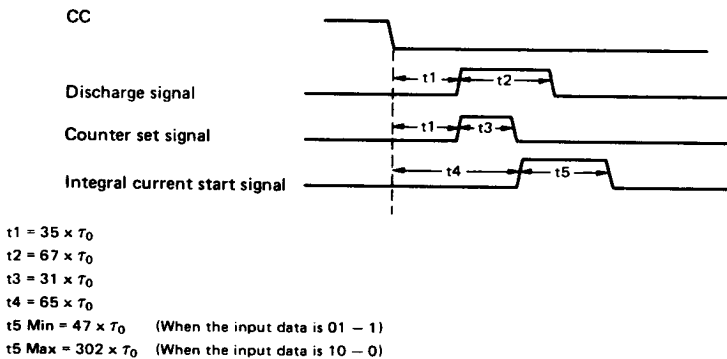
In the stereo mode, the Rch data is picked up when LRCK is at a low level and the Lch data is picked up when LRCK is at a high level. IOUTL and DCL operate only when LRCK is at a low level, and IOUTR and DCR operate only when LRCK is at a high level.

(2) Conversion operation (CC, LRCK, CIN, IOUTL, IOUTR, DCL, DCR)

When more than 3 clocks are fed from the clock input (CIN) with the conversion command (CC) at a high level, all the internal timing circuits are reset.

After the resetting, the internal timing circuit starts operation when a clock is input from CIN with CC at a low level.

From this operation, three signals, Discharge, Counter set and Integral current Start, are generated. Timing of these signals is determined as follows by the clock interval τ_0 and its quantity.



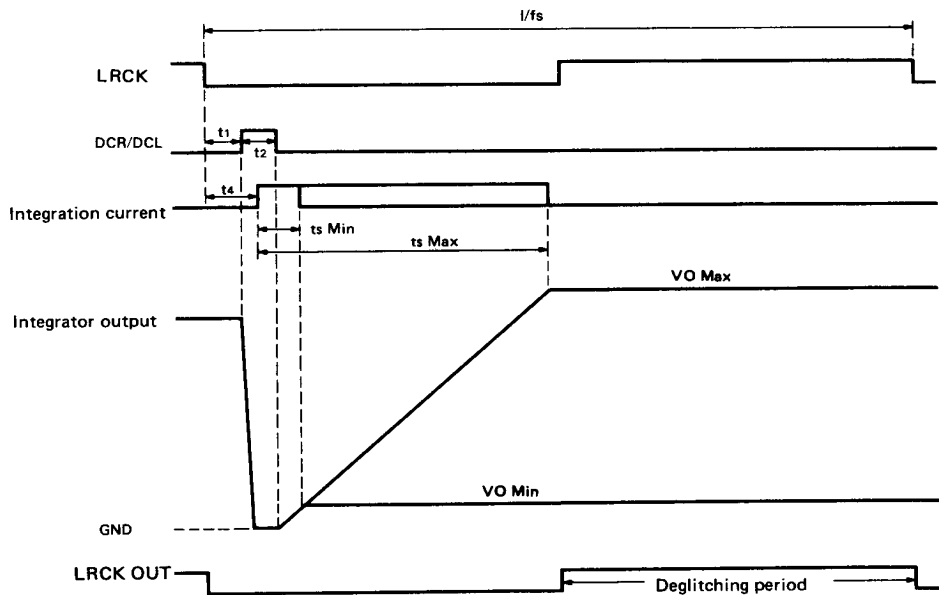
The counter set signal is used to set the data input in the latch to the counter but does not output externally.

The discharge signal is output from DCL and DCR and controlled by LRCK. It is output from DCL when LRCK is at a low level and from DCR when LRCK is at a high level.

The integral current start signal starts the upper current I_{o1} and lower current I_{o2} flowing. The counter starts counting from the preset value simultaneously when the discharge signal is off, counts 11 offsets after the end of the counting and outputs a signal to stop the integration current. The value t_5 is varied between 0 to 255 by the input data value preset to the counter.

Therefore, the time before the end of the integration after the low level has been set, i.e. the conversion time, requires the maximum ($t_4 + t_5 \text{ Max} = 367 \times \tau_0$) seconds.

The integration current of IOUTL is output, as with the discharge signal, when LRCK is at a low level; IOUTR is output when LRCK is at a high level.

(3) The relation between sampling frequency f_s and clock

The maximum and minimum values of the integration voltage output, VO_{Max} and VO_{Min} , are expressed as follows.

$$VO_{Max} = \frac{i_0}{C} \cdot \tau_c \cdot 267 + \frac{i_0}{C} \cdot \tau_c \cdot 266 \quad (t_4 + t_{s \text{ Max}})$$

$$VO_{Min} = \frac{i_0}{C} \cdot \tau_c \cdot 12 + \frac{i_0}{C} \cdot \tau_c \cdot 11 \quad (t_4 + t_{s \text{ Min}})$$

where f_{CLK} is a clock frequency and τ is a period.

The integration voltage is held by the capacitor C in the integrator when the current is switched off. This voltage is used as D/A conversion output during the deglitching period T which is given according to the settling time of the deglitching circuit.

The relation between the conversion frequency f_s and the clock frequency f_{CLK} is given as below assuming that the conversion time and deglitching period are equivalent:

$$f_s = \frac{f_{CLK}}{2 \times (t_4 + t_{s \text{ Max}})} = \frac{f_{CLK}}{734}$$

where $f_s = 44.1 \text{ kHz}$ results in 32.4 MHz of f_{CLK}

It is, however, recommendable to specify f_s as the follow for the practical use because a settling time of 0.5 to 1.0 μ s is required for the integrator after the current for t_s disappears:

$$f_s = \frac{f_{CLK}}{2(t_4 + t_{s \text{ Max}} + 1.0(\mu\text{s})) + T}$$

(4) Integration current setting (ISET, IOU_{TL}, IOU_{TR})

Integration current is determined by a constant current value input through the ISET pin, which is given as below:

$$\text{IOU}_{TL} (R) = I_0 + i_0 = \left(4 + \frac{1}{64}\right) \text{ISET}$$

where i_0 and I_0 are integration currents corresponded to the 1LSB and $2^8 \cdot \text{LSB}$, respectively.

If D_0 and D_{15} are specified as MSB and LSB, respectively, integrator output voltage V_0 is given by the following equation:

$$V_0 = \frac{I_0}{C} (D_0 \cdot 2^7 + \overline{D}_1 \cdot 2^7 + \dots + \overline{D}_7 \cdot 2^0 + 12) \tau_0 \\ + \frac{i_0}{C} (\overline{D}_8 \cdot 2^7 + \overline{D}_9 \cdot 2^6 + \dots + \overline{D}_{15} \cdot 2^0 + 11) \tau_0$$

where $\text{ISET} = 500 \mu\text{A}$, $\tau = \frac{1}{35 \text{ (MHz)}} = 28.6 \text{ (ns)}$ and $C=2000 \text{ pF}$ result in the maximum output voltage $V_{0 \text{ Max}}$ of the integrator when any of a value from 10 to 0 is given as an input data. Based on the relations below,

$$I_0 = 4 \cdot \text{ISET}$$

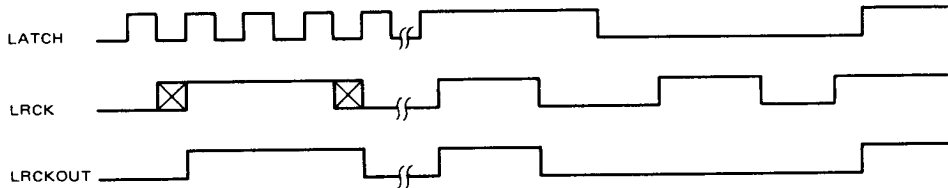
$$i_0 = \frac{1}{64} \cdot \text{ISET}$$

$V_{0 \text{ Max}}$ is calculated as the follow:

$$V_{0 \text{ Max}} = \frac{2.0 \times 10^{-3}}{2000 \times 10^{-12}} \cdot 267 \cdot 28.6 \times 10^{-9} \\ + \frac{400 \cdot 10^{-6} / 64}{2000 \times 10^{-12}} \cdot 266 \cdot 28.6 \times 10^{-9} \\ = 7.67 \text{ (V)}$$

(5) LRCK OUT operation (LATCH, LRCK, LRCK OUT)

The LRCK OUT is a drive output for the analog switch IC (equivalent to MC14053B) to clip the output converted by CX20152 and the integrator so that the converted output can be a PAM wave. If the PAM wave has a jitter, a conversion error results. To absorb this jitter, a D-type latch is built-in and the LATCH input is used as its clock. The D-type latch sets the output state in synchronization with the rise of the clock (LATCH) and the logic high.



Timing of LATCH, LRCK and LRCKOUT

In the high-speed conversion (with sampling frequency of 88.2kHz), the clock frequency is as high as about 70MHz. This will affect the delay time of the analog switch IC. The delay time possibly becomes equal to t_1 . Then, the last part of the PAM wave overlaps on the discharge time for CX20152 causing a considerable conversion error. In such a case, LRCK level can be fed through by keeping LATCH at a high level.

(6) Clock input/output Pin (COUT, CIN and $\overline{\text{CIN}}$)

The clock buffer consists of a circuit equivalent to a general-purpose ECL logic circuit, with its input pin biased with an internal bias circuit ($\approx -1.3\text{V}$). The output amplitude level is 0.8V.

(7) Bias Pin (DVEE, SUB, DGND, VCC, AVEE, AGND and DC BIAS)

SUB denotes the IC substrate and its voltage potential should be common to that of DVEE. The standard value of DVEE and AVEE is -5.0V .

VCC is the power supply for the interface circuit from a CMOS or TTL level to the internal ECL logic. Its standard value is $+5\text{V}$.

DC BIAS is the bias circuit of the discharge signal output circuit. As it requires about 2.5mA as its standard current, supply current should be $2.5\text{mA} + \alpha$. This pin voltage is biased to $2V_f$ and the value of α is determined as follows.

To maintain the pin voltage at $2V_f$ ($\approx 1.4\text{V}$), about 0.5mA of current is required. Additionally, the maximum current flowing through the load resistor R_L attached to DCR (Pin 15) and DCL (Pin 23) is obtained from the following equation.

$$1/R_L \times (V_{DCH} + |DVEE|) \times 2, \text{ where } R_L = 4.7\text{k}\Omega, V_{DCH} = 0.4\text{V} \text{ and } DVEE = -5\text{V}$$

Hence, $\alpha = 0.5 + 1.15 = 1.65$ (mA)

Therefore, the total current will be 4.32mA .

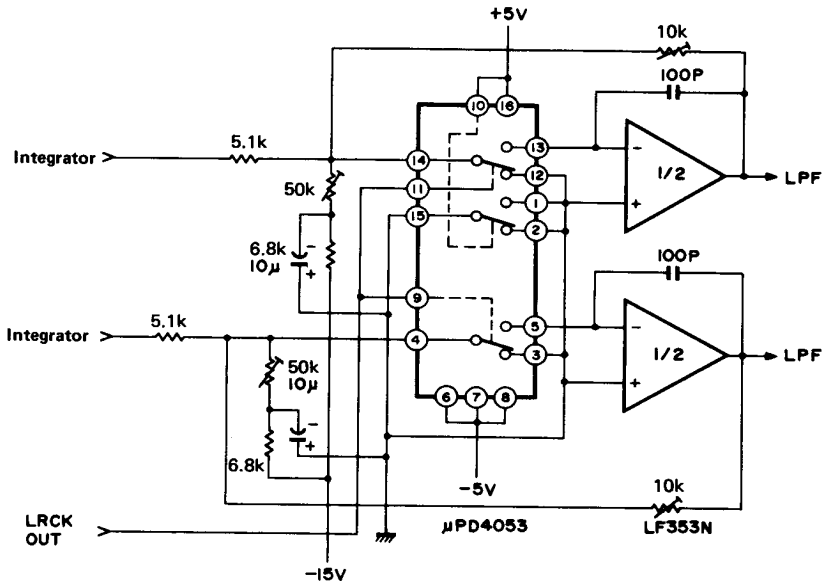
We recommend 5mA with R_L at $4.7\text{k}\Omega$.

(8) System clock output pin, ON/OFF (SCKL, ON/OFF)

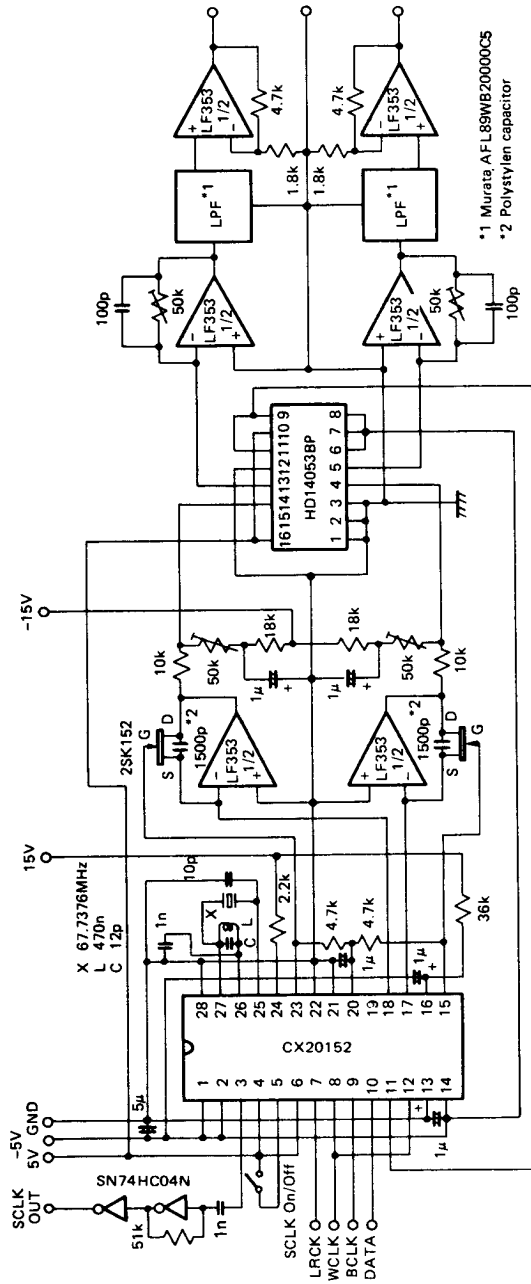
SCKL is the output pin of the $1/4$ frequency divider of the oscillation circuit's master clock frequency. The frequency outputs when the ON/OFF pin is supplied with 5V (V_{CC}) and stops when the ON/OFF pin is supplied with 0V or set to open.

As its output amplitude is 2V and too low to be connected directly to a TTL or CMOS, be sure to amplify before connection.

Application Circuit for Operating Deglitcher in Sample/Hold Type

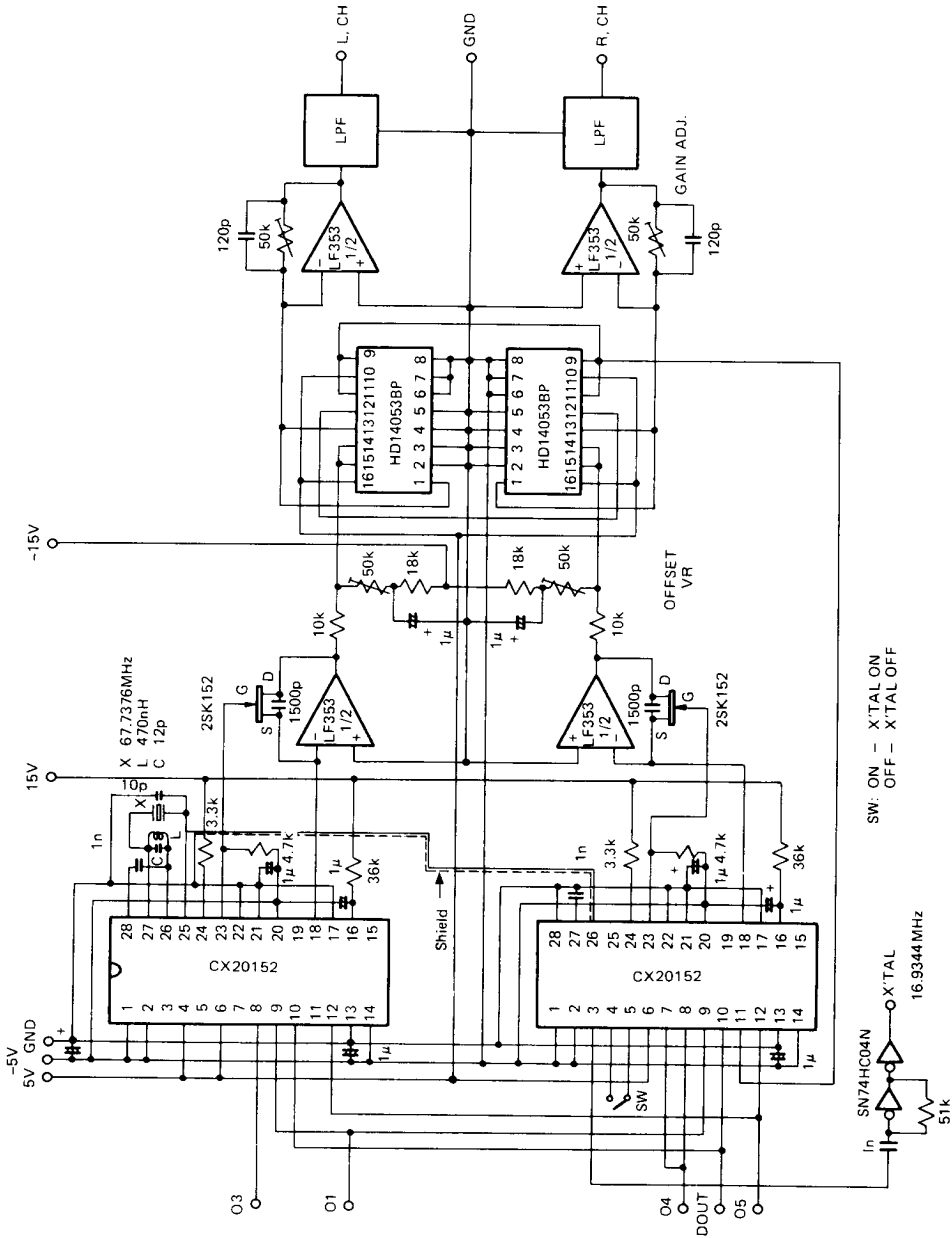


Application Circuit (Example 1)

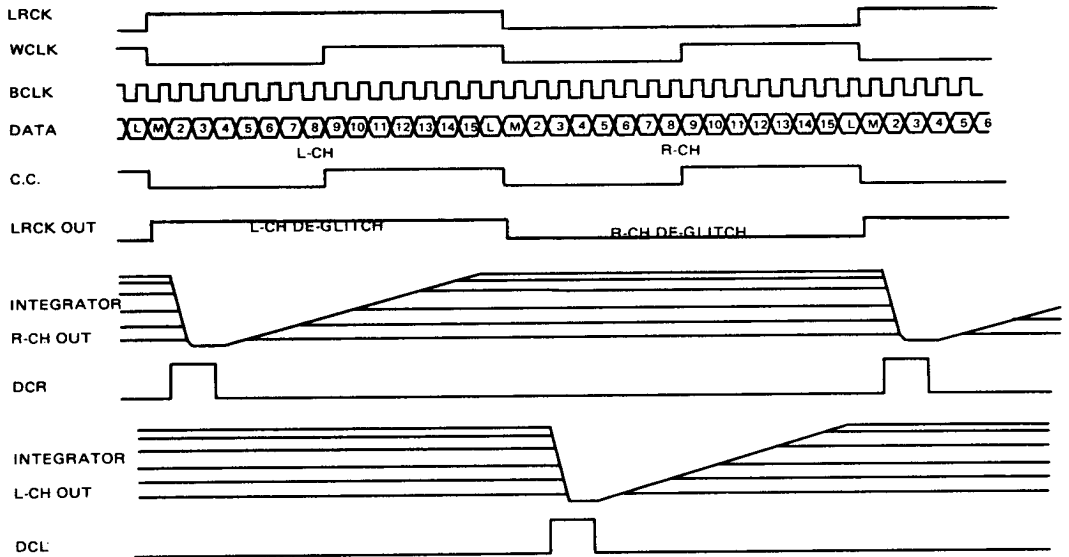


*1 Murata AFL89WB2000CS
*2 Polystylen capacitor

Application Circuit (Example 2)

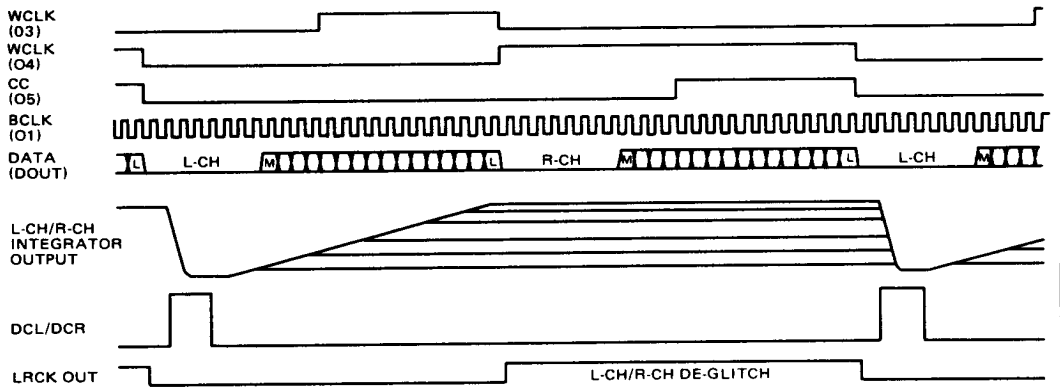


Timing Chart



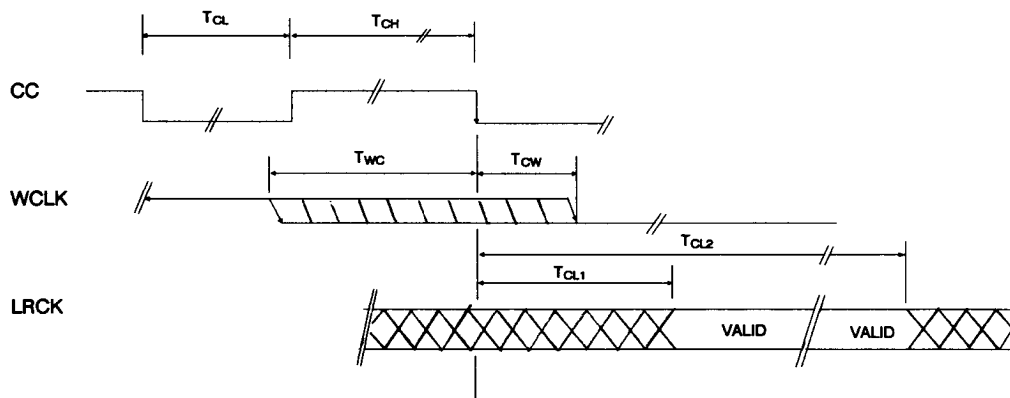
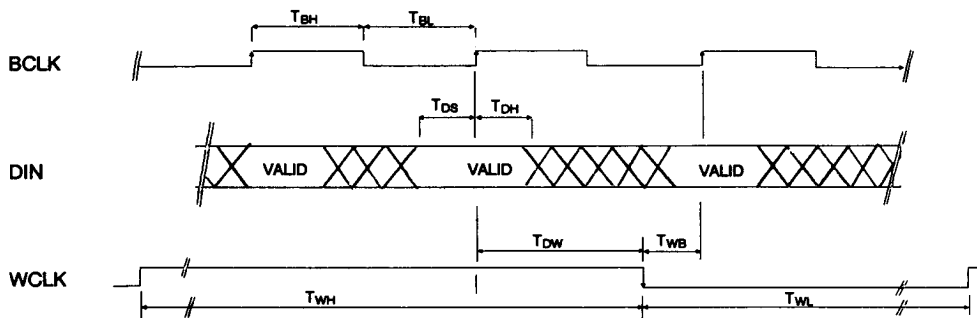
(See Application Circuit Ex. 1)







Timing Chart II



(See Application Circuit Ex. 2)

Detailed Timing Chart



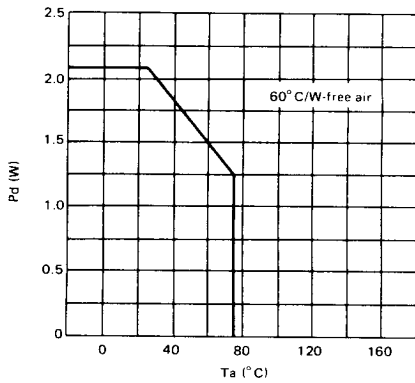
T _{BH}	BCLK "H" Pulse width	min = 100ns
T _{BL}	BCLK "L" Pulse width	min = 100ns
T _{DS}	DIN Set-up time	min = 50ns
T _{DH}	DIN Hold Time	min = 50ns
T _{DW}	from DIN  to WCLK	min = 150ns
T _{WB}	from WCLK  to BCLK	min = 50ns
T _{WH}	WCLK "H" Pulse Width	min = 100ns
T _{WL}	WCLK "L" Pulse Width	min = 100ns
T _{CH}	CC "H" Pulse width	min = 4 × τ _M
T _{CL}	CC "L" Pulse width	min = 102 × τ _M
T _{WC}	from WCLK  to CC	max = T _{CL} + T _{CH} - 70 × τ _M
T _{CW}	from CC  to WCLK	max = 30 × τ _M
T _{CL1}	from CC  to LRCK "Invalid → Valid"	max = 34 × τ _M - τ _A - τ _B /2
T _{CL2}	from CC  to LRCK "Valid → Invalid"	min = 367 × τ _M

$$\tau_M = 1/f_{MCLK}$$

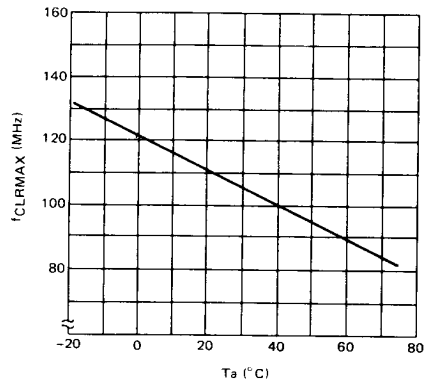
τ_A = Delay time produced by external analog switch

$$\tau_B = 1/f_{BCLK}$$

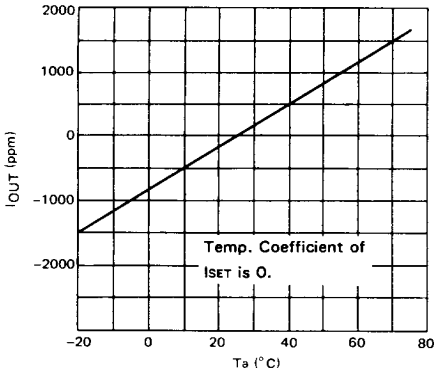
**Maximum allowable power dissipation
decrement curve**



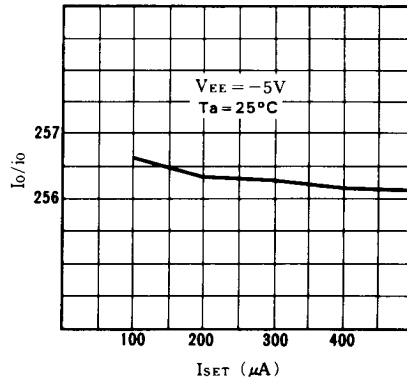
**Maximum clock frequency temperature
characteristics**



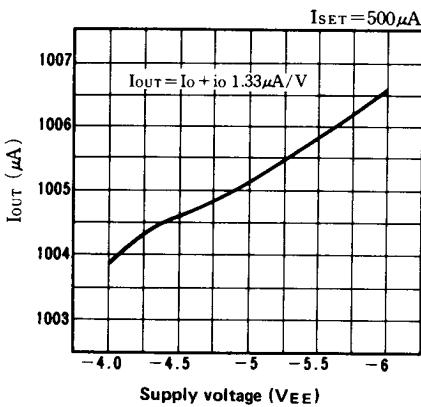
**Iout temperature characteristics (Io + io)
(Both of R, Lch)**



Io/io vs. ISET



Output current vs. Supply voltage (VEE)



Distortion factor

