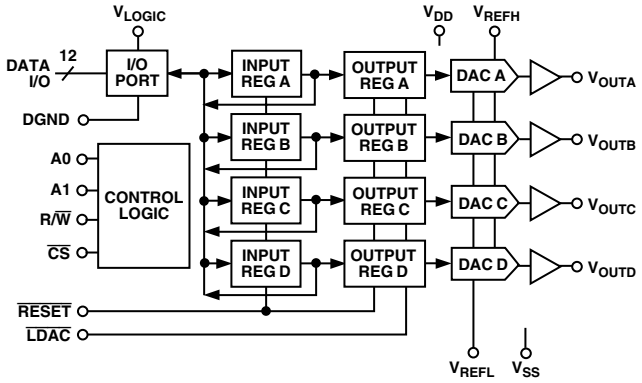
Quad, 12-Bit DAC Voltage Output with Readback

DAC8412/DAC8413

FEATURES
+5 V to ±15 V Operation
Unipolar or Bipolar Operation
True Voltage Output
Double-Buffered Inputs
Reset to Min (DAC8413) or Center Scale (DAC8412)
Fast Bus Access Time
Readback

APPLICATIONS
Automatic Test Equipment
Digitally Controlled Calibration
Servo Controls
Process Control Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAC8412 and DAC8413 are quad, 12-bit voltage output DACs with readback capability. Built using a complementary BiCMOS process, these monolithic DACs offer the user very high package density.

Output voltage swing is set by the two reference inputs V_{REFH} and V_{REFL}. By setting the V_{REFL} input to 0 V and V_{REFH} to a positive voltage, the DAC will provide a unipolar positive output range. A similar configuration with V_{REFH} at 0 V and V_{REFL} at a negative voltage will provide a unipolar negative output range. Bipolar outputs are configured by connecting both V_{REFH} and V_{REFL} to nonzero voltages. This method of setting output voltage range has advantages over other bipolar offsetting methods because it is not dependent on internal and external resistors with different temperature coefficients.

Digital controls allow the user to load or read back data from any DAC, load any DAC and transfer data to all DACs at one time.

An active low $\overline{\text{RESET}}$ loads all DAC output registers to mid-scale for the DAC8412 and zero scale for the DAC8413.

The DAC8412/DAC8413 are available in 28-lead plastic DIP, PLCC and LCC packages. They can be operated from a wide variety of supply and reference voltages with supplies ranging from single +5 V to ±15 V, and references from +2.5 V to ±10 V. Power dissipation is less than 330 mW with ±15 V supplies and only 60 mW with a +5 V supply.

For MIL-STD-883 applications, contact your local ADI sales office for the DAC8412/DAC8413/883 data sheet which specifies operation over the –55°C to +125°C temperature range. All 883 parts are also available on Standard Military Drawings 5962-91 76401MXA through 76404M3A.

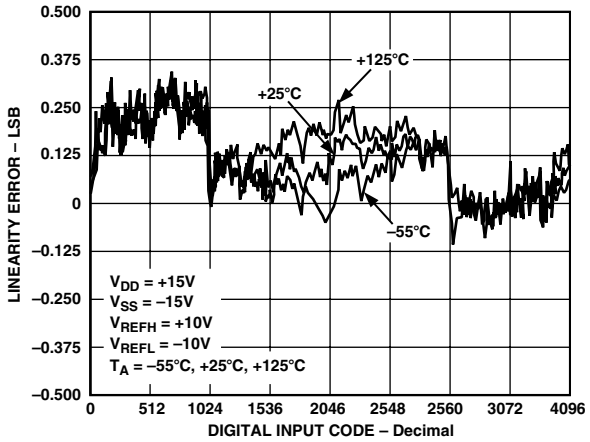


Figure 1. INL vs. Code Over Temperature

REV. D

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DAC8412/DAC8413–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($@ V_{DD} = +15.0$ V, $V_{SS} = -15.0$ V, $V_{LOGIC} = +5.0$ V, $V_{REFH} = +10.0$ V, $V_{REFL} = -10.0$ V, $-40°C \le T_A \le +85°C$ unless otherwise noted. See Note 1 for supply variations.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Integral Nonlinearity Error	INL	E Grade		0.25	±0.5	LSB
	INL	F Grade			±1	LSB
Differential Nonlinearity Error	DNL	Monotonic Over Temperature	–1			LSB
Min-Scale Error	V_{ZSE}	R_L = 2 kΩ			±2	LSB
Full-Scale Error	V_{FSE}	R_L = 2 kΩ			±2	LSB
Min-Scale Tempco	TCV_{ZSE}	R_L = 2 kΩ		15		ppm/°C
Full-Scale Tempco	TCV_{FSE}	R_L = 2 kΩ		20		ppm/°C
Linearity Matching		Adjacent DAC Matching		±1		LSB
REFERENCE						
Positive Reference Input Voltage Range		Note 2	V_{REFL} + 2.5		V_{DD} – 2.5	V
Negative Reference Input Voltage Range		Note 2	–10		V_{REFH} – 2.5	V
Reference High Input Current	I_{REFH}		–2.75	+1.5	+2.75	mA
Reference Low Input Current	I_{REFL}		0	+2	+2.75	mA
Large Signal Bandwidth	BW	–3 dB, V_{REFH} = 0 V to +10 V p-p		160		kHz
AMPLIFIER CHARACTERISTICS						
Output Current	I_{OUT}	R_L = 2 kΩ, C_L = 100 pF	–5		+5	mA
Settling Time	t_S	to 0.01%, 10 V Step, R_L = 1 kΩ		10		µs
Slew Rate	SR	10% to 90%		2.2		V/µs
Analog Crosstalk				72		dB
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}	T_A = +25°C	2.4			V
Logic Input Low Voltage	V_{INL}	T_A = +25°C			0.8	V
Logic Output High Voltage	V_{OH}	I_{OH} = +0.4 mA	2.4			V
Logic Output Low Voltage	V_{OL}	I_{OL} = –1.6 mA			0.4	V
Logic Input Current	I_{IN}				1	µA
Input Capacitance	C_{IN}			8		pF
Digital Feedthrough[3]		V_{REFH} = +2.5 V, V_{REFL} = 0 V		5		nV-s
LOGIC TIMING CHARACTERISTICS[3]		Note 4				
Chip Select Write Pulsewidth	t_{WCS}		80			ns
Write Setup	t_{WS}	t_{WCS} = 80 ns	0			ns
Write Hold	t_{WH}	t_{WCS} = 80 ns	0			ns
Address Setup	t_{AS}		0			ns
Address Hold	t_{AH}		0			ns
Load Setup	t_{LS}		70			ns
Load Hold	t_{LH}		30			ns
Write Data Setup	t_{WDS}	t_{WCS} = 80 ns	20			ns
Write Data Hold	t_{WDH}	t_{WCS} = 80 ns	0			ns
Load Data Pulsewidth	t_{LDW}		170			ns
Reset Pulsewidth	t_{RESET}		140			ns
Chip Select Read Pulsewidth	t_{RCS}		130			ns
Read Data Hold	t_{RDH}	t_{RCS} = 130 ns	0			ns
Read Data Setup	t_{RDS}	t_{RCS} = 130 ns	0			ns
Data to Hi Z	t_{DZ}	C_L = 10 pF			200	ns
Chip Select to Data	t_{CSD}	C_L = 100 pF			160	ns
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSS	14.25 V ≤ V_{DD} ≤ 15.75 V			150	ppm/V
Positive Supply Current	I_{DD}	V_{REFH} = +2.5 V		8.5	12	mA
Negative Supply Current	I_{SS}		–10	–6.5		mA
Power Dissipation	P_{DISS}				330	mW

NOTES

[1]All supplies can be varied ±5%, and operation is guaranteed. Device is tested with nominal supplies.

[2]Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.

[3]All parameters are guaranteed by design.

[4]All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS

(@ $V_{DD} = V_{LOGIC} = +5.0$ V ± 5%, $V_{SS} = 0.0$ V, $V_{REFH} = +2.5$ V, $V_{REFL} = 0.0$ V, and $V_{SS} = -5.0$ V ± 5%, $V_{REFL} = -2.5$ V, $-40°C \le T_A \le +85°C$ unless otherwise noted. See Note 1 for supply variations.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Integral Nonlinearity Error	INL	E Grade		1/2	±1	LSB
	INL	F Grade			±2	LSB
	INL	V_{SS} = 0.0 V; E Grade[2]			±2	LSB
	INL	V_{SS} = 0.0 V; F Grade[2]			±4	LSB
Differential Nonlinearity Error	DNL	Monotonic Over Temperature	–1			LSB
Min-Scale Error	V_{ZSE}	V_{SS} = –5.0 V			±4	LSB
Full-Scale Error	V_{FSE}	V_{SS} = –5.0 V			±4	LSB
Min-Scale Error	V_{ZSE}	V_{SS} = 0.0 V			±8	LSB
Full-Scale Error	V_{FSE}	V_{SS} = 0.0 V			±8	LSB
Min-Scale Tempco	TCV_{ZSE}			100		ppm/°C
Full-Scale Tempco	TCV_{FSE}			100		ppm/°C
Linearity Matching		Adjacent DAC Matching		±1		LSB
REFERENCE						
Positive Reference Input Voltage Range		Note 3	V_{REFL} + 2.5		V_{DD} – 2.5	V
Negative Reference Input Voltage Range		V_{SS} = 0.0 V	0		V_{REFH} – 2.5	V
		V_{SS} = –5.0 V	–2.5		V_{REFH} – 2.5	V
Reference High Input Current	I_{REFH}	Code 000H	–1.0		+1.0	mA
Large Signal Bandwidth	BW	–3 dB, V_{REFH} = 0 V to 2.5 V p-p		450		kHz
AMPLIFIER CHARACTERISTICS						
Output Current	I_{OUT}	R_L = 2 kΩ, C_L = 100 pF	–1.25		+1.25	mA
Settling Time	t_S	to 0.01%, 2.5 V Step, R_L = 1 kΩ		7		µs
Slew Rate	SR	10% to 90%		2.2		V/µs
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}	T_A = +25°C	2.4			V
Logic Input Low Voltage	V_{INL}	T_A = +25°C			0.8	V
Logic Output High Voltage	V_{OH}	I_{OH} = +0.4 mA	2.4			V
Logic Output Low Voltage	V_{OL}	I_{OL} = –1.6 mA			0.45	V
Logic Input Current	I_{IN}				1	µA
Input Capacitance	C_{IN}			8		pF
LOGIC TIMING CHARACTERISTICS[4]		Note 5				
Chip Select Write Pulsewidth	t_{WCS}		150			ns
Write Setup	t_{WS}	t_{WCS} = 150 ns	0			ns
Write Hold	t_{WH}	t_{WCS} = 150 ns	0			ns
Address Setup	t_{AS}		0			ns
Address Hold	t_{AH}		0			ns
Load Setup	t_{LS}		70			ns
Load Hold	t_{LH}		50			ns
Write Data Setup	t_{WDS}	t_{WCS} = 150 ns	20			ns
Write Data Hold	t_{WDH}	t_{WCS} = 150 ns	0			ns
Load Data Pulsewidth	t_{LDW}		180			ns
Reset Pulsewidth	t_{RESET}		150			ns
Chip Select Read Pulsewidth	t_{RCS}		170			ns
Read Data Hold	t_{RDH}	t_{RCS} = 170 ns	20			ns
Read Data Setup	t_{RDS}	t_{RCS} = 170 ns	0			ns
Data to Hi Z	t_{DZ}	C_L = 10 pF			200	ns
Chip Select to Data	t_{CSD}	C_L = 100 pF			320	ns
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSS			100		ppm/V
Positive Supply Current	I_{DD}			7	12	mA
Negative Supply Current	I_{SS}	V_{SS} = –5.0 V	–10			mA
Power Dissipation	P_{DISS}	V_{SS} = 0 V		60		mW
		V_{SS} = –5 V		110		mW

NOTES

[1]All supplies can be varied ±5%, and operation is guaranteed. Device is tested with V_{DD} = +4.75 V.

[2]For single supply operation only (V_{REFL} = 0.0 V, V_{SS} = 0.0 V): Due to internal offset errors, INL and DNL are measured beginning at code 2 (002_H).

[3]Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.

[4]All parameters are guaranteed by design.

[5]All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

Specifications subject to change without notice.

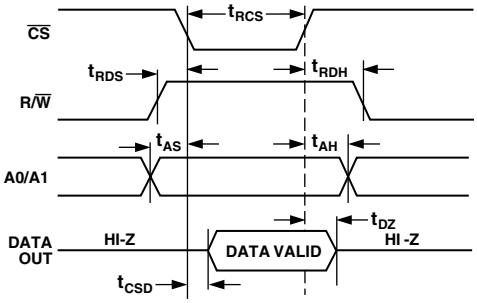


Figure 2. Data Output (Read Timing)

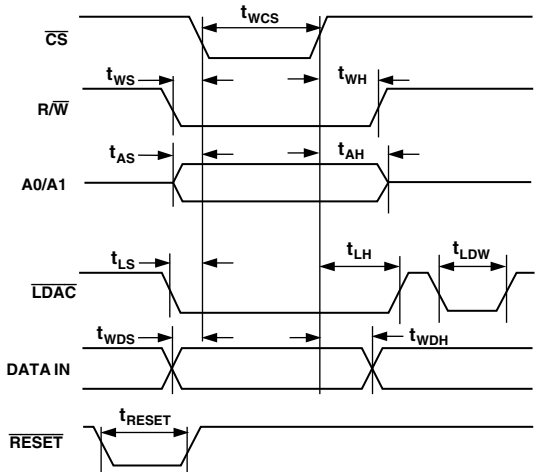


Figure 3. Data WRITE (Input and Output Registers) Timing

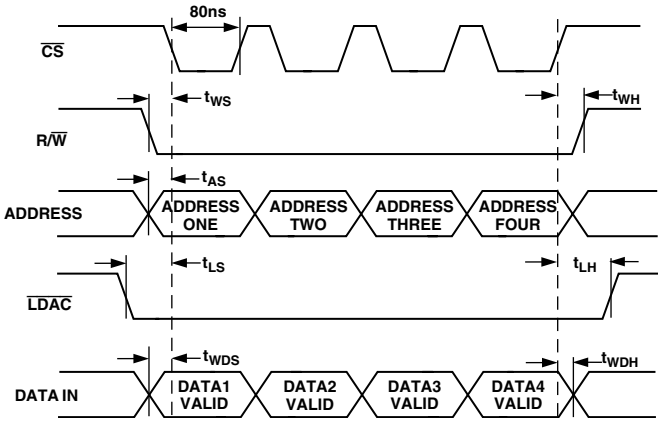


Figure 4. Single Buffer Mode

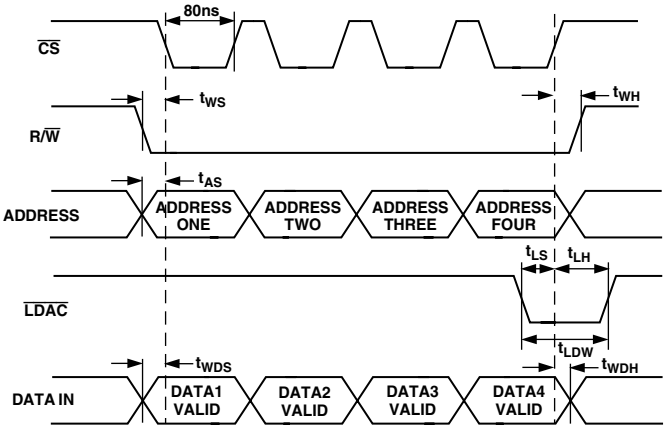
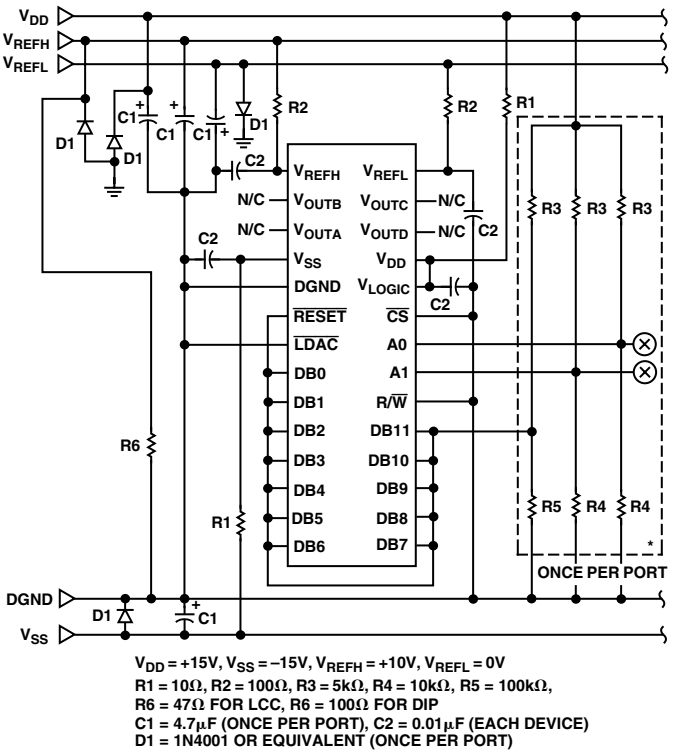


Figure 5. Double Buffer Mode



V_{DD} = +15V, V_{SS} = –15V, V_{REFH} = +10V, V_{REFL} = 0V
R1 = 10Ω, R2 = 100Ω, R3 = 5kΩ, R4 = 10kΩ, R5 = 100kΩ,
R6 = 47Ω FOR LCC, R6 = 100Ω FOR DIP
C1 = 4.7μF (ONCE PER PORT), C2 = 0.01μF (EACH DEVICE)
D1 = 1N4001 OR EQUIVALENT (ONCE PER PORT)

Figure 6. Burn-In Diagram

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{SS} to V_{DD} . . . . . –0.3 V, +33.0 V
V_{SS} to V_{LOGIC} . . . . . –0.3 V, +33.0 V
V_{LOGIC} to DGND . . . . . –0.3 V, +7.0 V
V_{SS} to V_{REFL} . . . . . –0.3 V, +V_{SS}–2.0 V
V_{REFH} to V_{DD} . . . . . +2.0 V, +33.0 V
V_{REFH} to V_{REFL} . . . . . +2.0 V, V_{SS}–V_{DD}
Current into Any Pin 4 . . . . . ±15 mA
Digital Input Voltage to DGND . . . . . –0.3 V, V_{LOGIC} +0.3 V
Digital Output Voltage to DGND . . . . . –0.3 V, +7.0 V
Operating Temperature Range
ET, FT, EP, FP, FPC . . . . . –40°C to +85°C
AT, BT, BTC . . . . . –55°C to +125°C
Dice Junction Temperature . . . . . +150°C
Storage Temperature . . . . . –65°C to +150°C
Power Dissipation Package . . . . . 1000 mW
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

Thermal Resistance

Package Type	θ_{JA}*	θ_{JC}	Units
28-Lead Plastic DIP (P)	48	22	°C/W
28-Lead Hermetic Leadless Chip Carrier (TC)	70	28	°C/W
28-Lead Plastic Leaded Chip Carrier (PC)	63	25	°C/W

*θ_{JA} is specified for worst-case mounting conditions, i. e., θ_{JA} is specified for device in socket.

ORDERING INFORMATION[1, 2]

INL (LSB)	Military[3] Temperature –55°C to +125°C	Extended Industrial[3] Temperature –40°C to +85°C	Package Description	Package Option
±1		DAC8412FPC	PLCC	P-28A
±1.5	DAC8412BTC/883		LCC	E-28A
0.5		DAC8412EP	Plastic DIP	N-28
±1		DAC8412FP	Plastic DIP	N-28
±1		DAC8413FPC	PLCC	P-28A
±1.5	DAC8413BTC/883		LCC	E-28A
±0.5		DAC8413EP	Plastic DIP	N-28
±1		DAC8413FP	Plastic DIP	N-28

NOTES
[1]Die Size 0.225 × 0.165 inches, 37,125 sq. mils (5.715 × 4.191 mm, 23.95 sq. mm). Substrate should be connected to V_{DD}; Transistor Count = 2595.
[2]Burn-in is available on extended industrial temperature range parts in cerdip.
[3]A complete /883 data sheet is available. For availability and burn-in information, contact your local sales office.

CAUTION

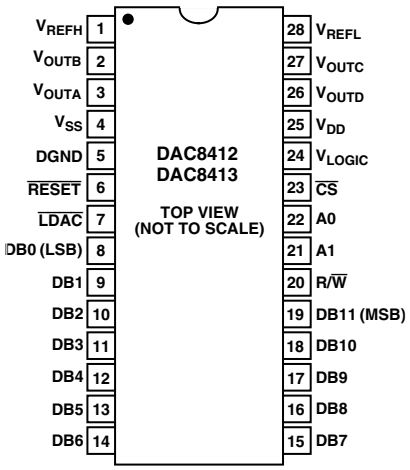
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper antistatic handling procedures.
3. Remove power before inserting or removing units from their sockets.
4. Analog outputs are protected from short circuit to ground or either supply.

PIN FUNCTION DESCRIPTIONS

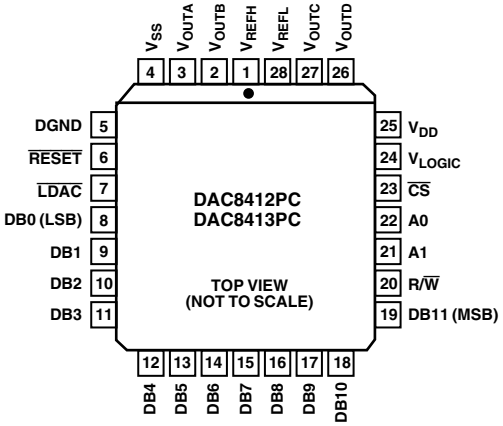
Pin	Name	Description
1	V_{REFH}	High-Side DAC Reference Input
2	V_{OUTB}	DAC B Output
3	V_{OUTA}	DAC A Output
4	V_{SS}	Lower-Rail Power Supply
5	DGND	Digital Ground
6	$\overline{RESET}$	Reset Input and Output Registers to all 0s, Enabled at Active Low
7	$\overline{LDAC}$	Load Data to DAC, Enabled at Active Low
8	DB0	Data Bit 0, LSB
9	DB1	Data Bit 1
10	DB2	Data Bit 2
11	DB3	Data Bit 3
12	DB4	Data Bit 4
13	DB5	Data Bit 5
14	DB6	Data Bit 6
15	DB7	Data Bit 7
16	DB8	Data Bit 8
17	DB9	Data Bit 9
18	DB10	Data Bit 10
19	DB11	Data Bit 11, MSB
20	R/$\overline{W}$	Active Low to Write Data to DAC. Active High to Readback Previous Data at Data Bit Pins with V_{LOGIC} Connected to +5 V
21	A1	Address Bit 1
22	A0	Address Bit 0
23	$\overline{CS}$	Chip Select, Enabled at Active Low
24	V_{LOGIC}	Voltage Supply for Readback Function. Can be Open Circuit If Not Used
25	V_{DD}	Upper-Rail Power Supply
26	V_{OUTD}	DAC D Output
27	V_{OUTC}	DAC C Output
28	V_{REFL}	Low-Side DAC Reference Input

PIN CONFIGURATIONS

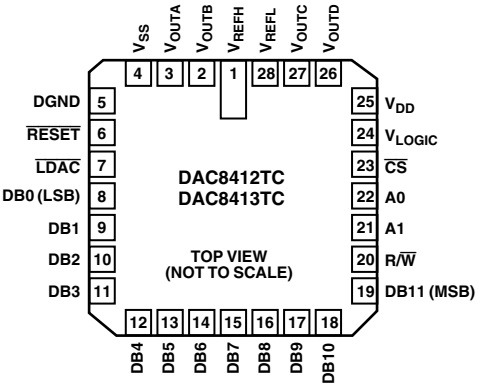
Plastic DIP



PLCC



LCC



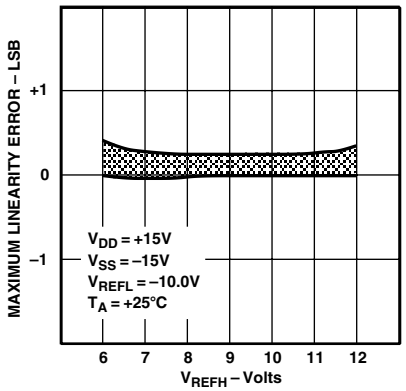


Figure 7. DNL vs. V_{REFH}

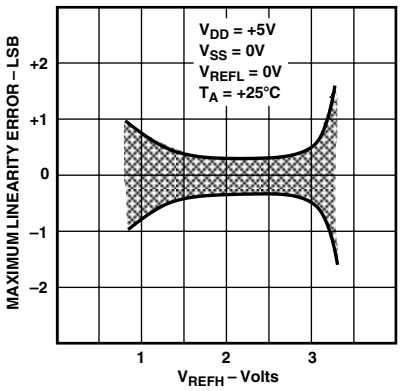


Figure 8. DNL vs. V_{REFH}

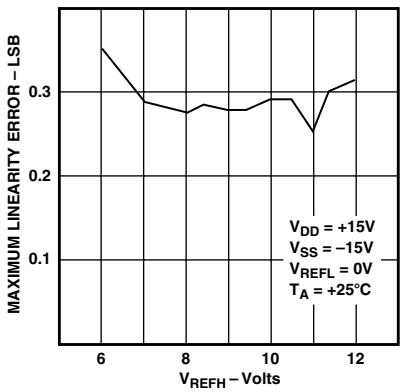


Figure 9. INL vs. V_{REFH}

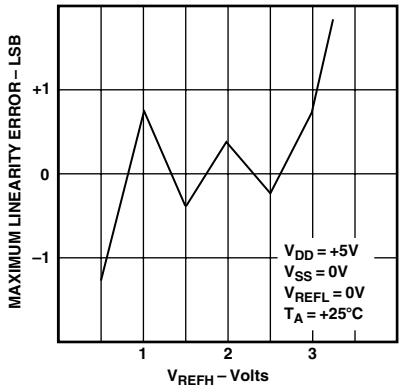


Figure 10. INL vs. V_{REFH}

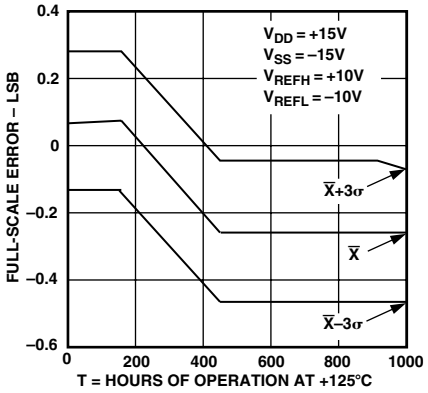


Figure 11. Full-Scale Error vs. Time Accelerated by Burn-In

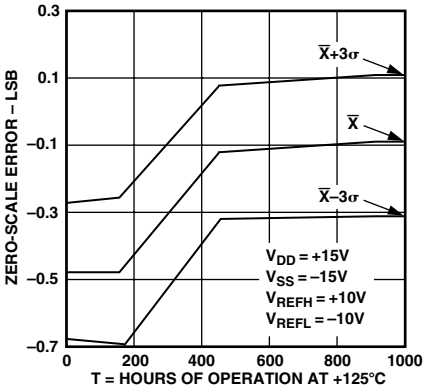


Figure 12. Zero-Scale Error vs. Time Accelerated by Burn-In

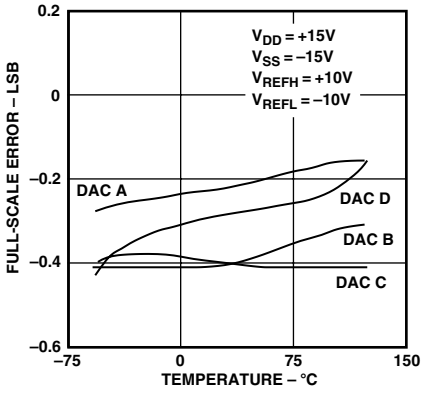


Figure 13. Full-Scale Error vs. Temperature

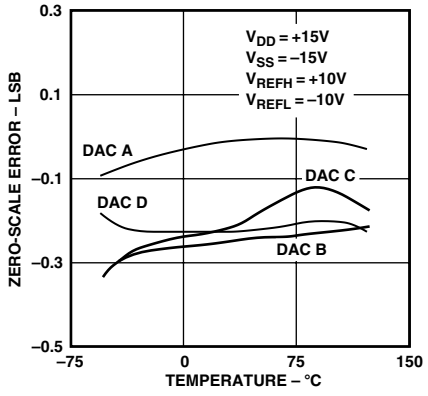


Figure 14. Zero-Scale Error vs. Temperature

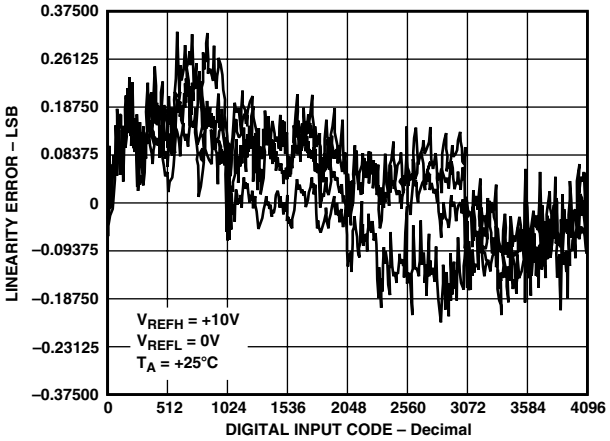


Figure 15. Channel-to-Channel Matching (V_{SUPPLY} = ±15 V)

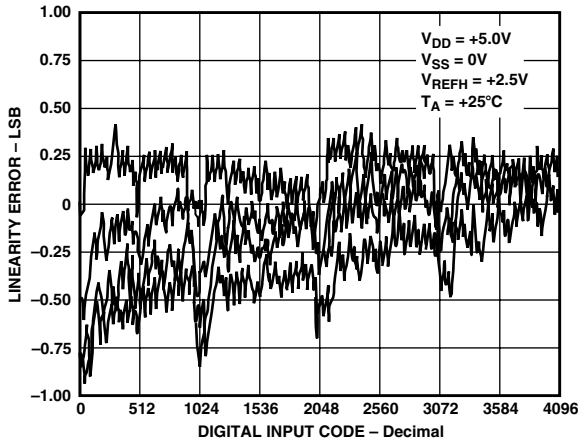


Figure 16. Channel-to-Channel Matching (V_{SUPPLY} = +5 V/GND)

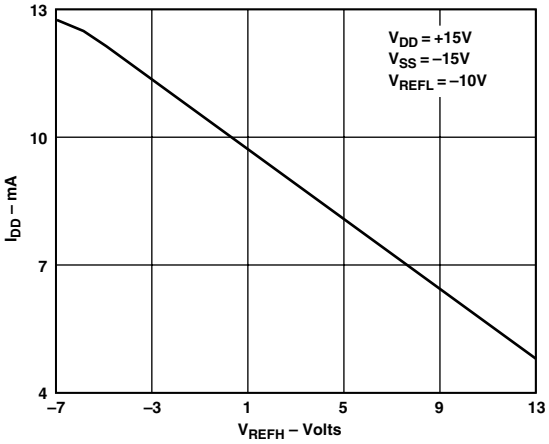


Figure 17. I_{DD} vs. V_{REFH} All DACs High

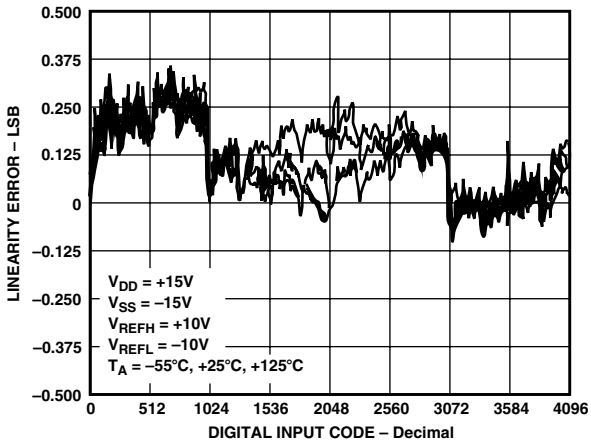


Figure 18. INL vs. Code

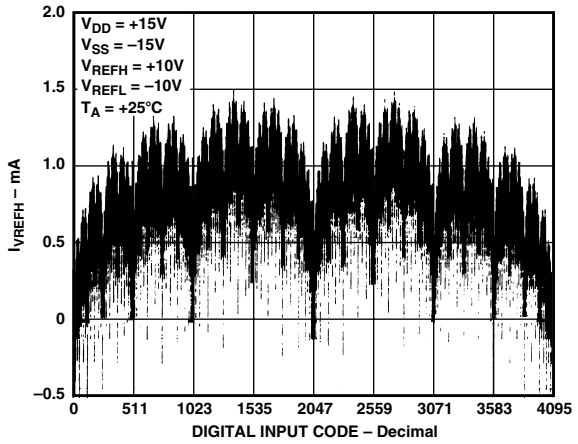


Figure 19. I_{VREFH} vs. Code

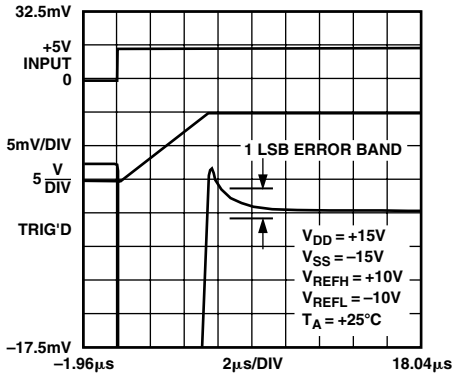


Figure 20. Settling Time (Positive)

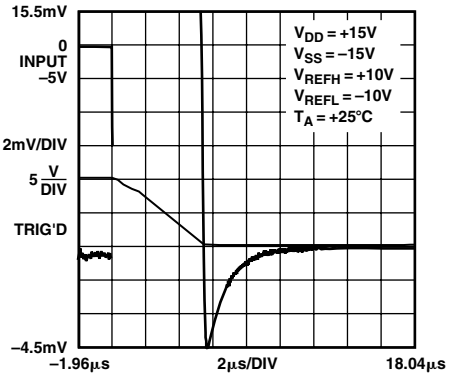


Figure 21. Settling Time (Negative)

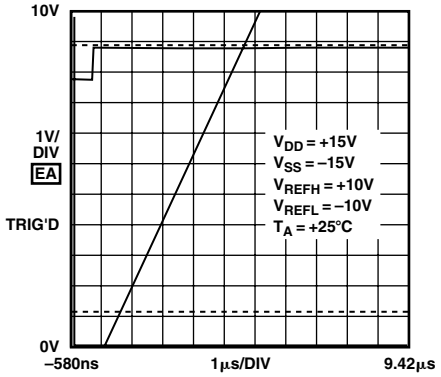


Figure 22. Positive Slew Rate

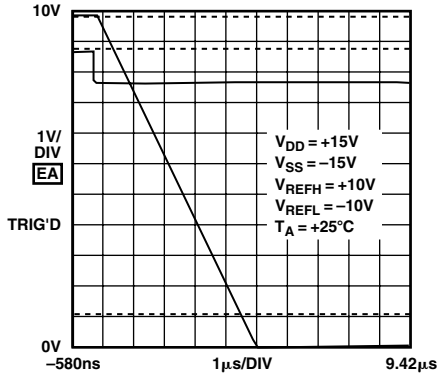


Figure 23. Negative Slew Rate

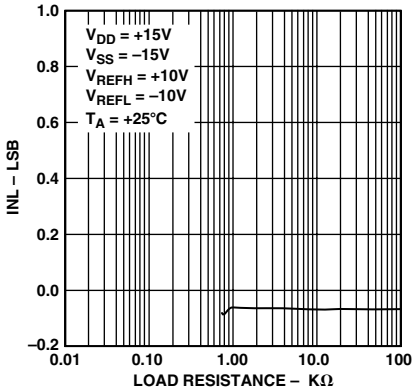


Figure 24. DAC 8412 INL vs. Load Resistance

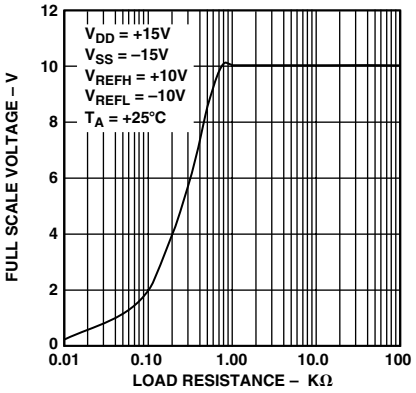


Figure 25. DAC 8412 Output Swing vs. Load Resistance

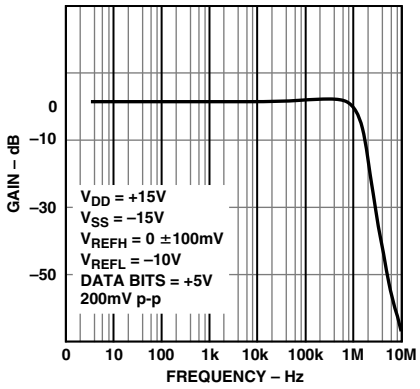


Figure 26. Small Signal Response

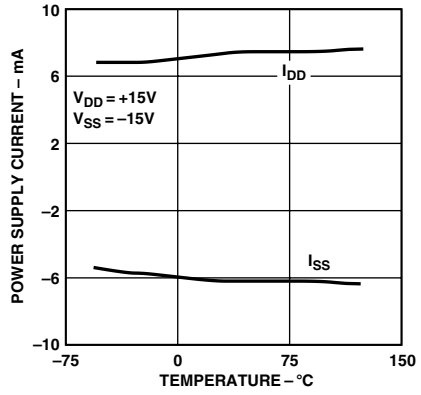


Figure 27. Power Supply Current vs. Temperature

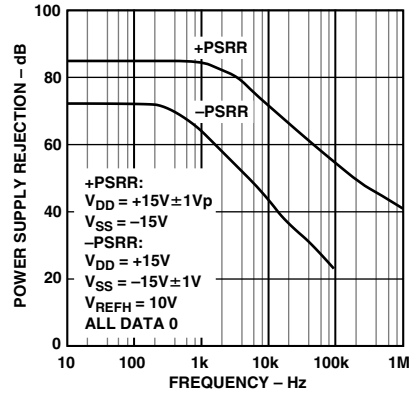


Figure 28. PSRR vs. Frequency

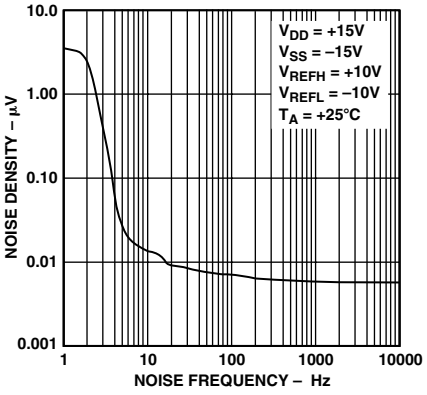


Figure 29. DAC8412 Noise Frequency vs. Noise Density

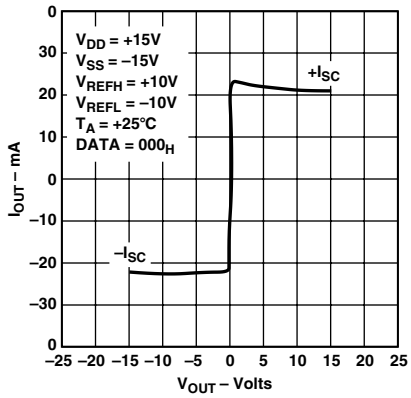


Figure 30. I_{OUT} vs. V_{OUT}

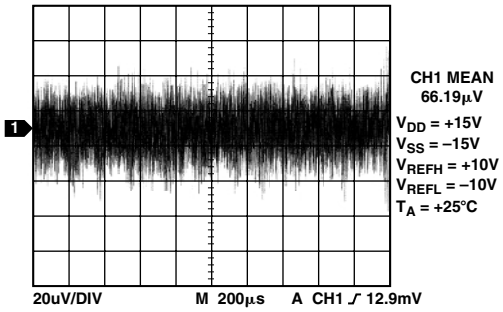


Figure 31. Broadband Noise

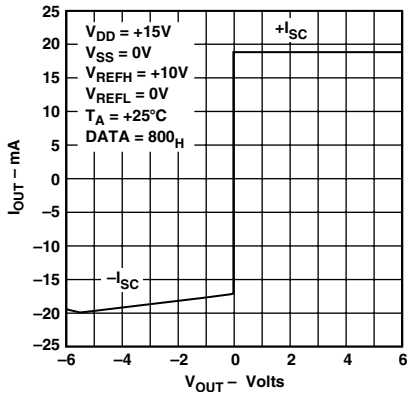


Figure 32. I_{OUT} vs. V_{OUT}

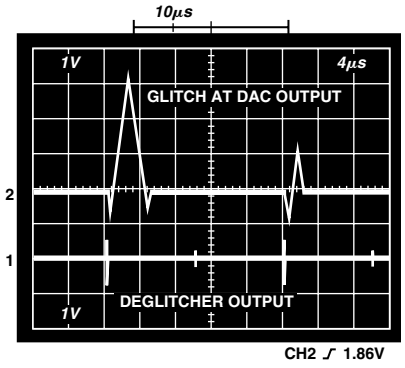


Figure 33. Glitch and Deglitched Results

OPERATION

Introduction

The DAC8412 and DAC8413 are quad, voltage output, 12-bit parallel input DACs featuring a 12-bit data bus with readback capability. The only differences between the DAC8412 and DAC8413 are the reset functions. The DAC8412 resets to mid-scale (code 800_H) and the DAC8413 resets to minimum scale (code 000_H).

The ability to operate from a single +5 V supply is a unique feature of these DACs.

Operation of the DAC8412 and DAC8413 can be viewed by dividing the system into three separate functional groups: the digital I/O and logic, the digital to analog converters and the output amplifiers.

DACs

Each DAC is a voltage switched, high impedance (R = 50 kΩ), R-2R ladder configuration. Each 2R resistor is driven by a pair of switches that connect the resistor to either V_{REFH} or V_{REFL}.

Glitch

Worst-case glitch occurs at the transition between half-scale digital code 1000 0000 0000 to half-scale minus 1 LSB, 0111 1111 1111. It can be measured at about 2 V μs. (See Figure 33.) For demanding applications such as waveform generation or precision instrumentation control, a deglitcher circuit can be implemented with a standard sample-and-hold circuit. (See Figure 34.) When $\overline{CS}$ is enabled by synchronizing the hold period to be longer than the glitch tradition, the output voltage can be smoothed with minimum disturbance. A quad sample-and-hold amplifier, SMP04, has been used to illustrate the deglitching result. (See Figure 33.)

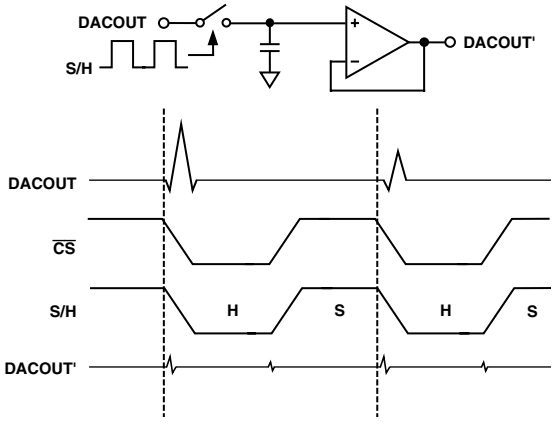


Figure 34. Deglitcher Circuit

Reference Inputs
All four DACs share common reference high (V_{REFH}) and reference low (V_{REFL}) inputs. The voltages applied to these reference inputs set the output high and low voltage limits of all four of the DACs. Each reference input has voltage restrictions with respect to the other reference and to the power supplies. The V_{REFL} can be set at any voltage between V_{SS} and V_{REFH} – 2.5 V, and V_{REFH} can be set to any value between $+V_{DD}$ – 2.5 V and V_{REFL} + 2.5 V. Note that because of these restrictions the DAC8412 references cannot be inverted (i.e., V_{REFL} cannot be greater than V_{REFH}).

It is important to note that the DAC8412's V_{REFH} input both sinks and sources current. Also the input current of both V_{REFH} and V_{REFL} are code dependent. Many references have limited current sinking capability and must be buffered with an amplifier to drive V_{REFH}. The V_{REFL} has no such special requirements.

It is recommended that the reference inputs be bypassed with 0.2 µF capacitors when operating with ±10 V references. This limits the reference bandwidth.

Digital I/O
See Table I for digital control logic truth table. Digital I/O consists of a 12-bit bidirectional data bus, two registers select inputs, A0 and A1, a R/$\overline{W}$ input, a $\overline{RESET}$ input, a Chip Select ($\overline{CS}$), and a Load DAC ($\overline{LDAC}$) input. Control of the DACs and bus direction is determined by these inputs as shown in Table I. Digital data bits are labeled with the MSB defined as data bit "11" and the LSB as data bit "0." All digital pins are TTL/CMOS compatible.

See Figure 35 for a simplified I/O logic diagram. The register select inputs A0 and A1 select individual DAC registers "A" (binary code 00) through "D" (binary code 11). Decoding of the registers is enabled by the $\overline{CS}$ input. When $\overline{CS}$ is high no decoding takes place, and neither the writing nor the reading of the input registers is enabled. The loading of the second bank of registers is controlled by the asynchronous $\overline{LDAC}$ input. By taking $\overline{LDAC}$ low while $\overline{CS}$ is enabled, all output registers can be updated simultaneously. Note that the t_{LDW} required pulsewidth for updating all DACs is a minimum of 170 ns.

The R/$\overline{W}$ input, when enabled by $\overline{CS}$, controls the writing to and reading from the input register.

Coding
Both the DAC8412 and DAC8413 use binary coding. The output voltage can be calculated by:

$$V_{OUT} = V_{REFL} + \frac{(V_{REFH} - V_{REFL}) \times N}{4096}$$

where N is the digital code in decimal.

$\overline{RESET}$
The $\overline{RESET}$ function can be used either at power-up or at any time during the DAC's operation. The $\overline{RESET}$ function is independent of $\overline{CS}$. This pin is active LOW and sets the DAC output registers to either center code for the DAC8412, or zero code for the DAC8413. The reset to center code is most useful when the DAC is configured for bipolar references and an output of zero volts after reset is desired.

Supplies
Supplies required are V_{SS}, V_{DD} and V_{LOGIC}. The V_{SS} supply can be set between –15 V and 0 V. V_{DD} is the positive supply; its operating range is between +5 V and +15 V.

V_{LOGIC} is the digital output supply voltage for the readback function. It is normally connected to +5 V. This pin is a logic reference input only. It does not supply current to the device. *If you are not using the readback function, V_{LOGIC} can be left open-circuit.* While V_{LOGIC} does not supply current to the DAC8412, it does supply currents to the digital outputs when readback is used.

Amplifiers
Unlike many voltage output DACs, the DAC8412 features buffered voltage outputs. Each output is capable of both sourcing and sinking 5 mA at ±10 volts, eliminating the need for external amplifiers when driving 500 pF or smaller capacitive load in most applications. These amplifiers are short-circuit protected.

Table I. DAC8412/DAC8413 Logic Table

A1	A0	R/$\overline{W}$	$\overline{CS}$	$\overline{RS}$	$\overline{LDAC}$	INPUT REG	OUTPUT REG	MODE	DAC
L	L	L	L	H	L	WRITE	WRITE	Transparent	A
L	H	L	L	H	L	WRITE	WRITE	Transparent	B
H	L	L	L	H	L	WRITE	WRITE	Transparent	C
H	H	L	L	H	L	WRITE	WRITE	Transparent	D
L	L	L	L	H	H	WRITE	HOLD	WRITE INPUT	A
L	H	L	L	H	H	WRITE	HOLD	WRITE INPUT	B
H	L	L	L	H	H	WRITE	HOLD	WRITE INPUT	C
H	H	L	L	H	H	WRITE	HOLD	WRITE INPUT	D
L	L	H	L	H	H	READ	HOLD	READ INPUT	A
L	H	H	L	H	H	READ	HOLD	READ INPUT	B
H	L	H	L	H	H	READ	HOLD	READ INPUT	C
H	H	H	L	H	H	READ	HOLD	READ INPUT	D
X	X	X	H	H	L	HOLD	Update all output registers		All
X	X	X	H	H	H	HOLD	HOLD	HOLD	All
X	X	X	X	L	X	*All registers reset to mid/zero-scale			All
X	X	X	H	↓	X	*All registers latched to mid/zero-scale			All

*DAC8412 resets to midscale, and DAC8413 resets to zero scale. L = Logic Low; H = Logic High; X - Don't Care. Input and Output registers are transparent when asserted.

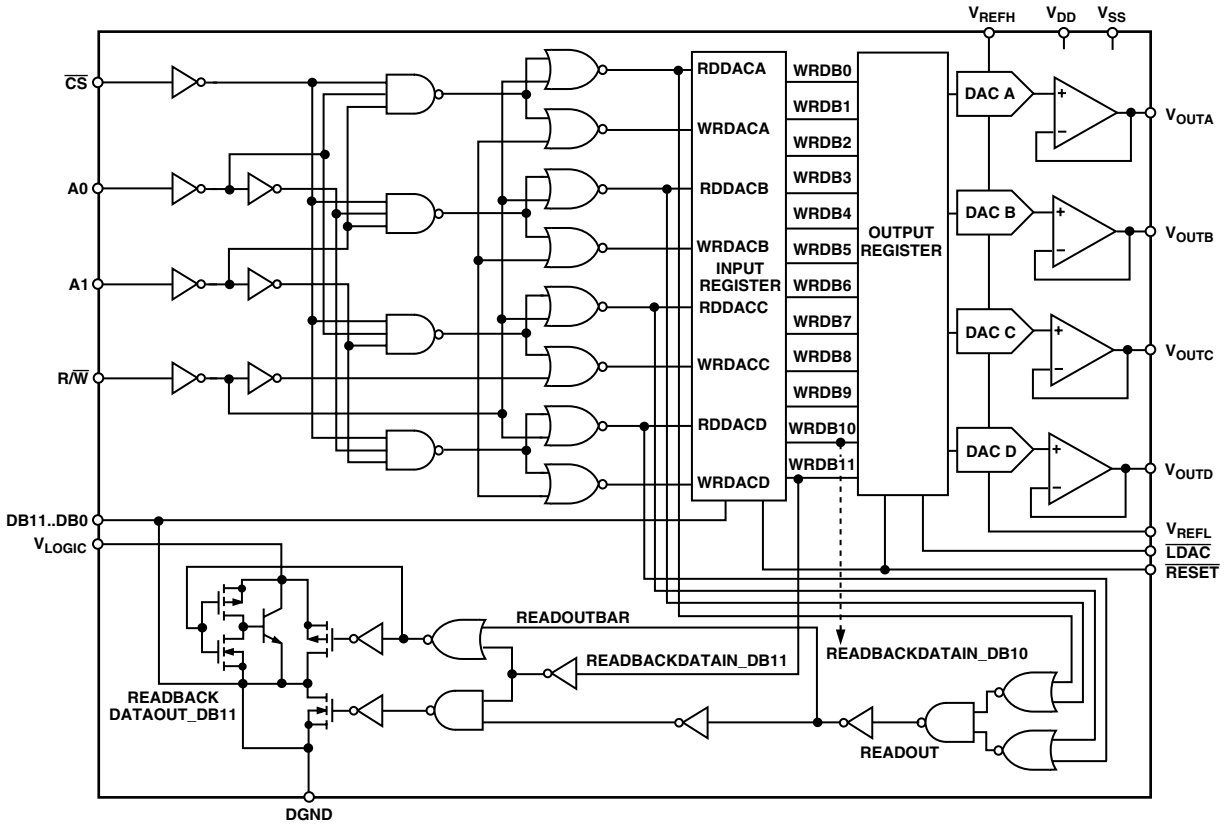


Figure 35. Simplified I/O Logic Diagram

Careful attention to grounding is important to accurate operation of the DAC8412. This is not because the DAC8412 is more sensitive than other 12-bit DACs, but because with four outputs and two references there is greater potential for ground loops. Since the DAC8412 has no analog ground, the ground must be specified with respect to the reference.

Reference Configurations

Output voltage ranges can be configured as either unipolar or bipolar, and within these choices a wide variety of options exists. The unipolar configuration can be either positive or negative voltage output, and the bipolar configuration can be either symmetrical or nonsymmetrical.

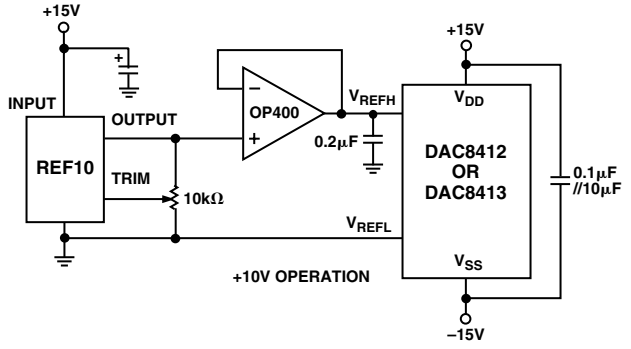


Figure 36. Unipolar +10 V Operation

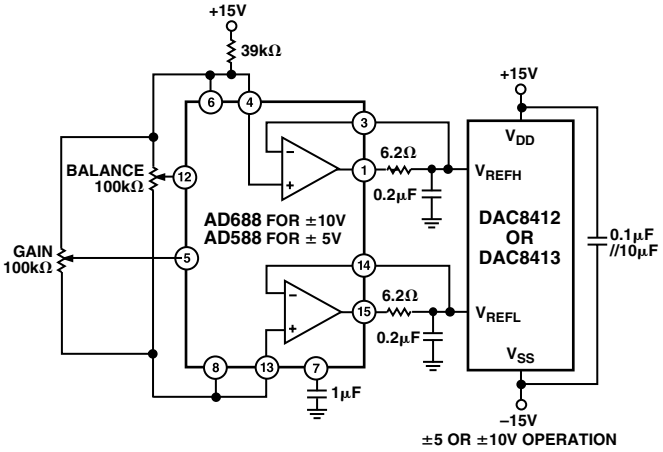


Figure 37. Symmetrical Bipolar Operation

Figure 37 (Symmetrical Bipolar Operation) shows the DAC8412 configured for ±10 V operation. *Note: See the AD688 data sheet for a full explanation of reference operation.* Adjustments may not be required for many applications since the AD688 is a very high accuracy reference. However if additional adjustments are required, adjust the DAC8412 full scale first. Begin by loading the digital full-scale code (FFF_H), and then adjust the Gain Adjust potentiometer to attain a DAC output voltage of 9.9976 V. Then, adjust the Balance Adjust to set the center scale output voltage to 0.000 V.

The 0.2 µF bypass capacitors shown at the reference inputs in Figure 37 should be used whenever ±10 V references are used. Applications with single references or references to ±5 V may not require the 0.2 µF bypassing. The 6.2 Ω resistor in series with the output of the reference amplifier is to keep the amplifier from oscillating with the capacitive load. We have found that this is large enough to stabilize this circuit. Larger resistor values are acceptable, provided that the drop across the resistor doesn't exceed a V_{BE}. Assuming a minimum V_{BE} of 0.6 V and a maximum current of 2.75 mA, then the resistor should be under 200 Ω for the loading of a single DAC8412.

Using two separate references is not recommended. Having two references could cause different drifts with time and temperature; whereas with a single reference, most drifts will track.

Unipolar positive full-scale operation can usually be set with a reference with the correct output voltage. This is preferable to using a reference and dividing down to the required value. For a 10 V full-scale output, the circuit can be configured as shown in Figure 38. In this configuration the full-scale value is set first by adjusting the 10 kΩ resistor for a full-scale output of 9.9976 V.

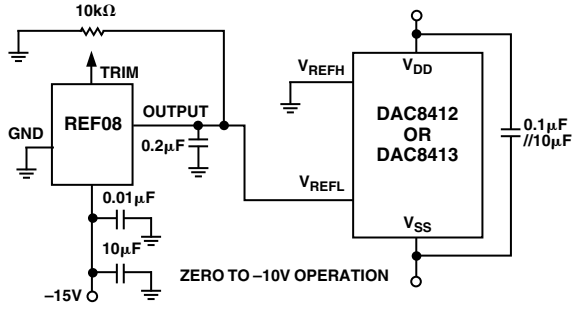


Figure 38. Unipolar –10 V Operation

Figure 38 shows the DAC8412 configured for –10 V to 0 V operation. A REF08 with a –10 V output is connected directly to V_{REFL} for the reference voltage.

Single +5 V Supply Operation

For operation with a +5 V supply, the reference voltage should be set between 1.0 V and +2.5 V for optimum linearity. Figure 39 shows a REF43 used to supply a +2.5 V reference voltage. The headroom of the reference and DAC are both sufficient to support a +5 V supply with ±5% tolerance. V_{DD} and V_{LOGIC} should be connected to the same supply. Separate bypassing to each pin should also be used.

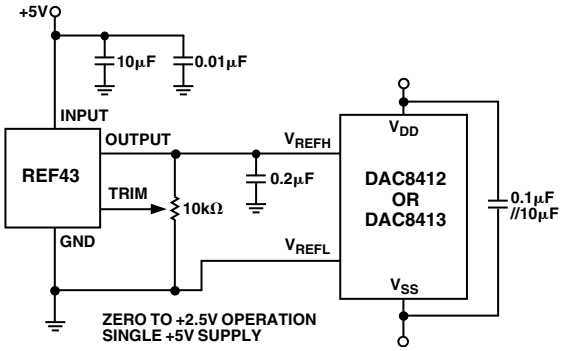
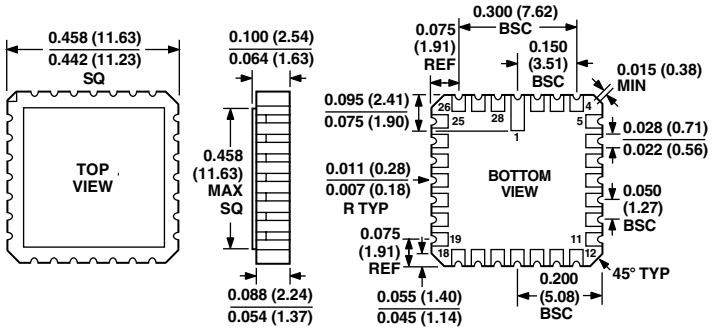


Figure 39. +5 V Single Supply Operation

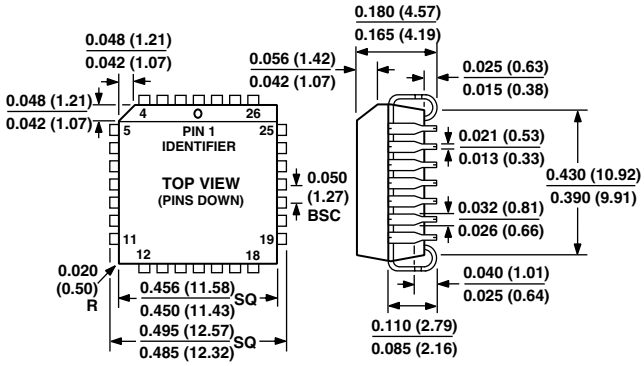
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

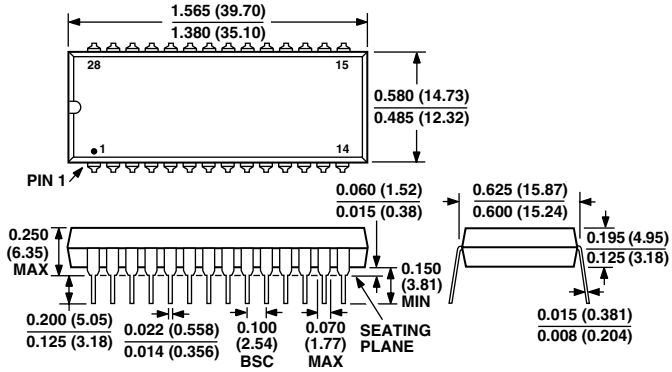
28-Position Leadless Chip Carrier
(TC Suffix)



28-Lead PLCC (P-28A)
(PC Suffix)



28-Lead Epoxy DIP (N-28)
(P Suffix)



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