

GD54/74HC298, GD54/74HCT298

QUAD 2-INPUT MULTIPLEXERS WITH OUTPUT LATCH

General Description

These devices are identical in pinout to the 54/74LS298. They select one of two 4-bit words to be stored in the output latch according to clock timing. When the word select input is taken low word 1 (A₁, B₁, C₁ and D₁) is presented to the inputs of the flip-flops, and when it is taken high word 2 (A₂, B₂, C₂ and D₂) is presented to the inputs of the flip-flops. The selected word is clocked to the output terminals on the falling edge of the clock pulse. This device is the equivalent of a quad 2-input multiplexer followed by a 4-bit edge-triggered latch. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

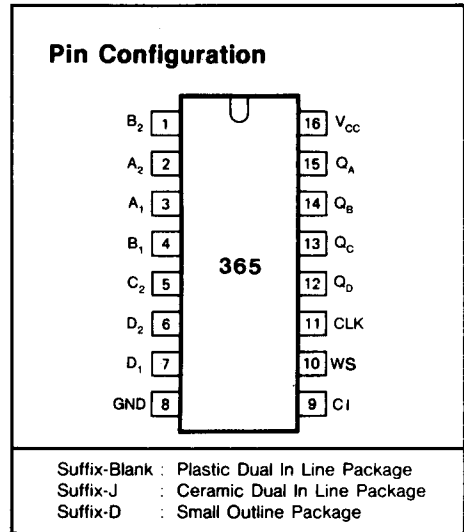
Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q _A	Q _B	Q _C	Q _D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q _{A0}	Q _{B0}	Q _{C0}	C _{D0}

H = High level (steady state)
 L = LOW level (steady state)
 X = Irrelevant (any input, including transitions)
 ↓ = transition from high to low level
 a1, a2, etc. = the level of steady-state input at A1, A2, etc.
 Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most-recent, ↓ transition of the clock input.



Logic Diagram

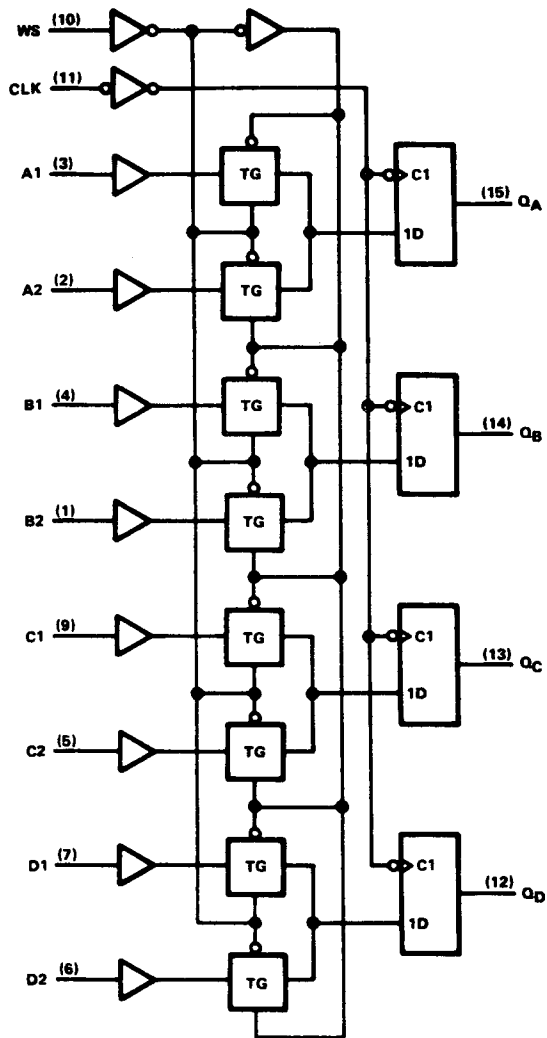


Fig. 1 Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HC298		GD54HC298		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		
V _{IH}	HIGH level Voltage		2.0	1.5			1.5		1.5		V	
			4.5	3.15			3.15		3.15			
			6.0	4.2			4.2		4.2			
V _{IL}	LOW level input voltage		2.0			0.3		0.3		0.3	V	
			4.5			0.9		0.9		0.9		
			6.0			1.2		1.2		1.2		
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH}	I _{OH} = -20μA	2.0	1.9	2.0		1.9		1.9	V	
				4.5	4.4	4.5		4.4		4.4		
				6.0	5.9	6.0		5.9		5.9		
		or V _{IL}	I _{OH} = -4mA I _{OH} = -5.2mA	4.5	3.98	4.3		3.84		3.7		
				6.0	5.48	5.2		5.34		5.2		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH}	I _{OL} = 20μA	2.0			0.1		0.1		V	
				4.5			0.1		0.1			0.1
				6.0			0.1		0.1			0.1
		or V _{IL}	I _{OL} = 4mA I _{OL} = 5.2mA	4.5		0.17	0.26		0.33			0.4
				6.0		0.15	0.26		0.33			0.4
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	6.0			0.1		1.0		1.0	μA	
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	6.0			8		80		160	μA	

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HCT298		GD54HCT298		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V	
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V	
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH}	I _{OH} = -20μA	4.5	4.4	4.5		4.4		4.4	V	
				4.5	3.98	4.3		3.84		3.7		
				6.0								
		or V _{IL}	I _{OH} = -4mA	4.5			0.1		0.1			0.1
				4.5		0.17	0.26		0.33			0.4
				6.0								
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	5.5			0.1		1.0		1.0	μA	
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	5.5			8		80		160	μA	

Timing Requirements for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HC298		GD54HC298		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _w	Pulse width	CLK high or low	2.0	75			95		115		ns
			4.5	15			19		23		
			6.0	13			16		20		
t _{su}	Setup time	WS, Data before CLK ↓	2.0	80			105		115		ns
			4.5	16			21		25		
			6.0	14			18		21		
t _h	Hold time	WS, Data after CLK ↓	2.0	0			0		0		ns
			4.5	0			0		0		
			6.0	0			0		0		

AC Characteristics for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HC298		GD54HC298		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f _{max}	Maximum Clock Pulse Frequency		2.0	6.5			5.5		4.3		MHz
			4.5	33			27		22		
			6.0	38			31		25		
t _{PLH} / t _{PHL}	Propagation Delay Time CLK to Q _n		2.0		46	120		155		190	ns
			4.5		15	25		31		38	
			6.0		12	21		21		31	
t _{TLH} / t _{THL}	Output Transition Time		2.0		19	75		95		110	ns
			4.5		7	15		19		22	
			6.0		6	13		16		19	

AC Waveforms

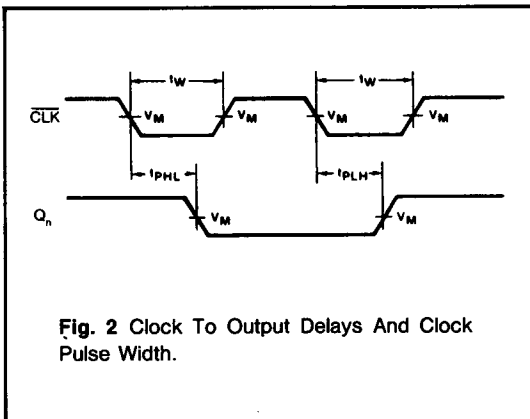


Fig. 2 Clock To Output Delays And Clock Pulse Width.

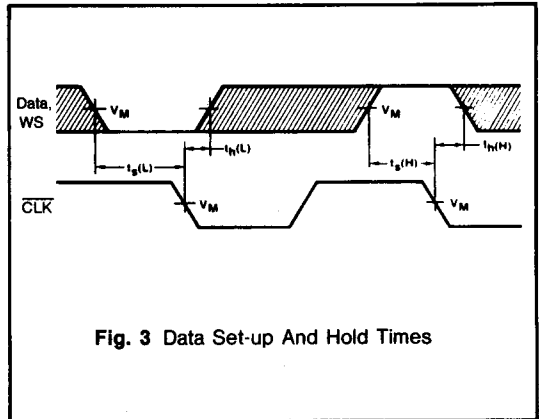


Fig. 3 Data Set-up And Hold Times

Note to AC waveforms

- (1) HC : V_M=50%; V_L=GND to V_{CC}.
- HCT : V_M=1.3V; V_L=GND to 3V.

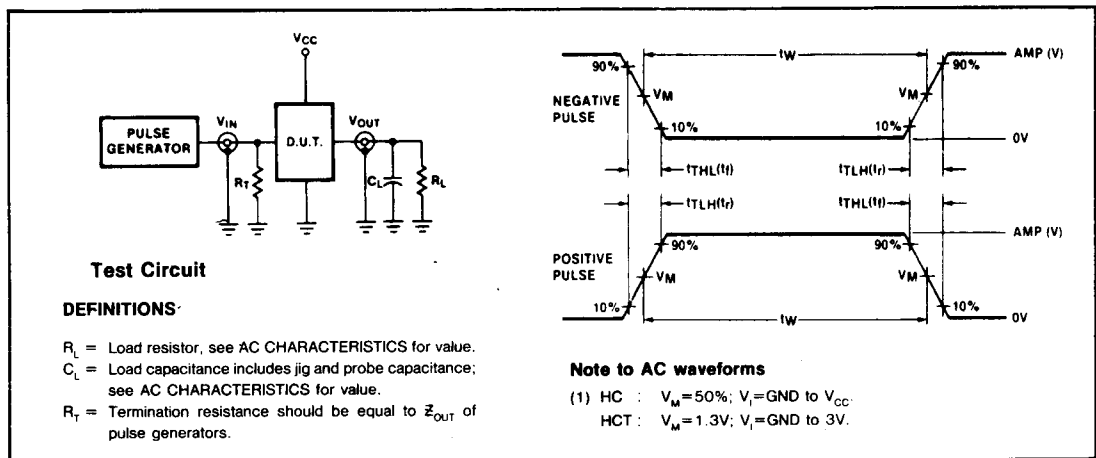
Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT298		GD54HCT298		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high or low	4.5	19			23		27		ns
t_{su}	Setup time	WS, Data before CLK \downarrow	4.5	17			21		26		ns
t_h	Hold time	WS, Data after CLK \downarrow	4.5	17			21		26		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT298		GD54HCT298		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		4.5	30			26		20		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Q_n		4.5		19	29	35		42		ns
$t_{TLH}/$ t_{THL}	Output Transition Time		4.5		7	15	19		22		ns

Typical Clear, Shift, and Clear Sequences



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