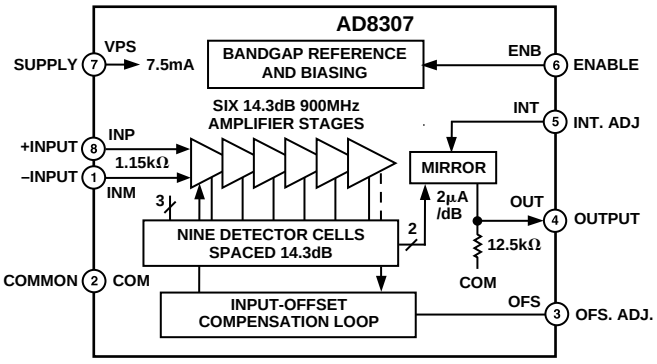
Low Cost DC-500 MHz, 92 dB Logarithmic Amplifier

AD8307

FEATURES
Complete Multistage Logarithmic Amplifier
92 dB Dynamic Range: –75 dBm to +17 dBm
to –90 dBm Using Matching Network
Single Supply of 2.7 V Min at 7.5 mA Typical
DC-500 MHz Operation, ±1 dB Linearity
Slope of 25 mV/dB, Intercept of –84 dBm
Highly Stable Scaling Over Temperature
Fully Differential DC-Coupled Signal Path
100 ns Power-Up Time, 150 μA Sleep Current

APPLICATIONS
Conversion of Signal Level to Decibel Form
Transmitter Antenna Power Measurement
Receiver Signal Strength Indication (RSSI)
Low Cost Radar and Sonar Signal Processing
Network and Spectrum Analyzers (to 120 dB)
Signal Level Determination Down to 20 Hz
True Decibel AC Mode for Multimeters

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD8307 is the first logarithmic amplifier in an 8-lead (SO-8) package. It is a complete 500 MHz monolithic demodulating logarithmic amplifier based on the progressive compression (successive detection) technique, providing a dynamic range of 92 dB to ±3 dB law-conformance and 88 dB to a tight ±1 dB error bound at all frequencies up to 100 MHz. It is extremely stable and easy to use, requiring no significant external components. A single supply voltage of 2.7 V to 5.5 V at 7.5 mA is needed, corresponding to an unprecedented power consumption of only 22.5 mW at 3 V. A fast-acting CMOS-compatible control pin can disable the AD8307 to a standby current of under 150 μA.

Each of the cascaded amplifier/limiter cells has a small-signal gain of 14.3 dB, with a –3 dB bandwidth of 900 MHz. The input is fully differential and at a moderately high impedance (1.1 kΩ in parallel with about 1.4 pF). The AD8307 provides a basic dynamic range extending from approximately –75 dBm (where dBm refers to a 50 Ω source, that is, a sine amplitude of about ±56 μV) up to +17 dBm (a sine amplitude of ±2.2 V). A simple input-matching network can lower this range to –88 dBm to +3 dBm. The logarithmic linearity is typically within ±0.3 dB up to 100 MHz over the central portion of this range, and is degraded only slightly at 500 MHz. There is no minimum frequency limit; the AD8307 may be used at audio frequencies (20 Hz) or even lower.

The output is a voltage scaled 25 mV/dB, generated by a current of nominally 2 μA/dB through an internal 12.5 kΩ resistor. This voltage varies from 0.25 V at an input of –74 dBm (that is, the ac intercept is at –84 dBm, a 20 μV rms sine input), up to 2.5 V for an input of +16 dBm. This slope and intercept can be trimmed using external adjustments. Using a 2.7 V supply, the output scaling may be lowered, for example to 15 mV/dB, to permit utilization of the full dynamic range.

The AD8307 exhibits excellent supply insensitivity and temperature stability of the scaling parameters. The unique combination of low cost, small size, low power consumption, high accuracy and stability, very high dynamic range, and a frequency range encompassing audio through IF to UHF, make this product useful in numerous applications requiring the reduction of a signal to its decibel equivalent.

The AD8307 is available in the industrial temperature range of –40°C to +85°C, and in 8-lead SOIC and PDIP packages.

REV. A

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AD8307–SPECIFICATIONS (V_S = +5 V, T_A = 25°C, $R_L \geq 1$ MΩ, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
GENERAL CHARACTERISTICS					
Input Range (±1 dB Error)	Expressed in dBm re 50 Ω	–72		16	dBm
Logarithmic Conformance	f ≤ 100 MHz, Central 80 dB		±0.3	±1	dB
	f = 500 MHz, Central 75 dB		±0.5		dB
Logarithmic Slope	Unadjusted[1]	23	25	27	mV/dB
vs. Temperature		23		27	mV/dB
Logarithmic Intercept	Sine Amplitude; Unadjusted[2]		20		µV
	Equivalent Sine Power in 50 Ω	–87	–84	–77	dBm
vs. Temperature		–88		–76	dBm
Input Noise Spectral Density	Inputs Shorted		1.5		nV/√Hz
Operating Noise Floor	R_{SOURCE} = 50 Ω/2		–78		dBm
Output Resistance	Pin 4 to Ground	10	12.5	15	kΩ
Internal Load Capacitance			3.5		pF
Response Time	Small Signal, 10%-90%, 0 mV–100 mV, C_L = 2 pF		400		ns
	Large Signal, 10%-90%, 0 V–2.4 V, C_L = 2 pF		500		ns
Upper Usable Frequency[3]			500		MHz
Lower Usable Frequency	Input AC-Coupled		10		Hz
AMPLIFIER CELL CHARACTERISTICS					
Cell Bandwidth	–3 dB		900		MHz
Cell Gain			14.3		dB
INPUT CHARACTERISTICS					
DC Common-Mode Voltage	Inputs AC-Coupled		3.2		V
Common-Mode Range	Either Input (Small Signal)	–0.3	1.6	V_S – 1	V
DC Input Offset Voltage[4]	$R_{SOURCE} \leq$ 50 Ω		50	500	µV
	Drift		0.8		µV/°C
Incremental Input Resistance	Differential		1.1		kΩ
Input Capacitance	Either Pin to Ground		1.4		pF
Bias Current	Either Input		10	25	µA
POWER INTERFACES					
Supply Voltage		2.7		5.5	V
Supply Current	$V_{ENB} \geq$ 2 V		8	10	mA
Disabled	$V_{ENB} \leq$ 1 V		150	750	µA

NOTES

[1]This may be adjusted downward by adding a shunt resistor from the Output to Ground. A 50 kΩ resistor will reduce the nominal slope to 20 mV/dB.

[2]This may be adjusted in either direction by a voltage applied to Pin 5, with a scale factor of 8 dB/V.

[3]See Application on 900 MHz operation.

[4]Normally nulled automatically by internal offset correction loop. May be manually nulled by a voltage applied between Pin 3 and Ground; see APPLICATIONS.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . +7.5 V
Input Voltage (Pins 1, 8) . . . . . V_{SUPPLY}
Storage Temperature Range, N, R . . . . . –65°C to +125°C
Ambient Temperature Range, Rated Performance Industrial,
AD8307AN, AD8307AR . . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

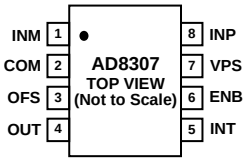
ORDERING GUIDE

Model	Temperature Range	Package Descriptions	Package Options
AD8307AR	–40°C to +85°C	SOIC	SO-8
AD8307AN	–40°C to +85°C	Plastic DIP	N-8
AD8307AR-REEL		13" REEL	
AD8307AR-REEL7		7" REEL	
AD8307-EB		Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8307 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Name	Function
1	INM	Signal Input, Minus Polarity; Normally at $V_{POS}/2$.
2	COM	Common Pin (Usually Grounded).
3	OFS	Offset Adjustment; External Capacitor Connection.
4	OUT	Logarithmic (RSSI) Output Voltage; R_{OUT} = 12.5 kΩ.
5	INT	Intercept Adjustment; ±6 dB (See Text).
6	ENB	CMOS-compatible Chip Enable; Active when "HI."
7	VPS	Positive Supply, 2.7 V–5.5 V.
8	INP	Signal Input, Plus Polarity; Normally at $V_{POS}/2$. Note: Due to the symmetrical nature of the response, there is no special significance to the sign of the two input pins. DC resistance from INP to INM = 1.1 kΩ.

AD8307–Typical Performance Characteristics

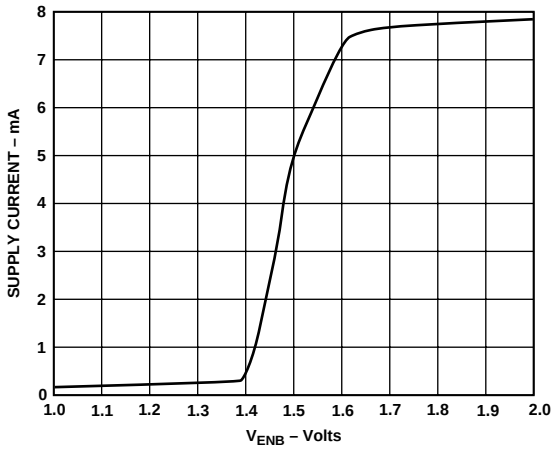


Figure 1. Supply Current vs. V_{ENB} Voltage (5 V)

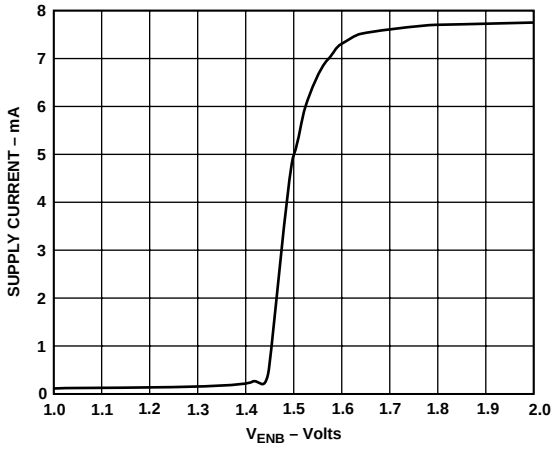


Figure 2. Supply Current vs. V_{ENB} Voltage (3 V)

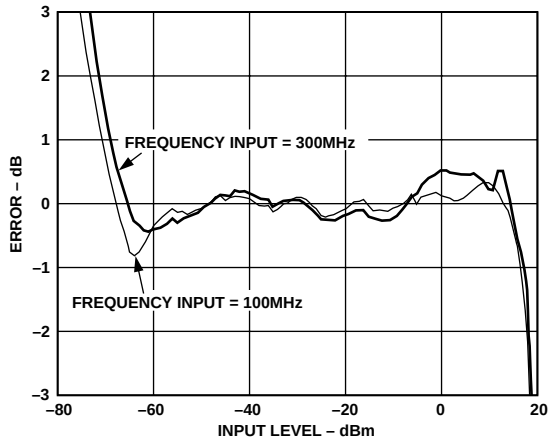


Figure 3. Log Conformance vs. Input Level (dBm) @ 100 MHz, 300 MHz

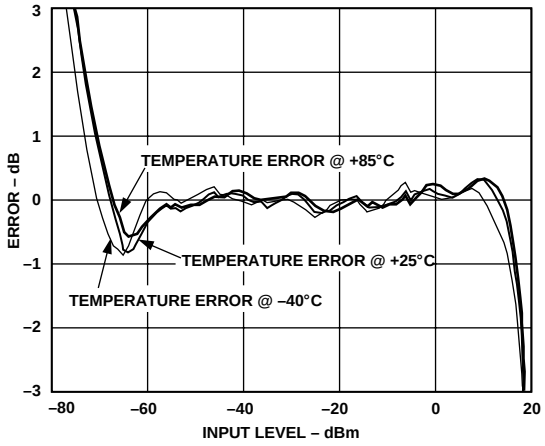


Figure 4. Log Conformance vs. Input Level (dBm) at 25°C, 85°C, –40°C

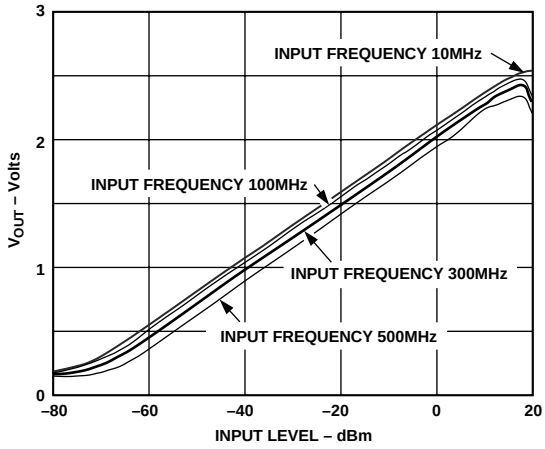


Figure 5. V_{OUT} vs. Input Level (dBm) at Various Frequencies

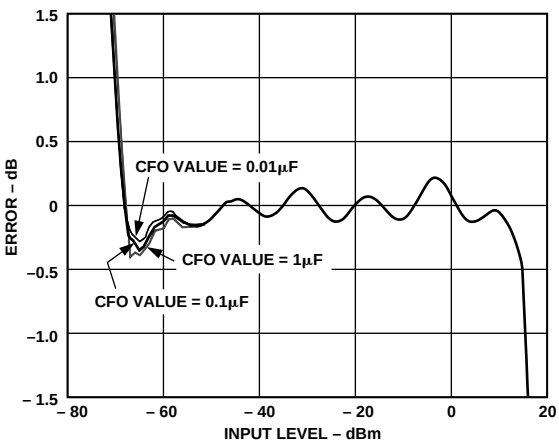


Figure 6. Log Conformance vs. CFO Values at 1 kHz Input Frequency

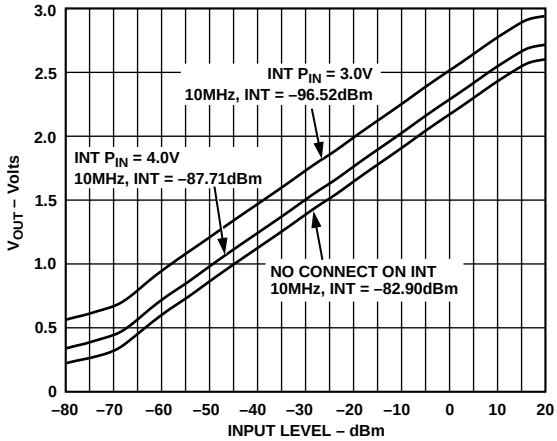


Figure 7. V_{OUT} vs. Input Level at 5 V Supply; Showing Intercept Adjustment

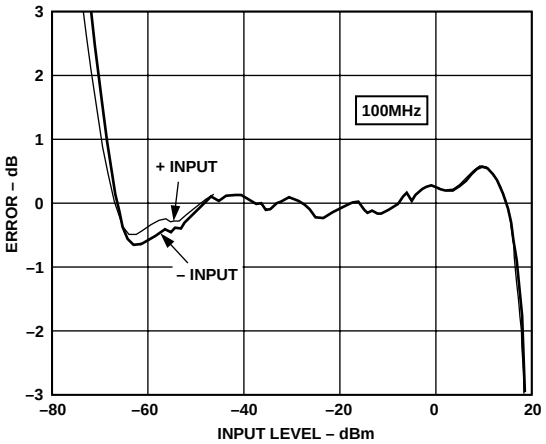


Figure 10. Log Conformance vs. Input Level at 100 MHz; Showing Response to Alternative Inputs

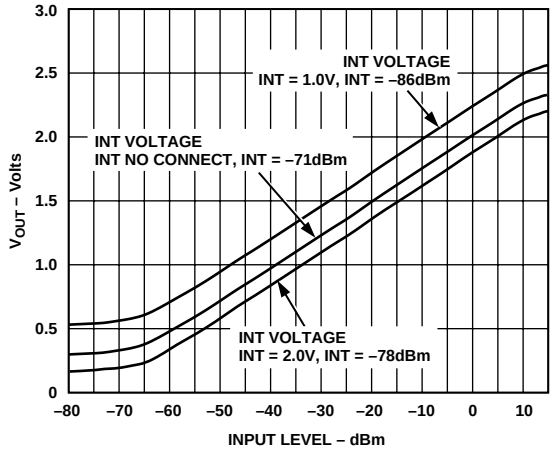


Figure 8. V_{OUT} vs. Input Level at 3 V Supply Using AD820 as Buffer, Gain = +2; Showing Intercept Adjustment

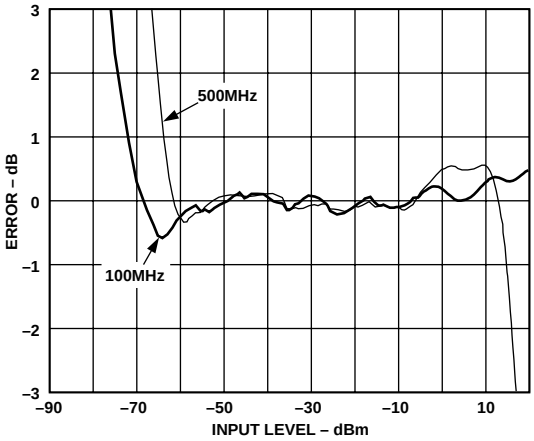


Figure 11. Log Conformance vs. Input at 100 MHz, 500 MHz; Input Driven Differentially Using Transformer

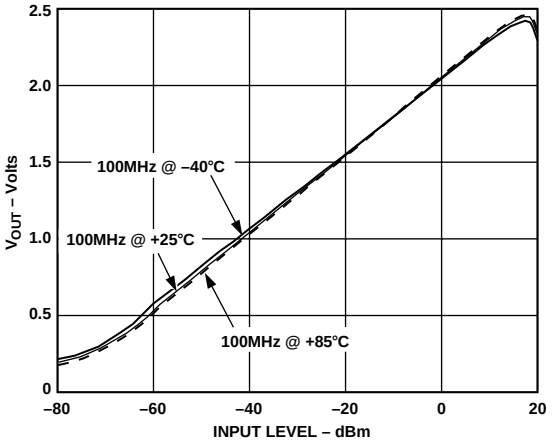


Figure 9. V_{OUT} vs. Input Level at Three Temperatures (–40°C, +25°C, +85°C)

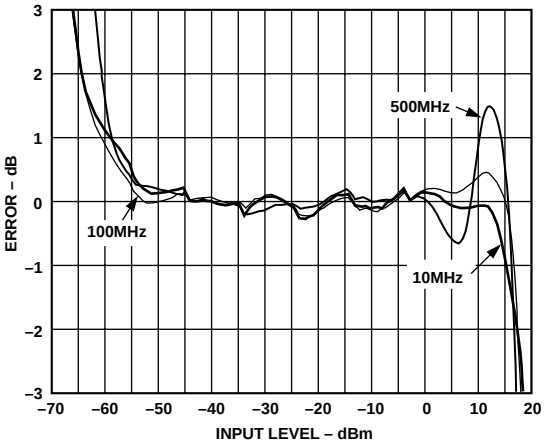


Figure 12. Log Conformance vs. Input Level at 3 V Supply Using AD820 as Buffer, Gain = +2

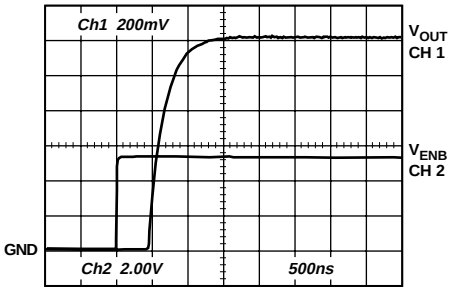


Figure 13. Power-Up Response Time

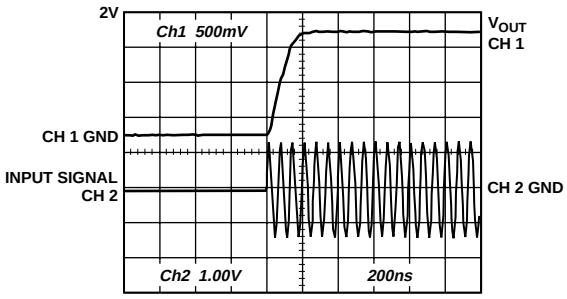


Figure 16. V_{OUT} Rise Time

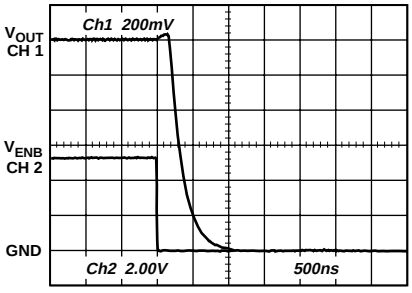


Figure 14. Power-Down Response Time

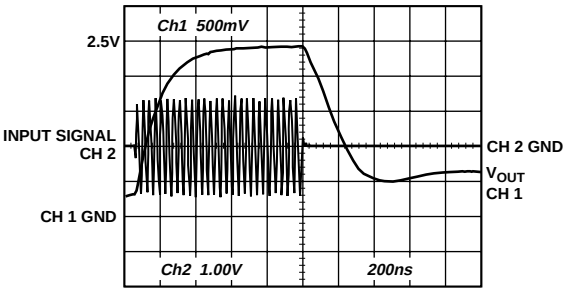


Figure 17. Large Signal Response Time

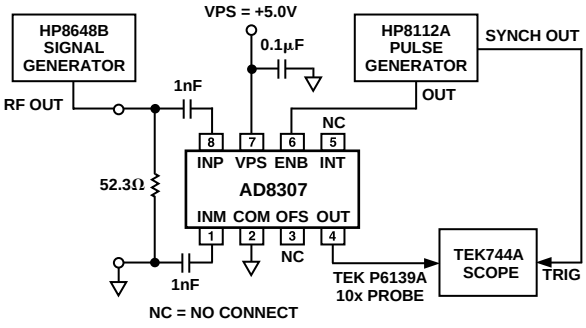


Figure 15. Test Setup For Power-Up/Power-Down Response Time

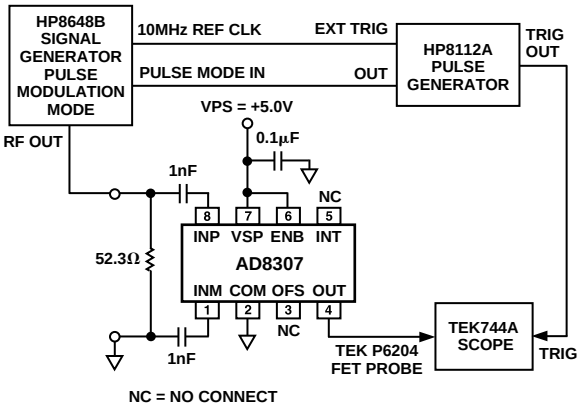


Figure 18. Test Setup For V_{OUT} Pulse Response

LOG AMP THEORY

Logarithmic amplifiers perform a more complex operation than that of classical linear amplifiers, and their circuitry is significantly different. A good grasp of what log amps do, and how they do it, will avoid many pitfalls in their application. The essential purpose of a log amp is not to amplify, though amplification is utilized to achieve the function. Rather, it is to compress a signal of wide dynamic range to its decibel equivalent. It is thus a measurement device. A better term might be logarithmic converter, since its basic function is the conversion of a signal from one domain of representation to another, via a precise nonlinear transformation.

Logarithmic compression leads to situations that may be confusing or paradoxical. For example, a voltage offset added to the output of a log amp is equivalent to a gain increase ahead of its input. In the usual case where all the variables are voltages, and regardless of the particular structure, the relationship between the variables can be expressed as:

$$V_{OUT} = V_Y \log (V_{IN}/V_X) \quad (1)$$

where:

V_{OUT} is the output voltage,

V_Y is called the slope voltage; the logarithm is usually taken to base-ten (in which case V_Y is also the volts-per-decade),

V_{IN} is the input voltage,

and

V_X is called the intercept voltage.

All log amps implicitly require two references, here V_X and V_Y, which determine the scaling of the circuit. The absolute accuracy of a log amp cannot be any better than the accuracy of its scaling references. Equation 1 is mathematically incomplete in representing the behavior of a demodulating log amp such as the AD8307, where V_{IN} has an alternating sign. However, the basic principles are unaffected, and we can safely use this as our starting point in the analyses of log amp scaling which follow.

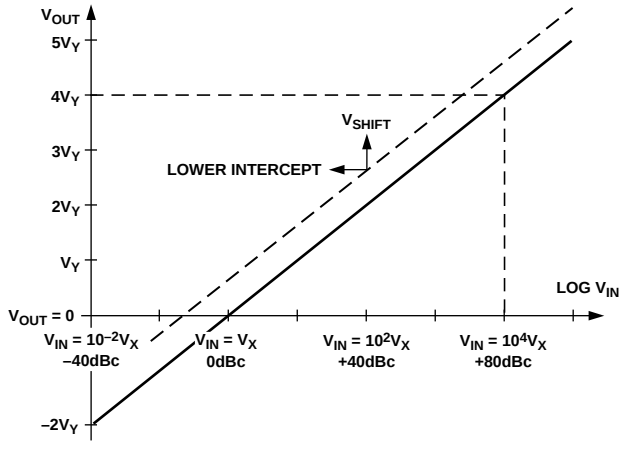


Figure 19. Ideal Log Amp Function

Figure 19 shows the input/output relationship of an ideal log amp, conforming to Equation 1. The horizontal scale is logarithmic and spans a wide dynamic range, shown here as over 120 dB, or six decades. The output passes through zero (the log-intercept) at the unique value $V_{IN} = V_X$ and would ideally become negative for inputs below the intercept. In the ideal case, the straight line describing V_{OUT} for all values of V_{IN} would continue indefinitely in both directions. The dotted line shows that the effect of adding an offset voltage V_{SHIFT} to the output is to lower the effective intercept voltage V_X. Exactly the same alteration could be achieved raising the gain (or signal level) ahead of the log amp by the factor V_{SHIFT}/V_Y. For example, if V_Y is 500 mV per decade (that is, 25 mV/dB, as for the AD8307), an offset of +150 mV added to the output will appear to lower the intercept by two tenths of a decade, or 6 dB. Adding an offset to the output is thus indistinguishable from applying an input level that is 6 dB higher.

The log amp function described by Equation 1 differs from that of a linear amplifier in that the incremental gain $\partial V_{OUT}/\partial V_{IN}$ is a very strong function of the instantaneous value of V_{IN}, as is apparent by calculating the derivative. For the case where the logarithmic base is e, we have:

$$\frac{\partial V_{OUT}}{\partial V_{IN}} = \frac{V_Y}{V_{IN}} \quad (2)$$

That is, the incremental gain is inversely proportional to the instantaneous value of the input voltage. This remains true for any logarithmic base, which is chosen as 10 for all decibel-related purposes. It follows that a perfect log amp would be required to have infinite gain under classical small-signal (zero-amplitude) conditions. Less ideally, this result indicates that, whatever means are used to implement a log amp, accurate response under small-signal conditions (that is, at the lower end of the dynamic range) demands the provision of a very high gain-bandwidth product. A further consequence of this high gain is that, in the absence of an input signal, even very small amounts of thermal noise at the input of a log amp will cause a finite output for zero input, resulting in the response line curving away from the ideal shown in Figure 19 toward a finite baseline, which can be either above or below the intercept. Note that the value given for this intercept may be an extrapolated value, in which case the output may not cross zero, or even reach it, as is the case for the AD8307.

While Equation 1 is fundamentally correct, a simpler formula is appropriate for specifying the calibration attributes of a log amp like the AD8307, which demodulates a sine wave input:

$$V_{OUT} = V_{SLOPE} (P_{IN} - P_0) \quad (3)$$

where:

V_{OUT} is the demodulated and filtered baseband (video or RSSI) output,

V_{SLOPE} is the logarithmic slope, now expressed in volts/dB (typically between 15 and 30 mV/dB),

P_{IN} is the input power, expressed in decibels relative to some reference power level,

and

P_0 is the logarithmic intercept, expressed in decibels relative to the same reference level.

The most widely used reference in RF systems is decibels above 1 mW in 50 Ω, written dBm. Note that the quantity $(P_{IN} - P_0)$ is just dB. The logarithmic function disappears from the formula because the conversion has already been implicitly performed in stating the input in decibels. This is strictly a concession to popular convention: log amps manifestly do not respond to power (tacitly, power absorbed at the input), but, rather, to input

voltage. The use of dBV (decibels with respect to 1 V rms) would be more precise, though still incomplete, since waveform is involved, too. Since most users think about and specify RF signals in terms of power—even more specifically, in dBm re 50 Ω—we will use this convention in specifying the performance of the AD8307.

Progressive Compression

Most high speed high dynamic range log amps use a cascade of nonlinear amplifier cells (Figure 20) to generate the logarithmic function from a series of contiguous segments, a type of piecewise-linear technique. This basic topology immediately opens up the possibility of enormous gain-bandwidth products. For example, the AD8307 employs six cells in its main signal path, each having a small-signal gain of 14.3 dB (×5.2) and a –3 dB bandwidth of about 900 MHz; the overall gain is about 20,000 (86 dB) and the overall bandwidth of the chain is some 500 MHz, resulting in the incredible gain-bandwidth product (GBW) of 10,000 GHz, about a million times that of a typical op amp. This very high GBW is an essential prerequisite to accurate operation under small-signal conditions and at high frequencies. Equation 2 reminds us, however, that the incremental gain will decrease rapidly as V_{IN} increases. The AD8307 continues to exhibit an essentially logarithmic response down to inputs as small as 50 μV at 500 MHz.

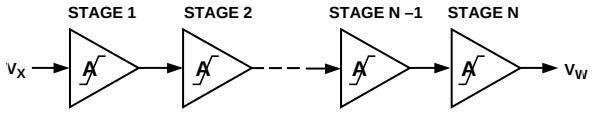


Figure 20. Cascade of Nonlinear Gain Cells

To develop the theory, we will first consider a slightly different scheme to that employed in the AD8307, but which is simpler to explain and mathematically more straightforward to analyze. This approach is based on a nonlinear amplifier unit, which we may call an A/1 cell, having the transfer characteristic shown in Figure 21. The local small-signal gain $\partial V_{OUT}/\partial V_{IN}$ is A, maintained for all inputs up to the knee voltage E_K, above which the incremental gain drops to unity. The function is symmetrical: the same drop in gain occurs for instantaneous values of V_{IN} less than $-E_K$. The large-signal gain has a value of A for inputs in the range $-E_K \le V_{IN} \le +E_K$, but falls asymptotically toward unity for very large inputs. In logarithmic amplifiers based on this amplifier function, both the slope voltage and the intercept voltage must be traceable to the one reference voltage, E_K. Therefore, in this fundamental analysis, the calibration accuracy of the log amp is dependent solely on this voltage. In practice, it is possible to separate the basic references used to determine V_Y and V_X and

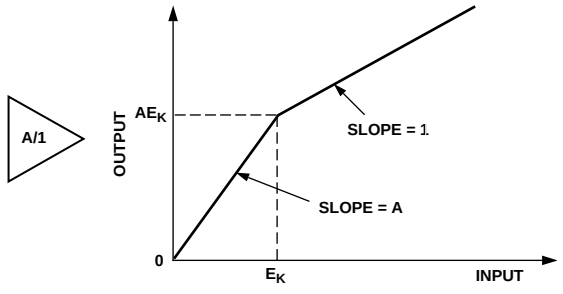


Figure 21. The A/1 Amplifier Function

in the case of the AD8307, V_Y is traceable to an on-chip bandgap reference, while V_X is derived from the thermal voltage kT/q and later temperature-corrected.

Let the input of an N-cell cascade be V_{IN}, and the final output V_{OUT}. For small signals, the overall gain is simply A^N. A six-stage system in which A = 5 (14 dB) has an overall gain of 15,625 (84 dB). The importance of a very high small-signal gain in implementing the logarithmic function has been noted; however, this parameter is of only incidental interest in the design of log amps.

From here onward, rather than considering gain, we will analyze the overall nonlinear behavior of the cascade in response to a simple dc input, corresponding to the V_{IN} of Equation 1. For very small inputs, the output from the first cell is $V_1 = AV_{IN}$; from the second, $V_2 = A^2 V_{IN}$, and so on, up to $V_N = A^N V_{IN}$. At a certain value of V_{IN}, the input to the Nth cell, V_{N-1}, is exactly equal to the knee voltage E_K. Thus, $V_{OUT} = AE_K$ and since there are N–1 cells of gain A ahead of this node, we can calculate that $V_{IN} = E_K/A^{N-1}$. This unique situation corresponds to the lin-log transition, labeled 1 on Figure 22. Below this input, the cascade of gain cells is acting as a simple linear amplifier, while for higher values of V_{IN}, it enters into a series of segments which lie on a logarithmic approximation (dotted line).

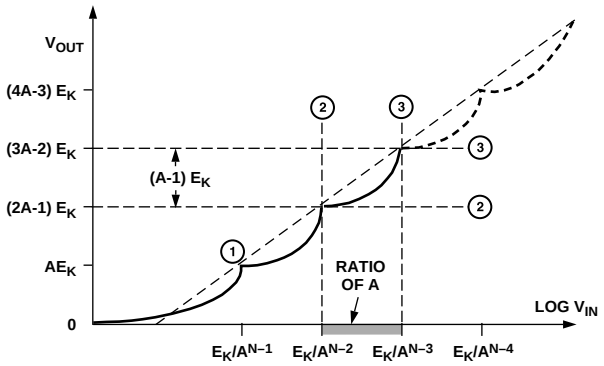


Figure 22. The First Three Transitions

Continuing this analysis, we find that the next transition occurs when the input to the (N–1) stage just reaches E_K; that is, when $V_{IN} = E_K/A^{N-2}$. The output of this stage is then exactly AE_K, and it is easily demonstrated (from the function shown in Figure 21) that the output of the final stage is $(2A–1)\,E_K$ (labeled ② on Figure 22). Thus, the output has changed by an amount $(A–1)E_K$ for a change in V_{IN} from E_K/A^{N-1} to E_K/A^{N-2}, that is, a ratio change of A. At the next critical point, labeled ③, we find the input is again A times larger and V_{OUT} has increased to $(3A–2)E_K$, that is, by another linear increment of $(A–1)E_K$. Further analysis shows that right up to the point where the input to the first cell is above the knee voltage, V_{OUT} changes by $(A–1)E_K$ for a ratio change of A in V_{IN}. This can be expressed as a certain fraction of a decade, which is simply $log_{10}(A)$. For example, when A = 5 a transition in the piecewise linear output function occurs at regular intervals of 0.7 decade (that is, $log_{10}(A)$, or 14 dB divided by 20 dB). This insight allows us to immediately write the Volts per Decade scaling parameter, which is also the Scaling Voltage V_Y, when using base-10 logarithms, as:

$$V_Y = \frac{Linear\ Change\ in\ V_{OUT}}{Decades\ Change\ in\ V_{IN}} = \frac{(A-1)E_K}{\log_{10}(A)} \quad (4)$$

Note that only two design parameters are involved in determining V_Y, namely, the cell gain A and the knee voltage E_K, while N, the number of stages, is unimportant in setting the slope of the overall function. For A = 5 and E_K = 100 mV, the slope would be a rather awkward 572.3 mV per decade (28.6 mV/dB). A well designed log amp will have rational scaling parameters.

The intercept voltage can be determined by using two pairs of transition points on the output function (consider Figure 22). The result is:

$$V_X = \frac{E_K}{A^{\left(N+1/\left(A-1\right)\right)}} \quad (5)$$

For the case under consideration, using N = 6, we calculate V_Z = 4.28 μV. However, we need to be careful about the interpretation of this parameter, since it was earlier defined as the input voltage at which the output passes through zero (see Figure 19). But clearly, in the absence of noise and offsets, the output of the amplifier chain shown in Figure 21 can be zero when, and only when, V_{IN} = 0. This anomaly is due to the finite gain of the cascaded amplifier, which results in a failure to maintain the logarithmic approximation below the lin-log transition (point ① in Figure 22). Closer analysis shows that the voltage given by Equation 5 represents the extrapolated, rather than actual, intercept.

Demodulating Log Amps

Log amps based on a cascade of A/1 cells are useful in baseband applications, because they do not demodulate their input signal. However, baseband and demodulating log amps alike can be made using a different type of amplifier stage, which we will call an A/0 cell. Its function differs from that of the A/1 cell in that the gain above the knee voltage E_K falls to zero, as shown by the solid line in Figure 23. This is also known as the limiter function, and a chain of N such cells is often used to generate a hard-limited output, in recovering the signal in FM and PM modes.

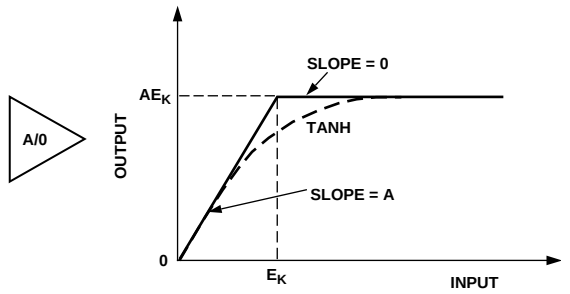


Figure 23. A/0 Amplifier Functions (Ideal and Tanh)

The AD640, AD606, AD608, AD8307 and various other Analog Devices communications products incorporating a logarithmic IF amplifier all use this technique. It will be apparent that the output of the last stage can no longer provide the logarithmic output, since this remains unchanged for all inputs above the limiting threshold, which occurs at $V_{IN} = E_K/A^{N-1}$. Instead, the logarithmic output is now generated by summing the outputs of all the stages. The full analysis for this type of log amp is only slightly more complicated than that of the previous case. It is readily shown that, for practical purpose, the intercept voltage V_X is identical to that given in Equation 5, while the slope voltage is:

$$V_Y = \frac{A\,E_K}{\log_{10}\left(A\right)} \quad (6)$$

Preference for the A/0 style of log amp, over one using A/1 cells, stems from several considerations. The first is that an A/0 cell can be very simple. In the AD8307 it is based on a bipolar-transistor differential pair, having resistive loads R_L and an emitter current source, I_E. This will exhibit an equivalent knee-voltage of E_K = 2 kT/q and a small signal gain of $A = I_E R_L/E_K$. The large signal transfer function is the hyperbolic tangent (see dotted line in Figure 23). This function is very precise, and the deviation from an ideal A/0 form is not detrimental. In fact, the rounded shoulders of the *tanh* function beneficially result in a lower ripple in the logarithmic conformance than that obtained using an ideal A/0 function.

An amplifier built of these cells is entirely differential in structure and can thus be rendered very insensitive to disturbances on the supply lines and, with careful design, to temperature variations. The output of each gain cell has an associated transconductance (g_m) cell, which converts the differential output voltage of the cell to a pair of differential currents, which are summed simply by connecting the outputs of all the g_m (detector) stages in parallel. The total current is then converted back to a voltage by a transresistance stage, to generate the logarithmic output. This scheme is depicted, in single-sided form, in Figure 24.

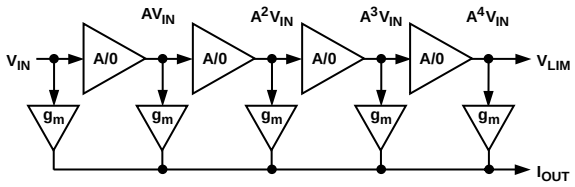


Figure 24. Log Amp Using A/0 Stages and Auxiliary Summing Cells

The chief advantage of this approach is that the slope voltage may now be decoupled from the knee-voltage E_K = 2 kT/q, which is inherently PTAT. By contrast, the simple summation of the cell outputs would result in a very high temperature coefficient of the slope voltage given by Equation 6. To do this, the detector stages are biased with currents (not shown in the Figure) which are rendered stable with temperature. These are derived either from the supply voltage (as in the AD606 and AD608) or from an internal bandgap reference (as in the AD640 and AD8307). This topology affords complete control over the magnitude and temperature behavior of the logarithmic slope, decoupling it completely from E_K.

A further step is yet needed to achieve the demodulation response, required when the log amp is to convert an alternating input into a quasi-dc baseband output. This is achieved by altering the g_m cells used for summation purposes to also implement the rectification function. Early discrete log amps based on the progressive compression technique used half-wave rectifiers. This made post-detection filtering difficult. The AD640 was the first commercial monolithic log amp to use a full-wave rectifier, a practice followed in all subsequent Analog Devices types.

We can model these detectors as being essentially linear g_m cells, but producing an output current independent of the sign of the voltage applied to the input of each cell. That is, they implement the absolute-value function. Since the output from the later A/0 stages closely approximates an amplitude-symmetric square wave for even moderate input levels (most stages of the amplifier chain operate in a limiting mode), the current output from each detector is almost constant over each period of the input. Somewhat earlier detectors stages produce a waveform having only very brief dropouts, while the detectors nearest the input produce a low level almost-sinusoidal waveform at twice the input frequency. These aspects of the detector system result in a signal that is easily filtered, resulting in low residual ripple on the output.

Intercept Calibration

All monolithic log amps from Analog Devices include accurate means to position the intercept voltage V_X (or equivalent power for a demodulating log amp). Using the scheme shown in Figure 24, the basic value of the intercept level departs considerably from that predicted by the simpler analyses given earlier. However, the intrinsic intercept voltage is still proportional to E_K, which is PTAT (Equation 5). Recalling that the addition of an offset to the output produces an effect which is indistinguishable from a change in the position of the intercept, we can cancel the left-right motion of V_X resulting from the temperature variation of E_K by adding an offset having the required temperature behavior.

The precise temperature-shaping of the intercept-positioning offset results in a log amp having stable scaling parameters, making it a true measurement device, for example, as a calibrated Received Signal Strength Indicator (RSSI). In this application, one is more interested in the value of the output for an input waveform which is invariably sinusoidal. The input level may alternatively be stated as an equivalent power, in dBm, but here we must step carefully. It is essential to know the load impedance in which this power is presumed to be measured.

In RF practice, it is generally safe to assume a reference impedance of 50 Ω, in which 0 dBm (1 mW) corresponds to a sinusoidal amplitude of 316.2 mV (223.6 mV rms). The intercept may likewise be specified in dBm. For the AD8307, it is positioned at –84 dBm, corresponding to a sine amplitude of 20 μV. It is important to bear in mind that log amps do not respond to power, but to the voltage applied to their input.

The AD8307 presents a nominal input impedance much higher than 50 Ω (typically 1.1 kΩ at low frequencies). A simple input matching network can considerably improve the sensitivity of this type of log amp. This will increase the voltage applied to the input and thus alter the intercept. For a 50 Ω match, the voltage gain is 4.8 and the whole dynamic range moves down by 13.6 dB (see Figure 33). Note that the effective intercept is a function of waveform. For example, a square-wave input will read 6 dB higher than a sine wave of the same amplitude, and a Gaussian noise input 0.5 dB higher than a sine wave of the same rms value.

Offset Control

In a monolithic log amp, direct-coupling between the stages is used for several reasons. First, this avoids the use of coupling capacitors, which may typically have a chip area equal to that of a basic gain cell, thus considerably increasing die size. Second, the capacitor values predetermine the lowest frequency at which the log amp can operate; for moderate values, this may be as high as 30 MHz, limiting the application range. Third, the parasitic (back-plate) capacitance lowers the bandwidth of the cell, further limiting the applications.

But the very high dc gain of a direct-coupled amplifier raises a practical issue. An offset voltage in the early stages of the chain is indistinguishable from a 'real' signal. If it were as high as, say, 400 μV, it would be 18 dB larger than the smallest ac signal (50 μV), potentially reducing the dynamic range by this amount. This problem is averted by using a global feedback path from the last stage to the first, which corrects this offset in a similar fashion to the dc negative feedback applied around an op amp. The high frequency components of the signal must, of course, be removed, to prevent a reduction of the HF gain in the forward path.

In the AD8307, this is achieved by an on-chip filter, providing sufficient suppression of HF feedback to allow operation above 1 MHz. To extend the range below this frequency, an external capacitor may be added. This permits the high pass corner to be lowered to audio frequencies using a capacitor of modest value. Note that this capacitor has no effect on the minimum signal frequency for input levels above the offset voltage: this extends down to dc (for a signal applied directly to the input pins). The offset voltage will vary from part to part; some will exhibit essentially stable offsets of under 100 μV, without the benefit of an offset adjustment.

Extension of Range

The theoretical dynamic range for the basic log amp shown in Figure 24 is A^N. For A = 5.2 (14.3 dB) and N = 6, it is 20,000 or 86 dB. The actual lower end of the dynamic range is largely determined by the thermal noise floor, measured at the input of the chain of amplifiers. The upper end of the range is extended upward by the addition of top-end detectors. The input signal is applied to a tapped attenuator, and progressively smaller signals are applied to three passive rectifying g_m cells whose outputs are summed with those of the main detectors. With care in design, the extension to the dynamic range can be seamless over the full frequency range. For the AD8307 it amounts to a further 27 dB.

The total dynamic range is thus theoretically 113 dB. The specified range of 90 dB (–74 dBm to +16 dBm) is that for high accuracy, calibrated operation, and includes the low end degradation due to thermal noise, and the top end reduction due to voltage limitations. The additional stages are not, however, redundant, but are needed to maintain accurate logarithmic conformance over the central region of the dynamic range, and in extending the usable range considerably beyond the specified range. In applications where log-conformance is less demanding, the AD8307 can provide over 95 dB of range.

PRODUCT OVERVIEW

The AD8307 comprises six main amplifier/limiter stages, each having a gain of 14.3 dB and small signal bandwidth of 900 MHz; the overall gain is 86 dB with a –3 dB bandwidth of 500 MHz. These six cells, and their associated g_m-styled full-wave detectors, handle the lower two-thirds of the dynamic range. Three top-end detectors, placed at 14.3 dB taps on a passive attenuator, handle the upper third of the 90 dB range. Biasing for these cells is provided by two references: one determines their gain; the other is a bandgap circuit that determines the logarithmic slope and stabilizes it against supply- and temperature-variations. The AD8307 may be enabled/disabled by a CMOS-compatible level at ENB (Pin 6). The first amplifier stage provides a low voltage noise spectral density (1.5 nV/$\sqrt{\text{Hz}}$).

The differential current-mode outputs of the nine detectors are summed and then converted to single-sided form in the output stage, nominally scaled 2 μA/dB. The logarithmic output voltage is developed by applying this current to an on-chip 12.5 kΩ resistor, resulting in a logarithmic slope of 25 mV/dB (i.e., 500 mV/decade) at OUT. This voltage is not buffered, allowing the use of a variety of special output interfaces, including the addition of post-demodulation filtering. The last detector stage includes a modification to temperature-stabilize the log intercept, which is accurately positioned to make optimal use of the full output voltage range available. The intercept may be adjusted using the pin INT, which adds or subtracts a small current to the signal current.

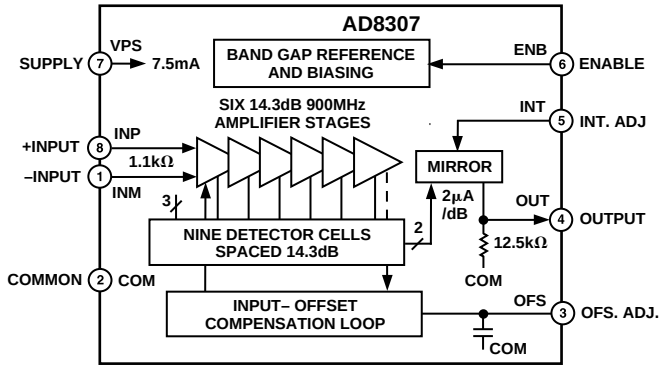


Figure 25. Main Features of the AD8307

The last gain stage also includes an offset-sensing cell. This generates a bipolarity output current when the main signal path has an imbalance due to accumulated dc offsets. This current is integrated by an on-chip capacitor (which may be increased in value by an off-chip component, at OFS). The resulting voltage is used to null the offset at the output of the first stage. Since it does not involve the signal input connections, whose ac coupling capacitors otherwise introduce a second pole in the feedback path, the stability of the offset correction loop is assured.

The AD8307 is built on an advanced dielectrically-isolated complementary bipolar process. Most resistors are thin-film types having a low temperature coefficient of resistance (TCR) and high linearity under large signal conditions. Their absolute tolerance will typically be within ±20%. Similarly, the capacitors have a typical tolerance of ±15% and essentially zero temperature or voltage sensitivity. Most interfaces have additional small junction capacitances associated with them, due to active devices or ESD protection; these may be neither accurate nor stable. Component numbering in each of these interface diagrams is local.

Enable Interface

The chip-enable interface is shown in Figure 26. The currents in the diode-connected transistors control the turn-on and turn-off states of the bandgap reference and the bias generator, and are a maximum of 100 μA when Pin 6 is taken to 5 V, under worst case conditions. Left unconnected, or at a voltage below 1 V, the AD8307 will be disabled and consume a sleep current of under 50 μA; tied to the supply, or a voltage above 2 V, it will be fully enabled. The internal bias circuitry is very fast (typically <100 ns for either OFF or ON), and in practice the latency period before the log amp exhibits its full dynamic range is more likely to be limited by factors relating to the use of ac coupling at the input or the settling of the offset-control loop (see following sections).

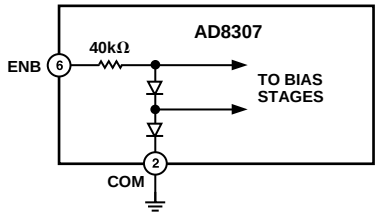


Figure 26. Enable Interface

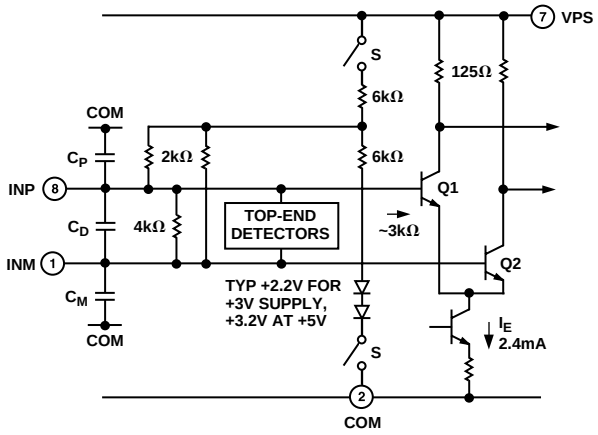


Figure 27. Signal Input Interface

Input Interface

Figure 27 shows the essentials of the signal input interface. C_P and C_M are the parasitic capacitances to ground; C_D is the differential input capacitance, mostly due to Q1 and Q2. In most applications both input pins are ac-coupled. The switches S close when Enable is asserted. When disabled, the inputs float, bias current I_E is shut off, and the coupling capacitors remain charged. If the log amp is disabled for long periods, small leakage currents will discharge these capacitors. If they are poorly matched, charging currents at power-up can generate a transient input voltage which may block the lower reaches of the dynamic range until it has become much less than the signal.

In most applications, the signal will be single-sided, and may be applied to either Pin 1 or Pin 8, with the other pin ac-coupled to ground. Under these conditions, the largest input signal that can be handled by the AD8307 is +10 dBm (sine amplitude of ±1 V) when operating from a 3 V supply; a +16 dBm may be handled using a 5 V supply. The full 16 dBm may be achieved for supplies down to 2.7 V, using a fully balanced drive. For frequencies above about 10 MHz, this is most easily achieved using a matching network (see below). Using such a network, having an inductor at the input, the input transient noted above is eliminated. Occasionally, it may be desirable to use the dc-coupled potential of the AD8307. The main challenge here is to present signals to the log amp at the elevated common-mode input level, requiring the use of low noise, low offset buffer amplifiers. Using dual supplies of ±3 V, the input pins may operate at ground potential.

Offset Interface

The input-referred dc offsets in the signal path are nulled via the interface associated with Pin 3, shown in Figure 28. Q1 and Q2 are the first stage input transistors, with their corresponding load resistors (125 Ω). Q3 and Q4 generate small currents, which can introduce a dc offset into the signal path. When the voltage on OFS is at about 1.5 V, these currents are equal, and nominally 16 μA. When OFS is taken to ground, Q4 is off and the effect of the current in Q3 is to generate an offset voltage of 16 μA × 125 Ω = 2 mV. Since the first stage gain is ×5, this is equivalent to a input offset (INP to INM) of 400 μV. When OFS is taken to its most positive value, the input-referred offset is reversed, to –400 μV. If true dc-coupling is needed, down to very small inputs, this automatic loop must be disabled, and the residual offset eliminated using a manual adjustment, as explained in the next section.

In normal operation, however, using an ac-coupled input signal, the OFS pin should be left open. Any residual input-offset voltage is then automatically nulled by the action of the feedback loop. The g_m cell, which is gated off when the chip is disabled, converts any output offset (sensed at a point near the end of the cascade of amplifiers) to a current. This is integrated by the on-chip capacitor C_{HP}, plus any added external capacitance C_{OFS}, so as to generate an error voltage, which is applied back to the input stage in the polarity needed to null the output offset. From a small-signal perspective, this feedback alters the response of the amplifier, which, rather than behaving as a fully dc-coupled system, now exhibits a zero in its ac transfer function, resulting in a closed-loop high-pass corner at about 700 kHz.

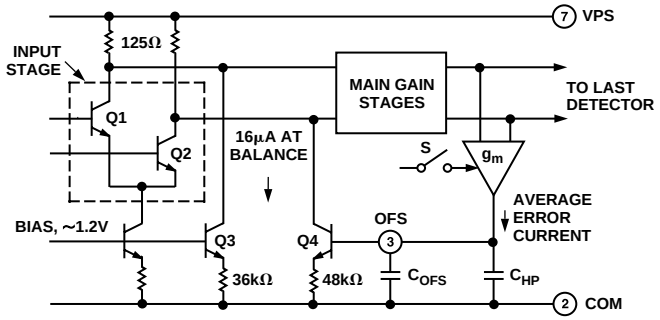


Figure 28. Offset Interface and Offset-Nulling Path

The offset feedback is limited to a range ±400 μV; signals larger than this override the offset control loop, which only impacts performance for very small inputs. An external capacitor reduces the high pass corner to arbitrarily low frequencies; using 1 μF this corner is below 10 Hz. All ADI log amps use an offset-nulling loop; the AD8307 differs in using this single-sided form.

Output Interface

The outputs from the nine detectors are differential currents, having an average value that is dependent on the signal input level, plus a fluctuation at twice the input frequency. The currents are summed at nodes LGP and LGN in Figure 29. Further currents are added at these nodes, to position the intercept, by slightly raising the output for zero input, and to provide temperature compensation. Since the AD8307 is not laser-trimmed, there is a small uncertainty in both the log slope and the log intercept. These scaling parameters may be adjusted (see below).

For zero-signal conditions, all the detector output currents are equal. For a finite input, of either polarity, their difference is converted by the output interface to a single-sided unipolar current nominally scaled 2 μA/dB (40 μA/decade), at the output pin OUT. An on-chip 12.5 kΩ resistor, R1, converts this current to a voltage of 25 mV/dB. C1 and C2 are effectively in shunt with R1 and form a low-pass filter pole, with a corner frequency of about 5 MHz. The pulse response settles to within 1% of the final value within 300 ns. This integral low-pass filter provides adequate smoothing in many IF applications. At 10.7 MHz, the 2f ripple is 12.5 mV in amplitude, equivalent to ±0.5 dB, and only 0.5 mV (±0.02 dB) at f = 50 MHz. A filter capacitor C_{FLT} added from OUT to ground will lower this corner frequency. Using 1 μF, the ripple is maintained to less than ±0.5 dB down to input frequencies of 100 Hz. Note that C_{OFS} (above) should also be increased in low frequency applications, and will typically be made equal to C_{FLT}.

It may be desirable to increase the speed of the output response, with the penalty of increased ripple. One way to do this is simply by connecting a shunt load resistor from OUT to ground, which raises the low pass corner frequency. This also alters the logarithmic slope, for example to 7.5 mV/dB using a 5.36 kΩ resistor, while reducing the 10%-90% rise time to 25 ns. The ripple amplitude for 50 MHz input remains 0.5 mV, but this is now equivalent to ±0.07 dB. If a negative supply is available, the output pin may be connected directly to the summing node of an external op amp connected as an inverting-mode transresistance stage.

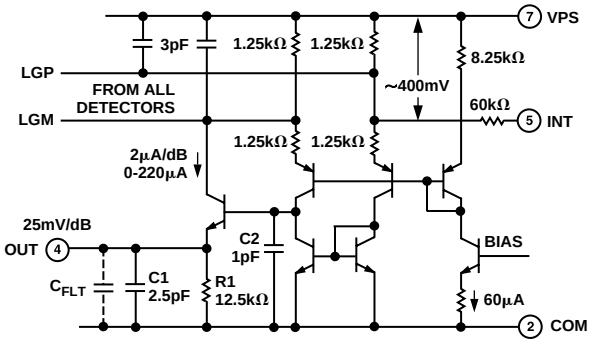


Figure 29. Simplified Output Interface

USING THE AD8307

The AD8307 has very high gain and a bandwidth from dc to over 1 GHz, at which frequency the gain of the main path is still over 60 dB. Consequently, it is susceptible to all signals within this very broad frequency range that find their way to the input terminals. It is important to remember that these are quite indistinguishable from the "wanted" signal, and will have the effect of raising the apparent noise floor (that is, lowering the useful dynamic range). For example, while the signal of interest may be an IF of 50 MHz, any of the following could easily be larger than the IF signal at the lower extremities of its dynamic range: 60 Hz hum, picked up due to poor grounding techniques; spurious coupling from a digital clock source on the same PC board; local radio stations; etc.

Careful shielding is essential. A ground plane should be used to provide a low impedance connection to the common pin COM, for the decoupling capacitor(s) used at VPS, and as the output ground. It is inadvisable to assume that the ground plane is an equipotential, however, and neither of the inputs should be ac-coupled directly to the ground plane, but kept separate from it, being returned instead to the low associated with the source. This may mean isolating the low side of an input connector with a small resistance to the ground plane.

Basic Connections

Figure 30 shows the simple connections suitable for many applications. The inputs are ac-coupled by C1 and C2, which should have the same value, say, C_C. The coupling time-constant is R_{IN} $C_C/2$, thus forming a high pass corner with a 3 dB attenuation at $f_{HP} = 1/(p\ R_{IN}\ C_C)$. In high frequency applications, f_{HP} should be as large as possible, in order to minimize the coupling of unwanted low frequency signals. Conversely, in low frequency applications, a simple RC network forming a low-pass filter should be added at the input for the same reason. For the case where the generator is not terminated, the signal range should be expressed in terms of the voltage response, and extends from –85 dBV to +6 dBV.

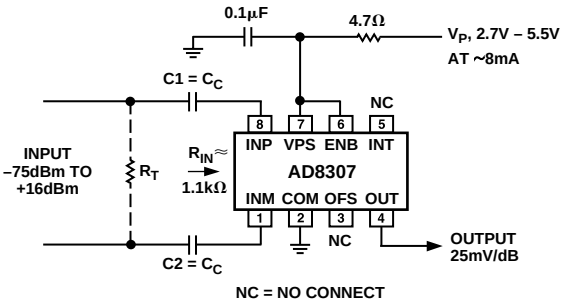


Figure 30. Basic Connections

Where it is necessary to terminate the source at a low impedance, the resistor R_T should be added, with allowance for the shunting effect of the basic 1.1 kΩ input resistance (R_{IN}) of the AD8307. For example, to terminate a 50 Ω source a 52.3 Ω 1% tolerance resistor should be used. This may be placed on the input side or the log-amp side of the coupling capacitors; in the former case, smaller capacitors can be used for a given frequency range; in the latter case, the effective R_{IN} is lowered directly at the log-amp inputs.

Figure 31 shows the output versus the input level, in dBm when driven from a terminated 50 Ω generator, for sine inputs at 10 MHz, 100 MHz and 500 MHz; Figure 32 shows the typical logarithmic conformance under the same conditions. Note that +10 dBm corresponds to a sine amplitude of 1 V, equivalent to an rms power of 10 mW in a 50 Ω termination. But if the termination resistor is omitted, the input power is negligible. The use of dBm to define input level therefore needs to be considered carefully in connection with the AD8307.

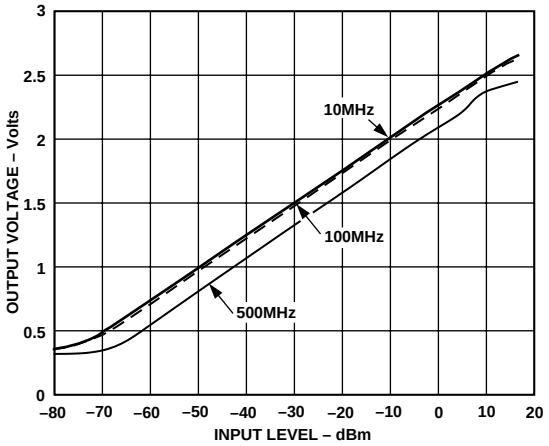


Figure 31. Log Response at 10 MHz, 100 MHz and 500 MHz

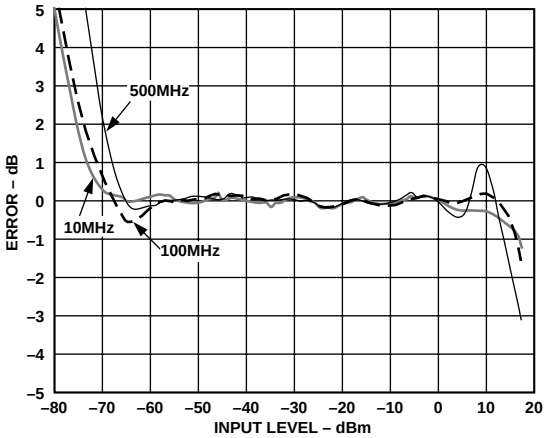


Figure 32. Logarithmic Law Conformance at 10 MHz, 100 MHz and 500 MHz

Input Matching

Where higher sensitivity is required, an input matching network is valuable. Using a transformer to achieve the impedance transformation also eliminates the need for coupling capacitors, lowers the offset voltage generated directly at the input, and balances the drives to INP and INM. The choice of turns ratio will depend somewhat on the frequency. At frequencies below 50 MHz, the reactance of the input capacitance is much higher than the real part of the input impedance. In this frequency range, a turns ratio of about 1:4.8 will lower the input impedance to 50 Ω while raising the input voltage, and thus lowering the effect of the short circuit noise voltage by the same factor. There will be a small contribution from the input noise current, so the total noise will be reduced by a somewhat smaller factor. The intercept will also be lowered by the turns ratio; for a 50 Ω match, it will be reduced by 20 log_{10} (4.8) or 13.6 dB.

Narrow-Band Matching

Transformer coupling is useful in broadband applications. However, a magnetically-coupled transformer may not be convenient in some situations. At high frequencies, it is often preferable to use a narrow-band matching network, as shown in Figure 33. This has several advantages. The same voltage gain is achieved, providing increased sensitivity, but now a measure of selectively is also introduced. The component count is low: two capacitors and an inexpensive chip inductor. Further, by making these capacitors unequal the amplitudes at INP and INM may be equalized when driving from a single-sided source; that is, the network also serves as a balun. Figure 34 shows the response for a center frequency of 100 MHz; note the very high attenuation at low frequencies. The high-frequency attenuation is due to the input capacitance of the log amp.

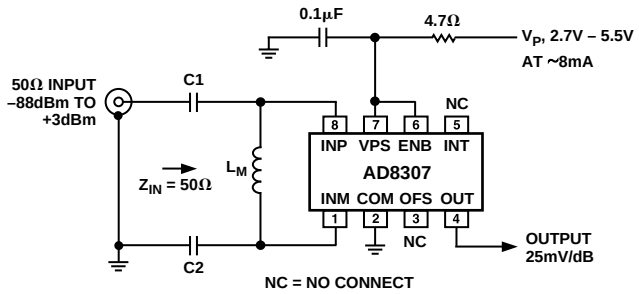


Figure 33. High Frequency Input Matching Network

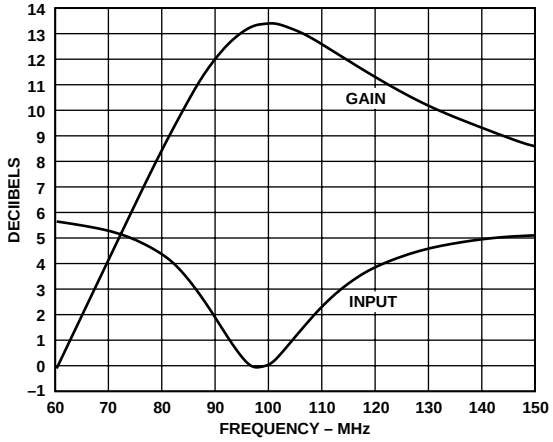


Figure 34. Response of 100 MHz Matching Network

Table I provides solutions for a variety of center frequencies F_C and matching impedances Z_{IN} of nominally 50 Ω and 100 Ω. The unequal capacitor values were chosen to provide a well-balanced differential drive, and also to allow better centering of the frequency response peak when using standard value components; this generally results in a Z_{IN} that is not exact. The full AD8307 HF input impedance and the inductor losses were included in the modeling.

Table I. Narrow-Band Matching Values

F_C MHz	Z_{IN} Ω	C1 pF	C2 pF	L_M nH	Voltage Gain (dB)
10	45	160	150	3300	13.3
20	44	82	75	1600	13.4
50	46	30	27	680	13.4
100	50	15	13	330	13.4
150	57	10	8.2	220	13.2
200	57	7.5	6.8	150	12.8
250	50	6.2	5.6	100	12.3
500	54	3.9	3.3	39	10.9
10	103	100	91	5600	10.4
20	102	51	43	2700	10.4
50	99	22	18	1000	10.6
100	98	11	9.1	430	10.5
150	101	7.5	6.2	260	10.3
200	95	5.6	4.7	180	10.3
250	92	4.3	3.9	130	9.9
500	114	2.2	2.0	47	6.8

Slope and Intercept Adjustments

Where higher calibration accuracy is needed, the adjustments shown in Figure 35 can be used, either singly or in combination. The log slope is lowered to 20 mV/dB by shunting the nominally 12.5 kΩ on-chip load resistor (see Figure 29) with 50 kΩ, adjusted by VR1. The calibration range is ±10% (18 mV/dB to 22 mV/dB), including full allowance for the variability in the value of the internal load. The adjustment may be made by alternately applying two input levels, provided by an accurate signal generator, spaced over the central portion of the log amp's dynamic range, for example –60 dBm and 0 dBm. An AM-modulated signal, at the center of the dynamic range, can also be used. For a modulation depth M, expressed as a fraction, the decibel range between the peaks and troughs over one cycle of the modulation period is given by:

$$\Delta\, dB = 20 \log_{10} \frac{1+M}{1-M} \qquad (7)$$

For example, using an rms signal level of –40 dBm with a 70% modulation depth (M = 0.7), the decibel range is 15 dB, as the signal varies from –47.5 dBm to –32.5 dBm.

The log intercept is adjustable over a ±3 dB range, which is sufficient to absorb the worst-case intercept error in the AD8307 plus some system-level errors. For greater range, set R_S to zero. VR2 is adjusted while applying an accurately known CW signal near the lower end of the dynamic range, in order to minimize the effect of any residual uncertainty in the slope. For example, to position the intercept to –80 dBm, a test level of –65 dBm may be applied and VR2 adjusted to produce a dc output of 15 dB above zero at 25 mV/dB, which is +0.3 V.

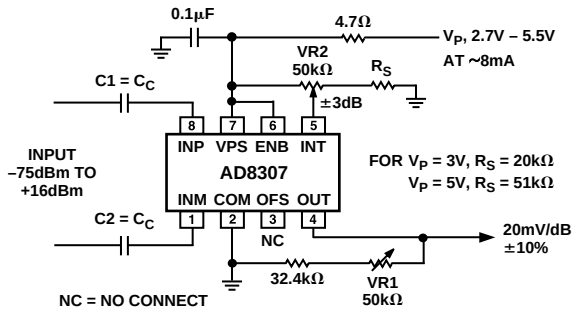


Figure 35. Slope and Intercept Adjustments

APPLICATIONS

The AD8307 is a highly versatile and easily applied log amp requiring very few external components. Most applications of this product can be accommodated using the simple connections shown in the preceding section. A few examples of more specialized applications are provided here.

Buffered Output

The output may be buffered, and the slope optionally increased, using an op amp. If the single-supply capability is to be preserved, a suitable component is the AD8031. Like the AD8307, it is capable of operating from a 2.7 V supply and features a rail-to-rail output capability; it is available in a 5-pin version and in dual form as the 8-pin AD8032. Figure 36 shows how the slope may be increased to 50 mV/dB (1 V per decade), requiring a 5 V supply (90 dB times 50 mV is a 4.5 V swing). VR1 provides a ±10% slope adjustment; VR2 provides a ±3 dB intercept range. With R2 = 4.99 kΩ, the slope is adjustable to 25 mV/dB, allowing the use of a 2.7 V supply. Setting R2 to 80.6 kΩ, it is raised to 100 mV/dB, providing direct reading in decibels on a digital voltmeter. Since a 90 dB range now corresponds to a 9 V swing, a supply of at least this amount is needed for the op amp.

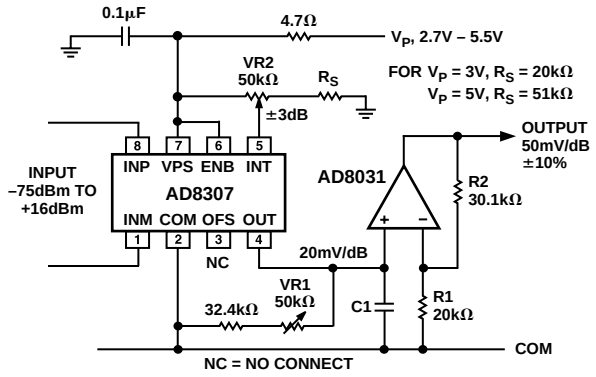


Figure 36. Log Amp with Buffered Output

C1 is optional; it lowers the corner frequency of the low-pass output filter. A value of 0.1 µF should be used for applications in which the output is measured on a voltmeter or other low speed device. On the other hand, when C1 is omitted the 10%-90% response time is under 200 ns, and is typically 300 ns to 99% of final value. To achieve faster response times, it is necessary to lower the load resistance at the output of the AD8307, then restore the scale using a higher gain in the op amp. Using 8.33 kΩ, the basic slope is 10 mV/dB; this can be restored to 25 mV/dB using a buffer gain of 2.5. The overall 10%-90% response time is under 100 ns. Figure 37 shows how the output current capability can be augmented to drive a 50 Ω load; R_T optionally provides reverse termination, which halves the slope to 12.5 mV/dB.

Four-Pole Filter

In low frequency applications, for example, audio down to 20 Hz, it is useful to employ the buffer amplifier as a multipole low-pass filter, in order to achieve low output ripple while maintaining a rapid response time to changes in signal level.

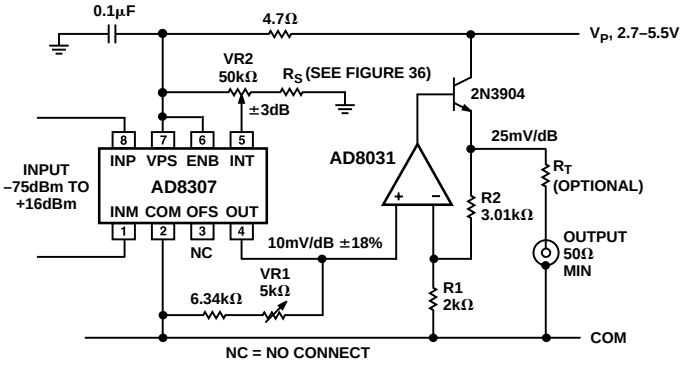


Figure 37. Cable-Driving Log Amp

In Figure 38, the capacitor values were chosen for operation in the audio field, providing a corner frequency of 10 Hz, an attenuation of 80 dB/decade above this frequency, and a 1% settling time of 150 ms (0.1% in 175 ms). The residual ripple is 4 mV (±0.02 dB) when the input to the AD8307 is at 20 Hz. This filter may easily be adapted to other frequencies, by proportional scaling of C5–C7 (e.g., for 100 kHz use 100 pF). Placed ahead of a digital multimeter, the convenient slope scaling of 100 mV/dB requires only a repositioning of the decimal point to read directly in decibels. The supply voltage for the filter must be large enough to support the dynamic range; a minimum of 9 V is needed for most applications; 12 V is recommended.

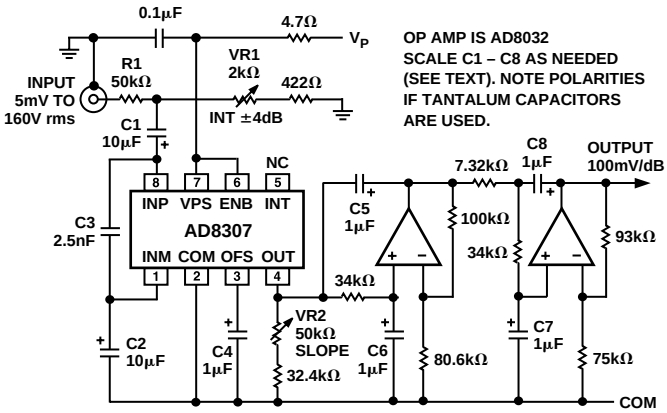


Figure 38. Log Amp with Four-Pole Low-Pass Filter

Figure 38 also shows the use of an input attenuator which may optionally be employed here, or in any other of these applications, to produce a useful wide-range ac voltmeter with direct-decibel scaling. The basic range of –73 dBm to +17 dBm (that is, 50 µV rms to 1.6 V rms, for sine excitations) is shifted, for illustrative purposes, to 5 mV to 160 V rms (at which point the power in R1 is 512 mW). Because the basic input resistance of the AD8307 is not precise, VR1 is used to center the signal range at its input, doubling as a ±4 dB intercept adjustment. The low frequency response extends to 15 Hz; a higher corner frequency can be selected as needed, by scaling C1 and C2. The shunt capacitor C3 is used to lower the high frequency bandwidth to about 100 kHz, and thus lower the susceptibility to spurious signals. Other values should be chosen as needed for the coupling and filter capacitors.

1 μW to 1 kW 50 Ω Power Meter

The front-end adaptation shown in Figure 39 provides the measurement of power being delivered from a transmitter final amplifier to an antenna. The range has been set to cover the power range –30 dBm (7.07 mV rms, or 1 μW) to +60 dBm (223 V rms, or 1 kW). A nominal voltage attenuation ratio of 158:1 (44 dB) is used; thus the intercept is moved from –84 dBm to –40 dBm and the AD8307, scaled 0.25 V/decade of power, will now read 1.5 V for a power level of 100 mW, 2.0 V at 10 W and 2.5 V at 1 kW.

The general expression is:

$$P\,(dBm) = 40\,(V_{OUT} - 1)$$

The required attenuation could be implemented using a capacitive divider, providing a very low input capacitance, but it is difficult to ensure accurate values of small capacitors. A better approach is to use a resistive divider, taking the required precautions to minimize spurious coupling into the AD8307 by placing it in a shielded box, with the input resistor passing through a hole in this box, as indicated in the figure. The coupling capacitors shown here are suitable for f ≥ 10 MHz. A capacitor may be added across the input pins of the AD8307 to reduce the response to spurious HF signals which, as already noted, extends to over 1 GHz.

The mismatch caused by the loading of this resistor will be trivial; only 0.05% of the power delivered to the load will be absorbed by the measurement system, a maximum of 500 mW at 1 kW. The post-demodulation filtering and slope-calibration arrangements should be chosen from other applications described here, to meet the particular system requirements. The 1 nF capacitor lowers the risk of HF signals entering the AD8307 via the load.

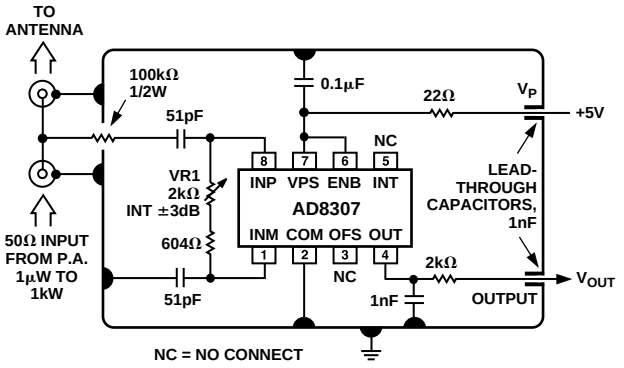


Figure 39. 1 μW to 1 kW 50-Ω Power Meter

Measurement System with 120 dB Dynamic Range

The dynamic range of the AD8307 can be extended further—from 90 dB to over 120 dB—by the addition of an X-AMP™ such as the AD603. This type of variable gain amplifier exhibits a very exact exponential gain control characteristic, which is another way of stating that the gain varies by a constant number of decibels for a given change in the control voltage. For the AD603, this scaling factor is 40 dB/V, or 25 mV/dB. It will be apparent that this property of a linear-in-dB response is characteristic of log amps; indeed, the AD8307 exhibits the same scaling factor.

The AD603 has a very low input referred noise: 1.3 nV/√Hz at its 100-Ω input, or 0.9 nV/√Hz when matched to 50 Ω, equivalent to 0.4 μV rms, or –115 dBm, in a 200 kHz bandwidth. It is also capable of handling inputs in excess of 1.4 V rms, or +16 dBm. It is thus able to cope with a dynamic range of over 130 dB in this particular bandwidth.

Now, if the gain control voltage for the X-AMP is derived from the output of the AD8307, the effect will be to raise the gain of this front-end stage when the signal is small and lower it when it is large, but without altering the fundamental logarithmic nature of the response. This gain range is 40 dB, which, combined with the 90 dB range of the AD8307, again corresponds to a 130 dB range.

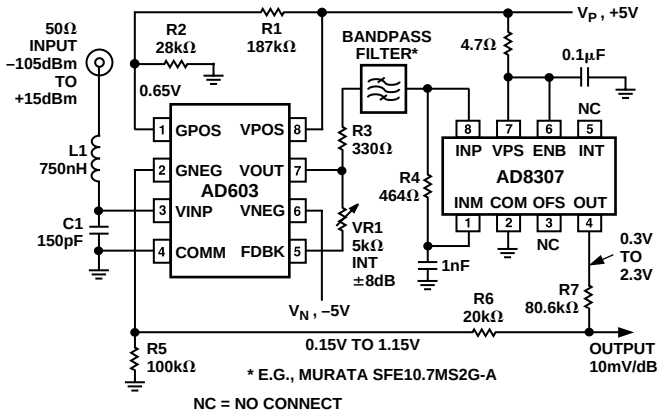


Figure 40. 120 dB Measurement System

Figure 40 shows how these two parts can work together to provide state-of-the-art IF measurements in applications such as spectrum/ network analyzers and other high dynamic range instrumentation. To understand the operation, note first that the AD8307 is used to generate an output of about 0.3 V to 2.3 V. This 2 V span is divided by 2 in R5/R6/R7 to provide the 1 V span needed by the AD603 to vary its gain by 40 dB. Note that an increase in the positive voltage applied at GNEG (Pin 2) lowers the gain. This feedback network is tapped to provide a convenient 10 mV/dB scaling at the output node, which may be buffered if necessary.

The center of the voltage range fed back to the AD603 is 650 mV and the ±20 dB gain range is centered by R1/R2. Note that the intercept calibration of this system benefits from the use of a well regulated 5 V supply. To absorb the insertion loss of the filter and center the full dynamic range, the intercept is adjusted by varying the maximum gain of the AD603, using VR1. Figure 41 shows the AD8307 output over the range –120 dBm to +20 dBm and the deviation from an ideal logarithmic response. The dotted line shows the increase in the noise floor that results when the filter is omitted; the decibel difference is about 10log10(50/0.2) or 24 dB, assuming a 50 MHz bandwidth from the AD603. An L-C filter may be used in place of the ceramic filter used in this example.

X-AMP is a trademark of Analog Devices, Inc.

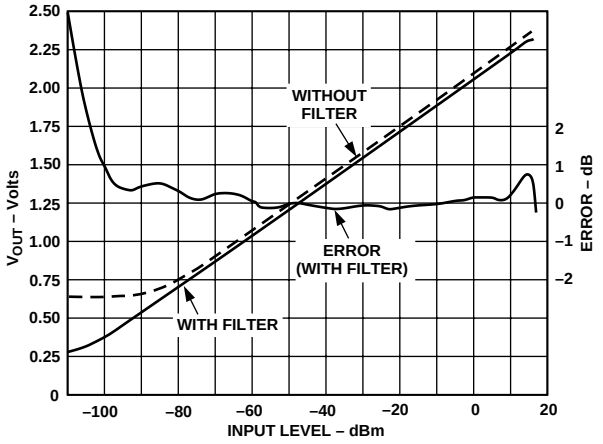


Figure 41. Results for 120 dB Measurement System

Operation at Low Frequencies

The AD8307 provides excellent logarithmic conformance at signal frequencies that may be arbitrarily low, depending only on the values used for the input coupling capacitors. It may also be desirable to add a low-pass input filter in order to desensitize the log amp to HF signals. Figure 42 shows a simple arrangement, providing coupling with an attenuation of 20 dB; the intercept is shifted up by this attenuation, from –84 dBm to –64 dBm, and the input range is now 0.5 mV to 20 V (sine amplitude).

A high pass 3 dB corner frequency of nominally 3 Hz is set by the 10 µF coupling capacitors C1 and C2, which are preferably tantalum electrolytics (note the polarity) and a low pass 3 dB corner frequency of 200 kHz (set by C3 and the effective resistance at the input of 1 kΩ). The –1% amplitude error points occur at 20 Hz and 30 kHz. These are readily altered to suit other applications by simple scaling. When C3 is zero, the low pass corner is at 200 MHz. Note that the lower end of the dynamic range is improved by this capacitor, which provides essentially an HF short circuit at the input, thus significantly lowering the wideband noise; the noise reduction is about 2 dB compared to the case when the AD8307 is driven from a 50 Ω source.

To ensure that the output is free of post-demodulation ripple, it is necessary to lower the low-pass filter time-constant. This is provided by C5; with the value shown, the output time-constant is 125 ms. (See also Figure 38 for a more elaborate filter). Finally, to improve the law-conformance at very low signal levels and at low frequencies, C4 has been added to the offset compensation loop.

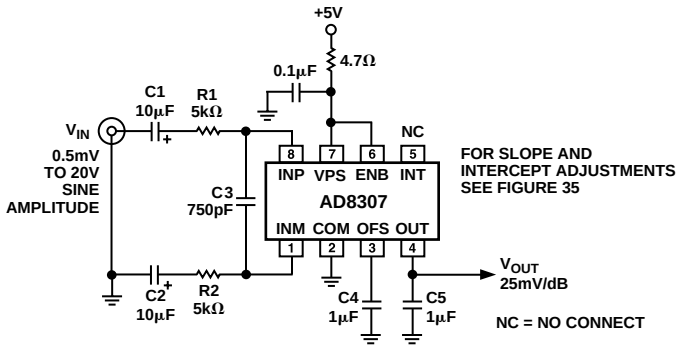


Figure 42. Connections for Low Frequency Operation

DC-Coupled Applications

It may occasionally be necessary to provide response to dc inputs. Since the AD8307 is internally dc-coupled, there is no fundamental reason why this is precluded. However, there is a practical constraint, which is that its inputs must be positioned about 2 V above the COM potential for proper biasing of the first stage. If it happens that the source is a differential signal at this level, it may be directly connected to the input. For example, a microwave detector can be ac-coupled at its RF input and its baseband load then automatically provided by the "floating" R_{IN} and C_{IN} of the AD8307, at about $V_P/2$.

Usually, the source will be a single-sided ground-referenced signal, and it will thus be necessary to provide a negative supply for the AD8307. This can be achieved as shown in Figure 43. The output is now referenced to this negative supply, and it is necessary to provide an output interface that performs a differential-to-single-sided conversion. This is the purpose of the AD830. The slope may be arranged to be 20 mV/dB, when the output ideally runs from zero, for a dc input of 10 µV, to +2.2 V for an input of 4 V. The AD8307 is fundamentally insensitive to the sign of the input signal, but with this biasing scheme, the maximum negative input is constrained to about –1.5 V. The transfer function after trimming and with R7 = 0, is

$$V_{OUT} = (0.4\ V)\ \log_{10}\ (V_{IN}/10\ \mu V)$$

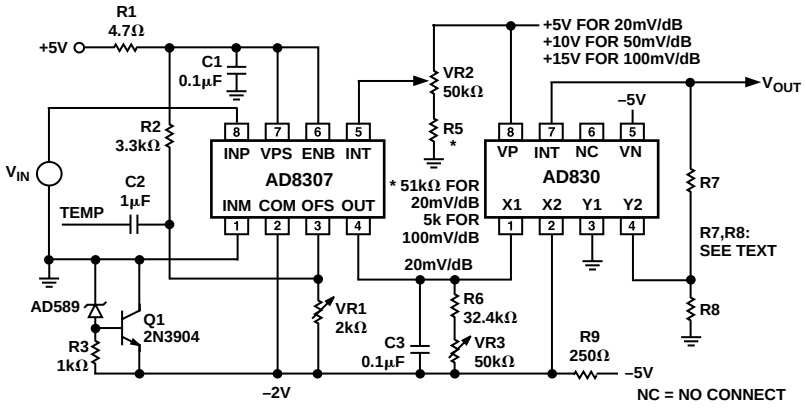


Figure 43. Connections for DC-Coupled Applications

The intercept can be raised, for example, to 100 µV, with the rationale that the dc precision does not warrant operation in the first decade (from 10 µV–100 µV). Likewise, the slope can be raised to 50 mV/dB, using R7 = 3 kΩ, R8 = 2 kΩ, or to 100 mV/dB, to simplify decibel measurements on a DVM, using R7 = 8 kΩ, R8 = 2 kΩ, which raises the maximum output to +11 V, thus requiring a +15 V supply for the AD830. The output may be made to swing in a negative direction by simply reversing Pins 1 and 2. Low-pass filtering capacitor C3 sets the output rise time to about 1 ms.

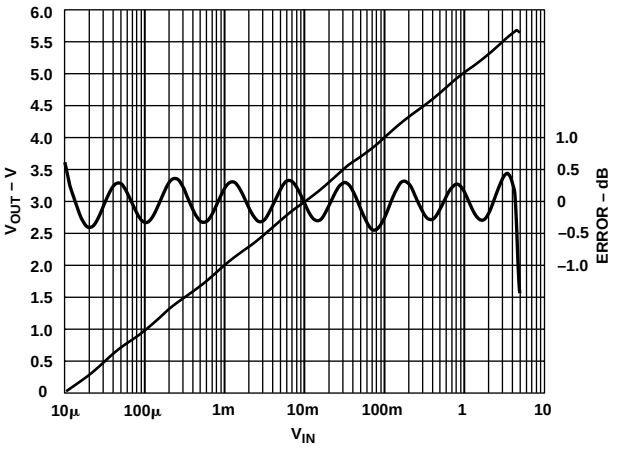


Figure 44. Ideal Output and Law-Conformance Error for the DC-Coupled AD8307 at 50 mV/dB

Figure 44 shows the output and the law-conformance error in the absence of noise and input offset, for the 50 mV/dB option. Note in passing that the error ripple for dc excitation is about twice that for the more usual sinusoidal excitation. In practice, both the noise and the internal offset voltage will degrade the accuracy in the first decade of the dynamic range. The latter is now manually nulled, by VR1, using a simple method that ensures very low residual offsets.

A temporary ac signal, typically a sine wave of 100 mV in amplitude at a frequency of about 100 Hz, is applied via the capacitor at node TEMP; this has the effect of disturbing the offset-nulling voltage. The output voltage is then viewed on an oscilloscope and VR1 is adjusted until the peaks of the (frequency-doubled) waveform are exactly equal in amplitude. This procedure can provide an input null down to about 10 µV; the temperature drift is very low, though not specified since the AD8307 is not principally designed to operate as a baseband log amp, and in ac modes this offset is continuously and automatically nulled.

Next, it is necessary to set the intercept. This is the purpose of VR2, which should be adjusted *after* VR1. The simplest method is to short the input and adjust VR2 for an output of 0.3 V, corresponding to the noise floor. For more exacting applications, a temporary sinusoidal test voltage of 1 mV in amplitude, at about 1 MHz, should be applied, which may require the use of a temporary onboard input attenuator. For 20 mV/dB scaling, a 10 µV dc intercept (which is 6 dB below the ac intercept) requires adjusting the output to 0.68 V; for the 100 mV/dB scaling, this becomes 3.4 V. If a 100 µV intercept is preferred (usefully lowering the maximum output voltage), these become 0.28 V and 1.4 V respectively.

Finally, the slope must be adjusted. This can be performed by applying a low frequency square wave to the main input, having precisely determined upper and lower voltage levels, provided by a programmable waveform generator. A suitable choice is a 100 Hz square wave with levels of 10 mV and 1 V. The output will be a low-pass filtered square wave, and its amplitude should be 0.8 V, for 20 mV/dB scaling, or 4 V for 100 mV/dB scaling.

Operation Above 500 MHz

The AD8307 is not intended for use above 500 MHz. However, it does provide useful performance at higher frequencies. Figure 45 shows a plot of the logarithmic output of the AD8307 for an input frequency of 900 MHz. The device shows good logarithmic conformance from –50 dBm to –10 dBm. There is a "bump" in the transfer function at –5 dBm, but if this is acceptable, the device is usable over a 60 dB dynamic range (–50 dBm to +10 dBm).

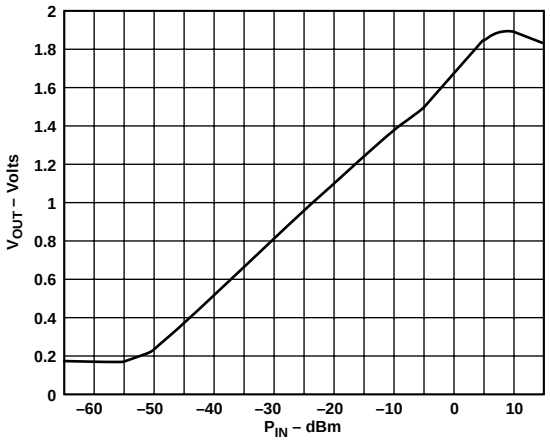


Figure 45. Output vs. Input Level for a 900 MHz Input Signal

Evaluation Board

An evaluation board, carefully laid out and tested to demonstrate the specified high speed performance of the AD8307 is available. Figure 46 shows the schematic of the evaluation board. For ordering information, please refer to the Ordering Guide.

Figures 47 and 49 show the component-side and solder-side silkscreens of the evaluation board. The component-side and solder-side layouts are shown in Figures 48 and 50.

For connection to external instruments, side-launched SMA type connectors are provided. Space is also provided on the board for the installation of SMB or SMC type connectors. When using the top-mount SMA connector, it is recommended that the stripline on the outside 1/8" of the board edge be removed (i.e., scraped using a blade) as this unused stripline acts as an open stub, which could degrade the overall performance of the evaluation board/device combination at high frequencies.

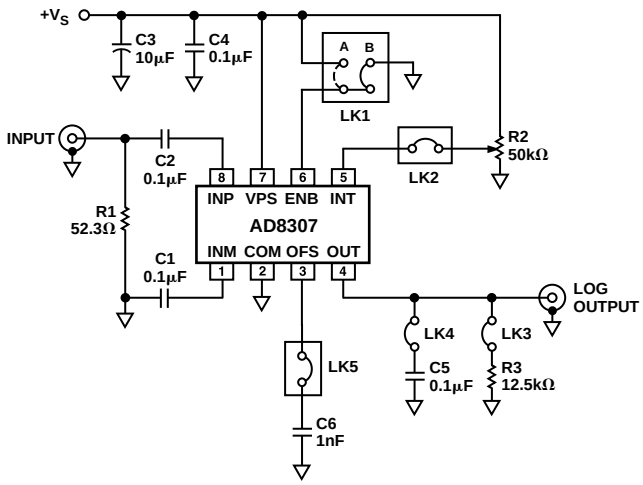


Figure 46. Evaluation Board Schematic

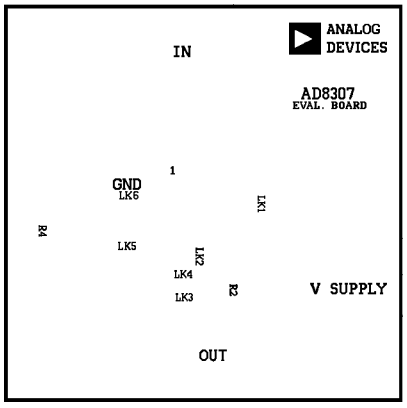


Figure 47. Component Side Silkscreen

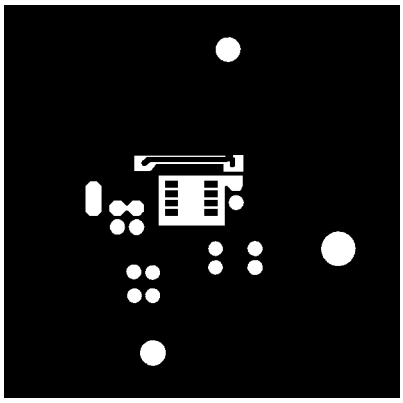


Figure 48. Board Layout (Component Side)

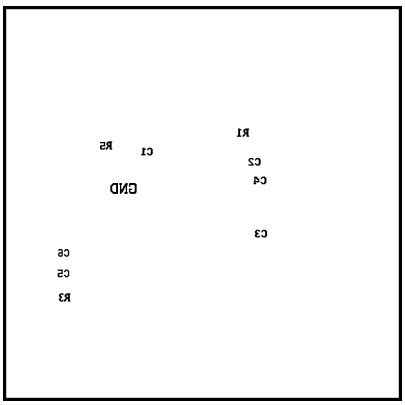


Figure 49. Solder Side Silkscreen

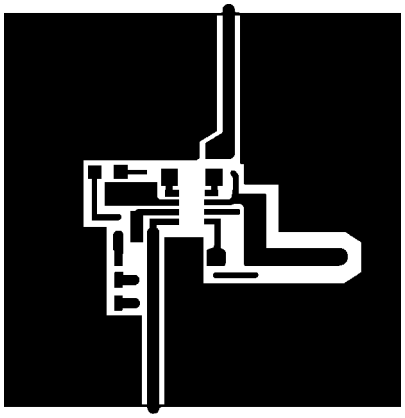


Figure 50. Board Layout (Solder Side)

Link and Trim Options

There are a number of link options and trim potentiometers on the evaluation board which should be set for the required operating setup before using the board. The functions of these link options and trim potentiometers are described in detail in Table II.

Table II. Evaluation Board Link Options

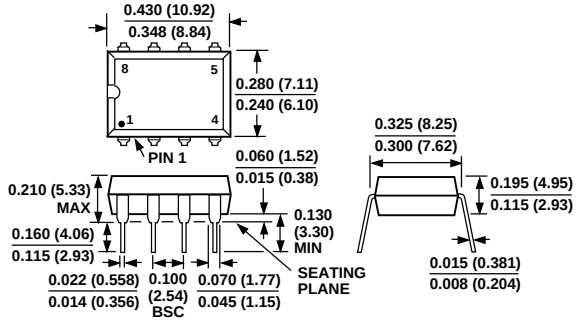
Link No.	Default Position	Function
LK1	A	Power Up/Power Down. When this link is in position B, the ENB pin is connected to ground, putting the AD8307 in power-down mode. Placing this link in position A connects the ENB pin to the positive supply, thereby putting the AD8307 in normal operating mode.
LK2	Open	Intercept Adjust. When Pin LK2 is left open, the AD8307 has a nominal logarithmic intercept of –84 dBm. Putting LK2 in place connects the wiper of potentiometer R2 to Pin 5 (INT). By varying the voltage on INT, the position of the intercept can be adjusted. The intercept varies by about 8 dB/V.
LK3	Open	Slope Adjust. When this link is open, the nominal slope of the output is 25 mV/dB. Putting this link in place connects a ground referenced 12.5 kΩ load resistor (R3) to the logarithmic output. The parallel combination of this resistor and an internal 12.5 kΩ resistor reduces the logarithmic slope to 12.5 mV/dB. R3 may be adjusted for other scaling factors.
LK4	Open	Corner Frequency of Low-Pass Demodulating Filter. When this link is open, the corner frequency of the low pass post demodulation filter has a nominal value of 4 MHz. This is set by an on-chip load impedance of 12.5 kΩ and an on-chip load capacitance of 3.5 pF. The load capacitance (e.g., of an oscilloscope probe) must be added to this capacitance, and will lower the internal video bandwidth, to a nominal 1 MHz for a total of 13.5 pF. Putting LK4 in place connects an external load capacitance (C5) of 0.1 μF to the output, reducing the corner frequency of the low-pass filter to about 125 Hz. For large values of C5, the corner frequency can be calculated using the equation, $f \approx 12.7\ Hz/C5\ (\mu F)$.
LK5	Open	Offset Control Loop. When this link is open, the internal offset control loop gives the circuit an overall high pass corner frequency of about 1 MHz. With LK5 link in place, a 1 nF capacitor (C6) is connected to the OFS pin, reducing the high pass corner frequency to allow accurate operation down to 10 kHz. To reduce the minimum operational frequency even further, a larger capacitor can replace C6 (e.g., a 1 μF capacitor allows operation down to 10 Hz). Note that that external capacitor C6 has no effect on the minimum signal frequency for input levels that exceed the offset voltage (typically 400 μV). The range for such signals extends down to dc (for signals applied directly to the input pins).

C3065a–0–3/99

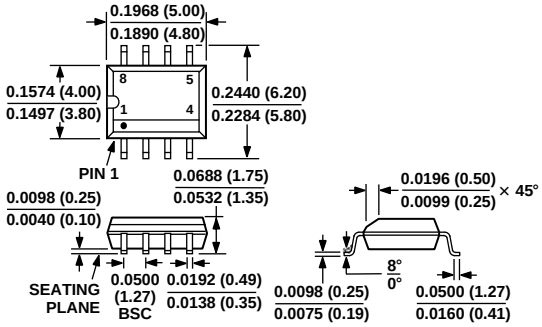
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP
(N-8)



8-Lead SOIC
(SO-8)



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