



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V <sub>CC</sub> Supply Voltage	7.0V
V <sub>2</sub> Supply Voltage	−30V
V <sub>3</sub> Supply Voltage	30V
V <sub>3</sub> –V <sub>2</sub> Voltage Differential	40V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C
Maximum Power Dissipation* at 25°C	
Metal Can (TO-5) Package	690 mW

\*Derate metal can package 4.6 mW/°C above 25°C.

## Operating Conditions

	Min	Max	Units
Supply Voltage, V <sub>CC</sub>			
DS7800	4.5	5.5	V
DS8800	4.75	5.25	V
Temperature (T <sub>A</sub> )			
DS7800	−55	+125	°C
DS8800	0	+70	°C

## Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 6)	Max	Units
V <sub>IH</sub>	Logical “1” Input Voltage	V <sub>CC</sub> = Min	2.0			V
V <sub>IL</sub>	Logical “0” Input Voltage	V <sub>CC</sub> = Min			0.8	V
I <sub>IH</sub>	Logical “1” Input Current	V <sub>CC</sub> = Max				
		V <sub>IN</sub> = 2.4V			5	μA
		V <sub>IN</sub> = 5.5V			1	mA
I <sub>IL</sub>	Logical “0” Input Current	V <sub>CC</sub> = Max, V <sub>IN</sub> = 0.4V		−0.2	−0.4	mA
I <sub>OL</sub>	Output Sink Current	V <sub>CC</sub> = Min, V <sub>IN</sub> = 2V, V <sub>3</sub> Open				
		DS7800	1.6			mA
		DS8800	2.3			mA
I <sub>OH</sub>	Output Leakage Voltage	V <sub>CC</sub> = Max, V <sub>IN</sub> = 0.8V (Notes 4 and 7)			10	μA
R <sub>O</sub>	Output Collector Resistor	T <sub>A</sub> = 25°C	11.5	16.0	20.0	kΩ
V <sub>OL</sub>	Logical “0” Output Voltage	V <sub>CC</sub> = Min, V <sub>IN</sub> = 2.0V (Note 7)			V <sub>2</sub> + 2.0	V
I <sub>CC(MAX)</sub>	Power Supply Current Output “ON” Per Gate	V <sub>CC</sub> = Max, V <sub>IN</sub> = 4.5V (Note 5)		0.85	1.6	mA
I <sub>CC(MIN)</sub>	Power Supply Current Output “OFF” Per Gate	V <sub>CC</sub> = Max, V <sub>IN</sub> = 0V (Note 5)		0.22	0.41	mA

## Switching Characteristics T<sub>A</sub> = 25°C, nominal power supplies unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t <sub>pd0</sub>	Transition Time to Logical “0” Output	T <sub>A</sub> = 25°C, C = 15 pF (Note 8)	25	70	125	ns
t <sub>pd1</sub>	Transition Time to Logical “1” Output	T <sub>A</sub> = 25°C, C = 15 pF (Note 9)	25	62	125	ns

**Note 1:** “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. Except for “Operating Temperature Range” they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

**Note 2:** Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7800 and across the 0°C to +70°C range for the DS8800.

**Note 3:** All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

**Note 4:** Current measured is drawn from V<sub>3</sub> supply.

**Note 5:** Current measured is drawn from V<sub>CC</sub> supply.

**Note 6:** All typical values are measured at T<sub>A</sub> = 25°C with V<sub>CC</sub> = 5.0V, V<sub>2</sub> = −22V, V<sub>3</sub> = +8V.

**Note 7:** Specification applies for all allowable values of V<sub>2</sub> and V<sub>3</sub>.

**Note 8:** Measured from 1.5V on input to 50% level on output.

**Note 9:** Measured from 1.5V on input to logic “0” voltage, plus 1V.

## Theory of Operation

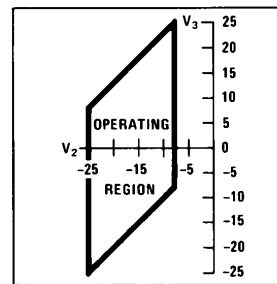
The two input diodes perform the AND function on TTL input voltage levels. When at least one input voltage is a logical "0", current from  $V_{CC}$  (nominally 5.0V) passes through  $R_1$  and out the input(s) which is at the low voltage. Other than small leakage currents, this current drawn from  $V_{CC}$  through the 20 k $\Omega$  resistor is the only source of power dissipation in the logical "1" output state.

When both inputs are at logical "1" levels, current passes through  $R_1$  and diverts to transistor  $Q_1$ , turning it on and thus pulling current through  $R_2$ . Current is then supplied to the PNP transistor,  $Q_2$ . The voltage losses caused by current through  $Q_1$ ,  $D_3$ , and  $Q_2$  necessitate that node P reach a voltage sufficient to overcome these losses before current begins to flow. To achieve this voltage at node P, the inputs must be raised to a voltage level which is one diode potential lower than node P. Since these levels are exactly the same as those experienced with conventional TTL, the interfacing with these types of circuits is achieved.

Transistor  $Q_2$  provides "constant current switching" to the output due to the common base connection of  $Q_2$ . When at least one input is at the logical "0" level, no current is delivered to  $Q_2$ ; so that its collector supplies essentially zero current to the output stage. But when both inputs are raised to a logical "1" level current is supplied to  $Q_2$ .

## Selecting Power Supply Voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply  $V_2$  is shown on the X axis. It must be between -25V and -8V. The allowable range for power supply  $V_3$  is governed by supply  $V_2$ . With a value chosen for  $V_2$ ,  $V_3$  may be selected as any value along a vertical line passing through the  $V_2$  value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.



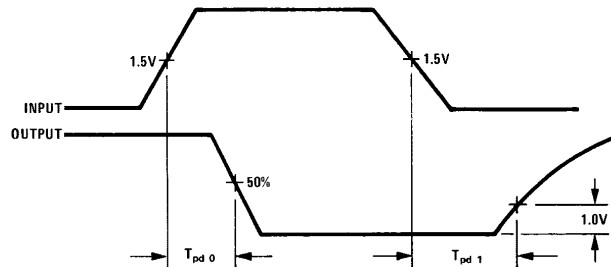
TL/F/5827-5

Since this current is relatively constant, the collector of  $Q_2$  acts as a constant current source for the output stage. Logic inversion is performed since logical "1" input voltages cause current to be supplied to  $Q_2$  and  $Q_3$ . And when  $Q_3$  turns on the output voltage drops to the logical "0" level.

The reason for the PNP current source,  $Q_2$ , is so that the output stage can be driven from a high impedance. This allows voltage  $V_2$  to be adjusted in accordance with the application. Negative voltages to -25V can be applied to  $V_2$ . Since the output will neither source nor sink large amounts of current, the output voltage range is almost exclusively dependent upon the values selected for  $V_2$  and  $V_3$ .

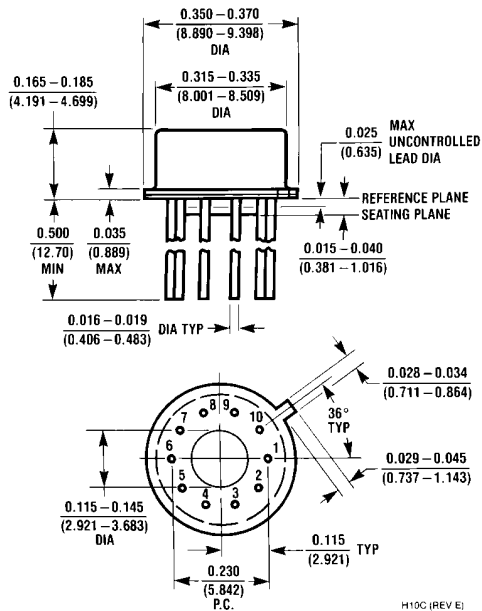
Maximum leakage current through the output transistor  $Q_3$  is specified at 10  $\mu$ A under worst-case voltage between  $V_2$  and  $V_3$ . This will result in a logical "1" output voltage which is 0.2V below  $V_3$ . Likewise the clamping action of diodes  $D_4$ ,  $D_5$ , and  $D_6$ , prevents the logical "0" output voltage from falling lower than 2V above  $V_2$ , thus establishing the output voltage swing at typically 2 volts less than the voltage separation between  $V_2$  and  $V_3$ .

## Switching Time Waveforms



TL/F/5827-6

## Physical Dimensions inches (millimeters)



**Metal Can Package (H)**  
**Order Number DS7800H or DS8800H**  
**NS Package Number H10C**

H10C (REV E)

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