19-0055; Rev 0; 8/92

MAXIM

CMOS, 12-Bit, Serial-Input Multiplying DAC

1.0 SCOPE

1.1 This specification covers the detail requirements for a serial-input digital-to-analog converter. This circuit is processed in accordance with MIL-STD-883 and is fully compliant to paragraph 1.2.1.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace source control drawings.

For typical applications and operating characteristics, consult Maxim's data books.

1.2 Part Numbers

Device	Part Number
-1	MAX543AM(X)/883B
-2	MAX543BM(X)/883B

1.3 Package

(X)	Package	Description
JA	J-8	8-Pin Ceramic Dual-In-Line Package (CERDIP)

Note: See *Package Information* section for package drawing and dimensions.

1.4 Absolute Maximum Ratings

(T_A = +25°C, unless otherwise noted.)

V_{DD} to GND ..... +17V
VREF to GND ..... ±25V
V_{RFB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, (V_{DD} + 0.3V)
V_{IOUT} to GND ..... -0.3V, (V_{DD} + 0.3V)
Power Dissipation (Tj = +150°C)
  up to +70°C 640mW
  derate above +70°C ..... 8mW/°C
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

1.5 Thermal Resistance

Θ_{JC} = 55°C/W
Θ_{JA} = 125°C/W

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2.0 REQUIREMENTS

2.1 Electrical performance characteristics are specified in Table 1 and apply over the full ambient operating temperature range, unless otherwise specified.

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
STATIC PERFORMANCE							
Resolution	N		All	1, 2, 3	12		Bits
Integral Nonlinearity	INL		-1	1, 2, 3		±1/2	LSB
			-2	1, 2, 3		±1	
Differential Nonlinearity	DNL	Guaranteed monotonic	-1	1, 2, 3		±1/2	LSB
			-2	1, 2, 3		±1	
Gain Error	FSE	Use internal R_{FB}	-1	1		±1	LSB
			-2	1		±2	
			-1, -2	2, 3		±2	
Gain Tempco (Note 2)	TCFS	Use Internal R_{FB}	All			±5	ppm/°C
DC Supply Rejection	PSR	ΔV_{DD} = ±5%	All	1, 2, 3		±0.001	%/%
DYNAMIC PERFORMANCE							
Current Settling Time	t_S	(Note 3)	All	9		1	µs
Digital-to-Analog Glitch	Q	(Note 4)	All	4		20	nV-s
AC Feedthrough at I_{OUT}	FTE	(Note 5)	All	4		1	mV_{p-p}
Output Noise-Voltage Density	en	(Note 6)	All	4		15	$nV/\sqrt{Hz}$
REFERENCE INPUT							
Input Resistance	RREF		All	1, 2, 3	7	15	kΩ
ANALOG INPUT							
I_{OUT} Leakage Current	I_{LKG}	DAC register all 0s	All	1		±5	nA
				2, 3		±100	
Output Capacitance	C_{OUT}	DAC register all 0s	All	4		80	pF
		DAC register all 1s				110	
DIGITAL INPUTS							
Input High Voltage	V_{IH}	V_{DD} = 5V	All	1, 2, 3	2.4		V
		V_{DD} = 15V			13.5		
Input Low Voltage	V_{IL}	V_{DD} = 5V	All	1, 2, 3		0.8	V
		V_{DD} = 15V				1.5	
Input Leakage Current	I_{IN}	Digital inputs = 0V or V_{DD}	All	1, 2, 3		±1	µA
Input Capacitance	C_{IN}	Digital inputs = 0V or V_{DD}	All	4		8	pF

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1) (continued)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
SWITCHING CHARACTERISTICS							
CLK Pulse Width High	t_{CH}		All	9	90		ns
CLK Pulse Width Low	t_{CL}		All	9	120		ns
SRI Data to CLK Setup	t_{DS}		All	9	40		ns
SRI Data to CLK Hold	t_{DH}		All	9	80		ns
$\overline{LOAD}$ Pulse Width	t_{LD}		All	9	120		ns
LSB CLK to $\overline{Load}$	t_{SL}		All	9	0		ns
$\overline{LOAD}$ High to CLK	t_{LC}		All	9	0		ns
POWER SUPPLY							
Positive Supply Range (Note 7)	V_{DD}	V_{DD} = 5V	All	1, 2, 3	4.75	5.25	V
		V_{DD} = 15V			14.25	15.75	
Negative Supply Range	I_{DD}	All digital inputs = V_{IL} or V_{IH}	All	1, 2, 3		500	µA
		All digital inputs = 0V or V_{DD}				100	

Note 1: V_{DD} = +5V or +15V, VREF = +10V, I_{OUT} = GND = 0V, unless otherwise noted.
Note 2: Characteristics supplied for use as a typical design limit, but not production tested.
Note 3: Settling time to 1/2LSB. I_{OUT} load is 100Ω | | 13pF. DAC register alternately loaded with all 1s and all 0s.
Note 4: VREF = 0V. I_{OUT} load is 100Ω | | 13pF. DAC register alternately loaded with all 1s and all 0s.
Note 5: VREF = ±10Vp-p at 10kHz. DAC register loaded with all 0s.
Note 6: 10Hz to 100kHz. Measured between R_{FB} and I_{OUT}.
Note 7: Guaranteed by PSR testing.

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3.0 QUALITY ASSURANCE

3.1 Sampling and inspection procedures shall be in accordance with MIL-M-38510 and, to the extent specified, with MIL-STD-883.

3.2 Screening shall be in accordance with Method 5004 of MIL-STD-883. Burn-in test (Method 1015):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Interim and final electrical test requirements shall be as specified in Table 2.

3.3 Quality conformance inspection shall be in accordance with Method 5005 of MIL-STD-883 including Groups A, B, C, and D inspection.
Group A inspection:
(1) Tests as specified in Table 2.
(2) Selected subgroups in Table 1, Method 5005 of MIL-STD-883 shall be omitted.

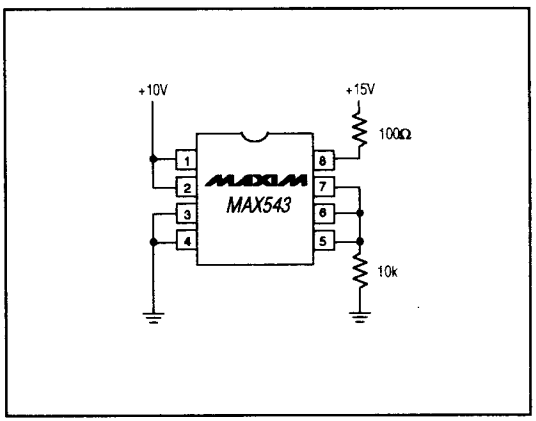
3.4 Groups C and D inspections:
a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test (Method 1005 of MIL-STD-883):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Test duration, 1000 hours, except as permitted by Method 1005 of MIL-STD-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

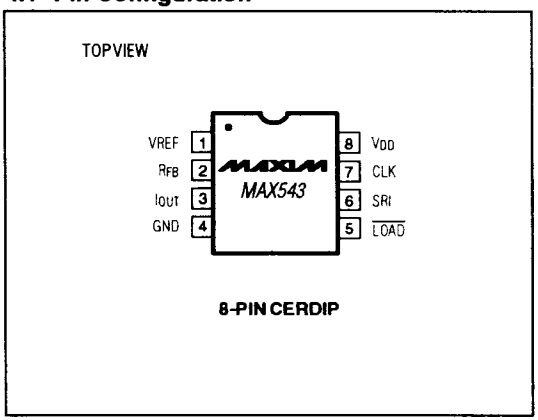
MIL-STD-883 Test Requirements	Subgroups (per Method 5005, Table 1)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Parameters (Method 5004)	1,* 2, 3, 9
Group A Test Requirements (Method 5005)	1, 2, 3, 4,** 9
Groups C and D End-Point Electrical Parameters (Method 5005)	1

* PDA applies to Subgroup 1 only.
** Subgroup 4 shall be tested at initial qualification and upon redesign. Sample size will be 5 units.

4.0 Life Test/Burn-In Circuit



4.1 Pin Configuration



4.2 Functional Diagram