

DATA SHEET

74ABT620

Octal transceiver with dual enable,
inverting (3-State)

Product specification

1993 Jun 21

IC23 Data Handbook

Octal transceiver with dual enable, inverting (3-State)

74ABT620

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Power-up 3-State
- Live insertion/extraction permitted
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT620 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT620 device is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The 74ABT620 is designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs (\overline{OEBA} and OEAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

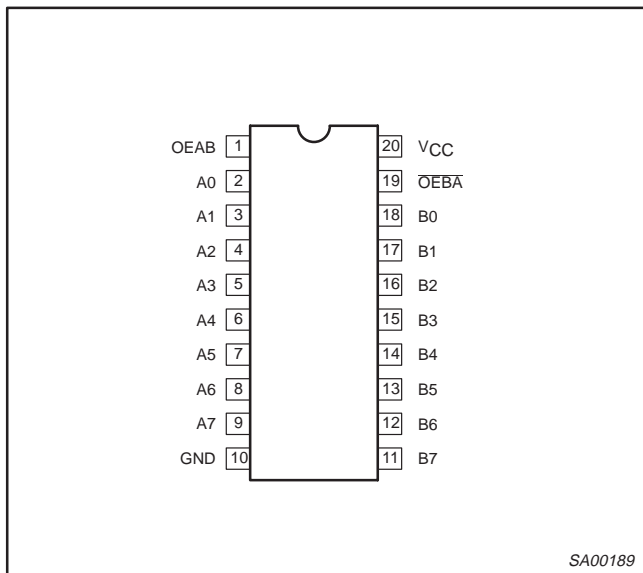
QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$ | TYPICAL | UNIT |
|------------------------|--|--|---------|---------------|
| t_{PLH} t_{PHL} | Propagation delay An to Bn or Bn to An | $C_L = 50\text{pF}; V_{CC} = 5\text{V}$ | 3.1 | ns |
| C_{IN} | Input capacitance OEAB, \overline{OEBA} | $V_I = 0\text{V}$ or V_{CC} | 4 | pF |
| $C_{I/O}$ | I/O capacitance | Outputs disabled; $V_O = 0\text{V}$ or V_{CC} | 7 | pF |
| I_{CCZ} | Total supply current | Outputs disabled; $V_{CC} = 5.5\text{V}$ | 50 | μA |

ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|-----------------------------|-------------------|-----------------------|---------------|------------|
| 20-Pin Plastic DIP | -40°C to +85°C | 74ABT620 N | 74ABT620 N | SOT146-1 |
| 20-Pin plastic SO | -40°C to +85°C | 74ABT620 D | 74ABT620 D | SOT163-1 |
| 20-Pin Plastic SSOP Type II | -40°C to +85°C | 74ABT620 DB | 74ABT620 DB | SOT339-1 |
| 20-Pin Plastic TSSOP Type I | -40°C to +85°C | 74ABT620 PW | 74ABT620PW DH | SOT360-1 |

PIN CONFIGURATION



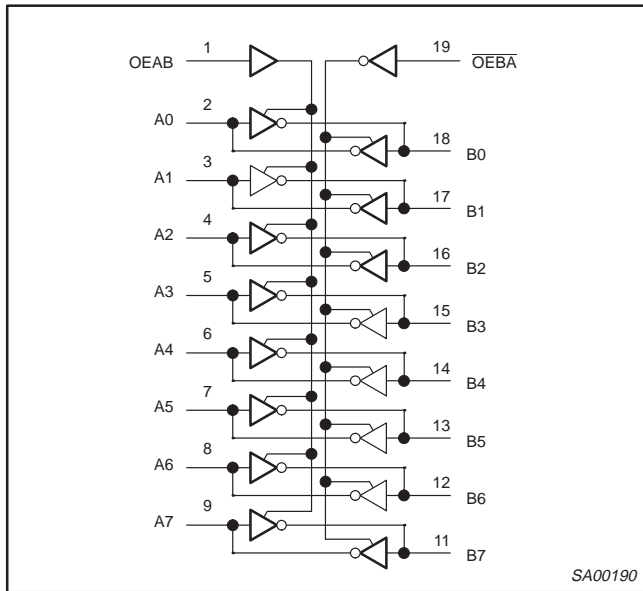
PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|--------------------------------|-------------------|---|
| 1 | OEAB | Output enable input, A side to B side (active-High) |
| 2, 3, 4, 5, 6, 7, 8, 9 | A0 – A7 | Data inputs/outputs (A side) |
| 18, 17, 16, 15, 14, 13, 12, 11 | B0 – B7 | Data inputs/outputs (B side) |
| 19 | \overline{OEBA} | Output enable input, B side to A side (active-Low) |
| 10 | GND | Ground (0V) |
| 20 | V_{CC} | Positive supply voltage |

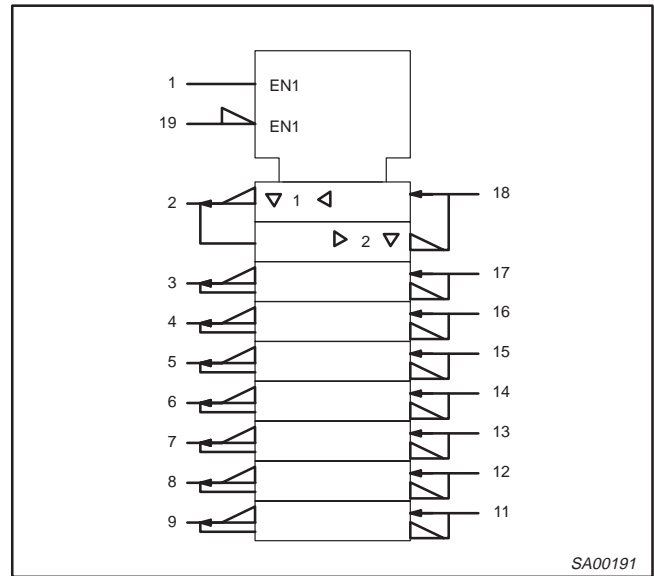
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LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

| INPUTS | | INPUTS/OUTPUTS | |
|--------|------|--|-------------|
| OEBA | OEAB | An | Bn |
| L | L | \bar{B}_n | Inputs |
| H | H | Inputs | \bar{A}_n |
| H | L | Z | Z |
| L | H | \bar{B}_n Inputs or Inputs \bar{A}_n | |

H = High voltage level
 L = Low voltage level
 Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS^{1, 2}

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|-----------|--------------------------------|-----------------------------|--------------|------|
| V_{CC} | DC supply voltage | | -0.5 to +7.0 | V |
| I_{IK} | DC input diode current | $V_I < 0$ | -18 | mA |
| V_I | DC input voltage ³ | | -1.2 to +7.0 | V |
| I_{OK} | DC output diode current | $V_O < 0$ | -50 | mA |
| V_{OUT} | DC output voltage ³ | output in Off or High state | -0.5 to +5.5 | V |
| I_{OUT} | DC output current | output in Low state | 128 | mA |
| T_{stg} | Storage temperature range | | -65 to 150 | °C |

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|---------------------|--------------------------------------|--------|----------|------|
| | | Min | Max | |
| V_{CC} | DC supply voltage | 4.5 | 5.5 | V |
| V_I | Input voltage | 0 | V_{CC} | V |
| V_{IH} | High-level input voltage | 2.0 | | V |
| V_{IL} | Low-level Input voltage | | 0.8 | V |
| I_{OH} | High-level output current | | -32 | mA |
| I_{OL} | Low-level output current | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | 5 | ns/V |
| T_{amb} | Operating free-air temperature range | -40 | +85 | °C |

DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT |
|--------------------|--|---|---------------------------------|------------|-----------|---|-----------|---------------|
| | | | $T_{amb} = +25^{\circ}\text{C}$ | | | $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | | |
| | | | Min | Typ | Max | Min | Max | |
| V_{IK} | Input clamp voltage | $V_{CC} = 4.5\text{V}; I_{IK} = -18\text{mA}$ | | -0.9 | -1.2 | | -1.2 | V |
| V_{OH} | High-level output voltage | $V_{CC} = 4.5\text{V}; I_{OH} = -3\text{mA}; V_I = V_{IL}$ or V_{IH} | 2.5 | 2.9 | | 2.5 | | V |
| | | $V_{CC} = 5.0\text{V}; I_{OH} = -3\text{mA}; V_I = V_{IL}$ or V_{IH} | 3.0 | 3.4 | | 3.0 | | V |
| | | $V_{CC} = 4.5\text{V}; I_{OH} = -32\text{mA}; V_I = V_{IL}$ or V_{IH} | 2.0 | 2.4 | | 2.0 | | V |
| V_{OL} | Low-level output voltage | $V_{CC} = 4.5\text{V}; I_{OL} = 64\text{mA}; V_I = V_{IL}$ or V_{IH} | | 0.42 | 0.55 | | 0.55 | V |
| I_I | Input leakage current | Control pins $V_{CC} = 5.5\text{V}; V_I = \text{GND}$ or 5.5V | | ± 0.01 | ± 1.0 | | ± 1.0 | μA |
| | | Data pins $V_{CC} = 5.5\text{V}; V_I = \text{GND}$ or 5.5V | | ± 5 | ± 100 | | ± 100 | μA |
| I_{OFF} | Power-off leakage current | $V_{CC} = 0.0\text{V}; V_O$ or $V_I \leq 4.5\text{V}$ | | ± 5.0 | ± 100 | | ± 100 | μA |
| I_{PU}/I_{PD} | Power-up/down 3-State output current ³ | $V_{CC} = 2.1\text{V}; V_O = 0.5\text{V}; V_I = \text{GND}$ or V_{CC} ; V_{OE} and $\overline{V_{OE}} = \text{Don't care}$ | | ± 5.0 | ± 50 | | ± 50 | μA |
| $I_{IH} + I_{OZH}$ | 3-State output High current | $V_{CC} = 5.5\text{V}; V_O = 2.7\text{V}; V_I = V_{IL}$ or V_{IH} | | 5.0 | 50 | | 50 | μA |
| $I_{IL} + I_{OZL}$ | 3-State output Low current | $V_{CC} = 5.5\text{V}; V_O = 0.5\text{V}; V_I = V_{IL}$ or V_{IH} | | -5.0 | -50 | | -50 | μA |
| I_{CEX} | Output High leakage current | $V_{CC} = 5.5\text{V}; V_O = 5.5\text{V}; V_I = \text{GND}$ or V_{CC} | | 5.0 | 50 | | 50 | μA |
| I_O | Output current ¹ | $V_{CC} = 5.5\text{V}; V_O = 2.5\text{V}$ | -50 | -100 | -180 | -50 | -180 | mA |
| I_{CCH} | Quiescent supply current | $V_{CC} = 5.5\text{V}; \text{Outputs High}, V_I = \text{GND}$ or V_{CC} | | 50 | 250 | | 250 | μA |
| I_{CCL} | | $V_{CC} = 5.5\text{V}; \text{Outputs Low}, V_I = \text{GND}$ or V_{CC} | | 24 | 30 | | 30 | mA |
| I_{CCZ} | | $V_{CC} = 5.5\text{V}; \text{Outputs 3-State}; V_I = \text{GND}$ or V_{CC} | | 50 | 250 | | 250 | μA |
| ΔI_{CC} | Additional supply current per input pin ² | $V_{CC} = 5.5\text{V}; \text{one input at } 3.4\text{V}, \text{ other inputs at } V_{CC}$ or GND | | 0.05 | 1.5 | | 1.5 | mA |

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From $V_{CC} = 2.1\text{V}$ to $V_{CC} = 5\text{V} \pm 10\%$ a transition time of up to 100 μsec is permitted.

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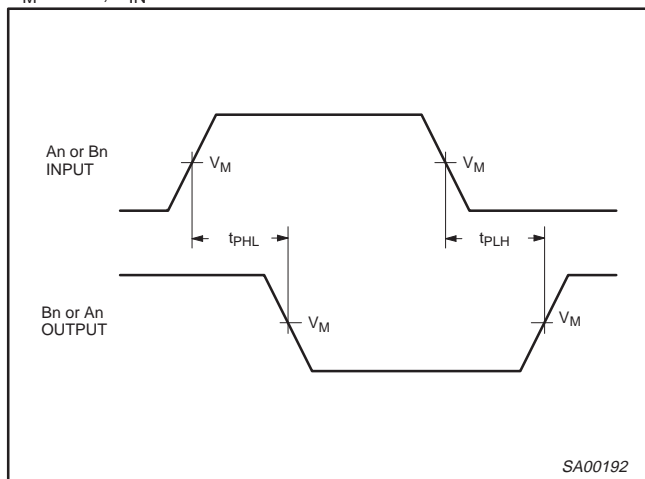
AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

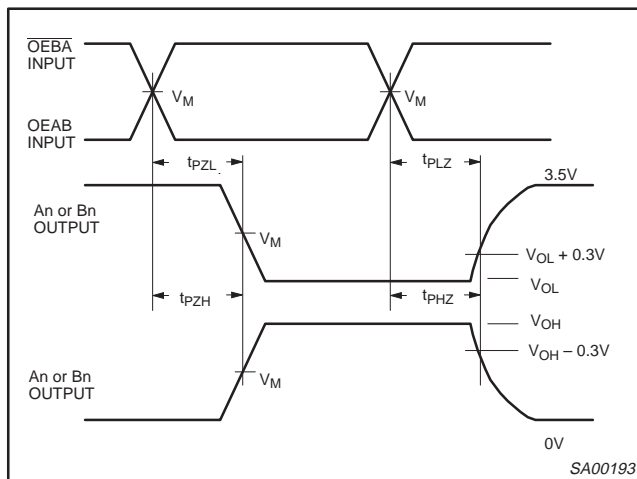
| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | UNIT |
|--------------------------------------|---|----------|--|-----|-----|--|-----|------|
| | | | $T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$ | | | $T_{\text{amb}} = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$ | | |
| | | | Min | Typ | Max | Min | Max | |
| t_{PLH} t_{PHL} | Propagation delay An to Bn or Bn to An | 1 | 1.0 | 2.9 | 4.1 | 1.0 | 4.8 | ns |
| t_{PZH} t_{PZL} | Output enable time OEBA to An | 2 | 1.3 | 3.2 | 4.6 | 1.3 | 5.5 | ns |
| t_{PHZ} t_{PLZ} | Output disable time $\overline{\text{OEBA}}$ to An | 2 | 2.0 | 5.0 | 6.3 | 2.0 | 7.0 | ns |
| t_{PZH} t_{PZL} | Output enable time OEAB to Bn | 2 | 1.6 | 4.6 | 6.2 | 1.6 | 6.8 | ns |
| t_{PHZ} t_{PLZ} | Output disable time OEAB to Bn | 2 | 1.2 | 3.9 | 5.6 | 1.2 | 6.5 | ns |

AC WAVEFORMS

$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



Waveform 1. Waveforms Showing the Input to Output Propagation Delays

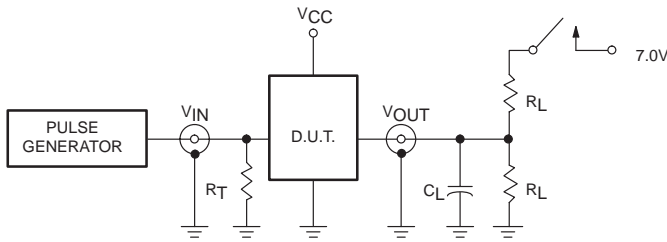


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

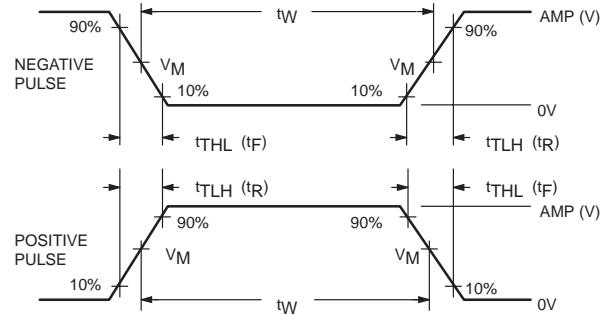
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TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

| TEST | SWITCH |
|------------------|--------|
| t _{PLZ} | closed |
| t _{pZL} | closed |
| All other | open |

DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|--------|--------------------------|-----------|----------------|----------------|----------------|
| | Amplitude | Rep. Rate | t _W | t _R | t _F |
| 74ABT | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |

SA00012

Octal transceiver with dual enable, inverting
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DIP20: plastic dual in-line package; 20 leads (300 mil)
SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT146-1
SOT163-1

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

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DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|----------------------------------|-------------------------------|--|
| <i>Objective Specification</i> | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| <i>Preliminary Specification</i> | Preproduction Product | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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