

# 74ACT11652 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS087A – APRIL 1993 – REVISED APRIL 1996

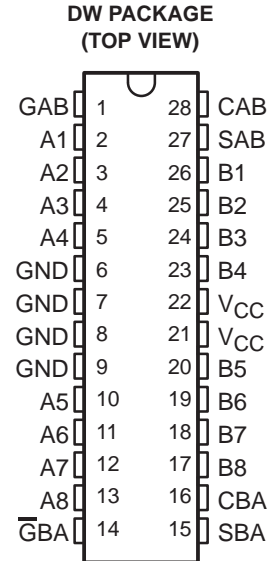
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C

## description

This device consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and  $\overline{GBA}$  are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and  $\overline{GBA}$ . In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The 74ACT11652 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .



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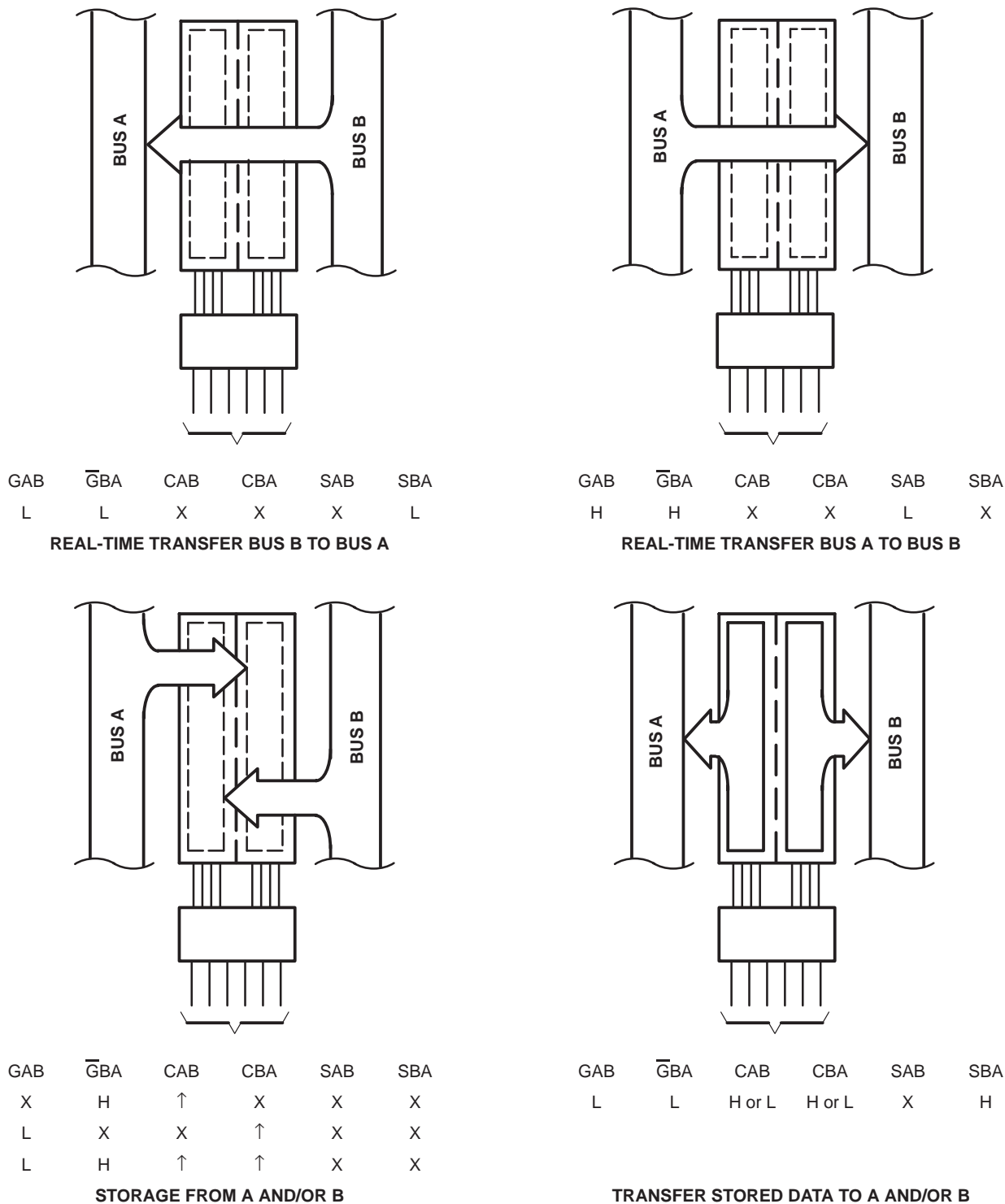


Figure 1. Bus Transfer Diagram

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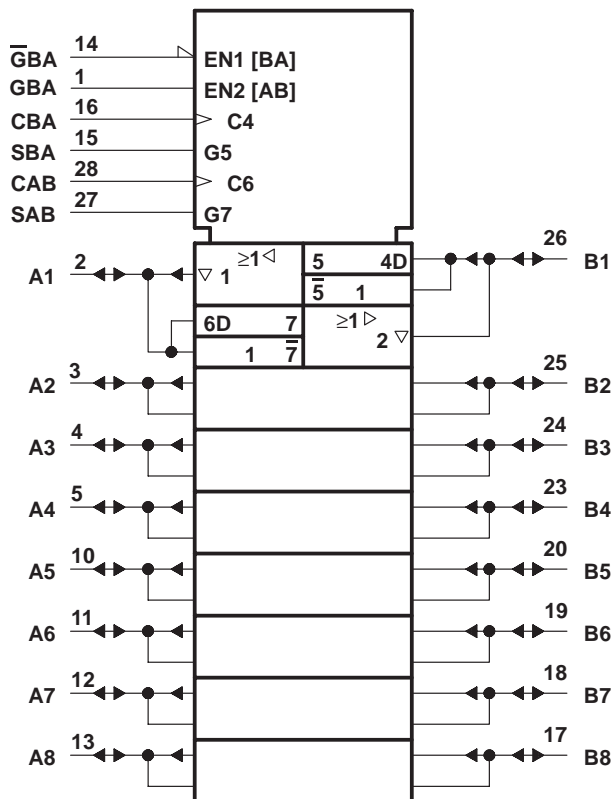
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
GAB	$\overline{\text{GBA}}$	CAB	CBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified†	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified†	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data-output functions may be enabled or disabled by various signals at the GAB or  $\overline{\text{GBA}}$  inputs. Data-input functions are always enabled, i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously. Select control = H: clocks must be staggered to load both registers.

## logic symbols§

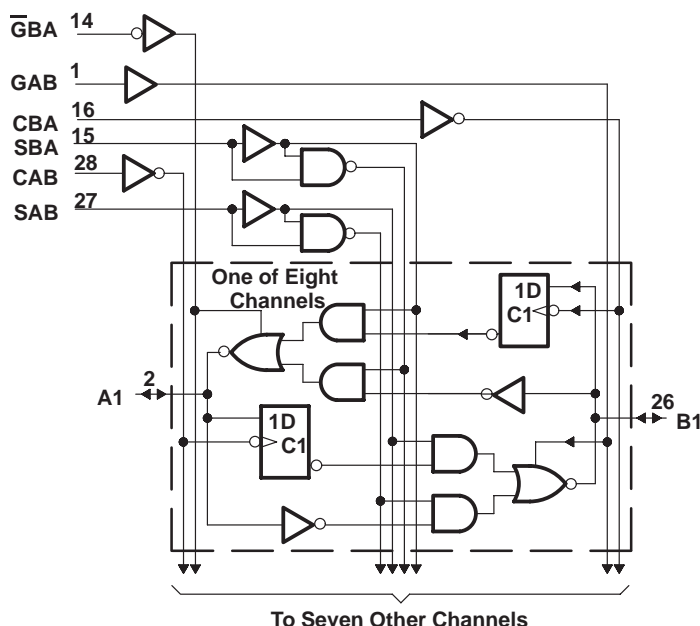


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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## logic diagram (positive logic)



## absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$	.....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	.....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	.....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	.....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	.....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	.....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	.....	$\pm 200$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2)	.....	1.7 W
Storage temperature range, $T_{stg}$	.....	$-65^\circ\text{C}$ to $150^\circ\text{C}$

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils.

## recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24	mA
$I_{OL}$	Low-level output current		24	mA
$\Delta t/\Delta V$	Input transition rise or fall rate	0	10	ns/V
$T_A$	Operating free-air temperature	-40	85	$^\circ\text{C}$

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT	
			MIN	TYP	MAX				
V <sub>OH</sub>	I <sub>OH</sub> = – 50 μA	4.5 V	4.4			4.4		V	
		5.5 V	5.4			5.4			
	I <sub>OH</sub> = – 24 mA	4.5 V	3.94			3.8			
		5.5 V	4.94			4.8			
I <sub>OH</sub> = – 75 mA <sup>†</sup>	5.5 V				3.85				
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V				0.1		V	
		5.5 V				0.1			
	I <sub>OL</sub> = 24 mA	4.5 V				0.36			
		5.5 V				0.36			
I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V				1.65				
I <sub>OZ</sub>	A or B ports <sup>‡</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V	±0.5			±5		μA
I <sub>I</sub>	GAB or $\overline{\text{G}}\text{BA}$	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V	±0.1			±1		μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	8			80		μA
ΔI <sub>CC</sub> <sup>§</sup>		One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V	0.9			1		mA
C <sub>i</sub>	GAB or $\overline{\text{G}}\text{BA}$	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	4.5					pF
C <sub>o</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V	12					pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

<sup>§</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)**

PARAMETER		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f <sub>clock</sub>	Clock frequency	0	105	0	105	MHz
t <sub>w</sub>	Pulse duration, CAB or CBA high or low	4.8		4.8		ns
t <sub>su</sub>	Setup time, A before CLK <sup>↑</sup> or B before CBA <sup>↑</sup>	4		4		ns
t <sub>h</sub>	Hold time, A after CAB <sup>↑</sup> or B after CBA <sup>↑</sup>	2.5		2.5		ns



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f <sub>max</sub>			105			105		MHz
t <sub>PLH</sub>	A or B	B or A	3.8	7	9.9	3.8	11.1	ns
t <sub>PHL</sub>			3.4	6.7	10.7	3.4	11.6	
t <sub>PLH</sub>	CBA or CAB	A or B	5.4	8.4	11.8	5.4	13.1	ns
t <sub>PHL</sub>			6.1	9.4	13.1	6.1	14.4	
t <sub>PLH</sub>	SBA or SAB† with A or B high	A or B	2.8	6.2	10.1	2.8	11	ns
t <sub>PHL</sub>			5.5	8.7	12.1	5.5	13.3	
t <sub>PLH</sub>	SBA or SAB† with A or B low	A or B	4.9	7.8	11	4.9	12.2	ns
t <sub>PHL</sub>			3.9	7.5	11.6	3.9	12.6	
t <sub>PZH</sub>	$\overline{\text{GBA}}$	A	3.3	7.2	11.4	3.3	12.6	ns
t <sub>PZL</sub>			4.1	7.8	12.6	4.1	13.8	
t <sub>PHZ</sub>	$\overline{\text{GBA}}$	A	5.2	7.2	9.3	5.2	9.9	ns
t <sub>PLZ</sub>			4.8	6.7	8.6	4.8	9.3	
t <sub>PZH</sub>	GAB	B	5.1	9.1	13.4	5.1	15.2	ns
t <sub>PZL</sub>			5.8	9.7	14.2	5.8	16.1	
t <sub>PHZ</sub>	GAB	B	3.4	6.8	9.7	3.4	10.3	ns
t <sub>PLZ</sub>			3.1	6	8.8	3.1	9.3	

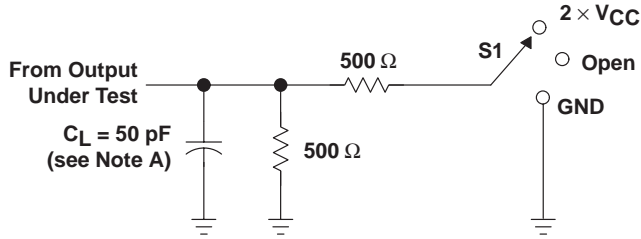
† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

**operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per transceiver	Outputs enabled	59	pF
		Outputs disabled	14	

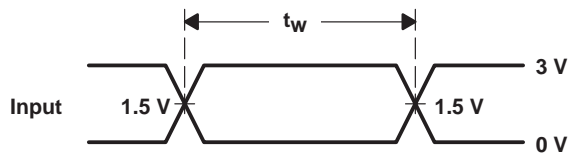


PARAMETER MEASUREMENT INFORMATION

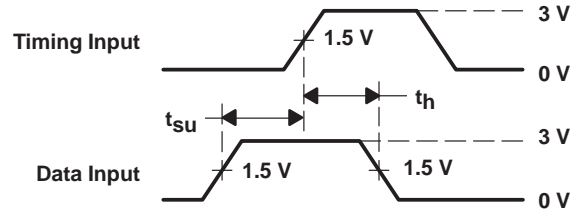


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

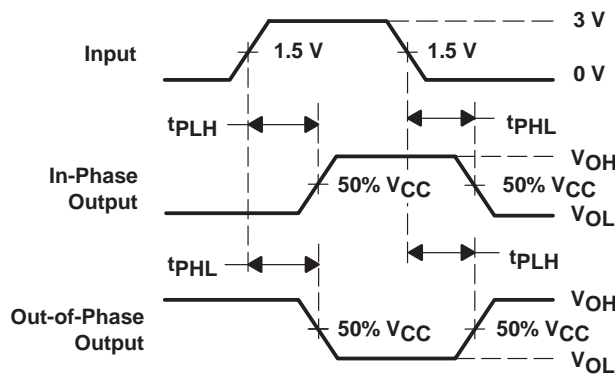
LOAD CIRCUIT



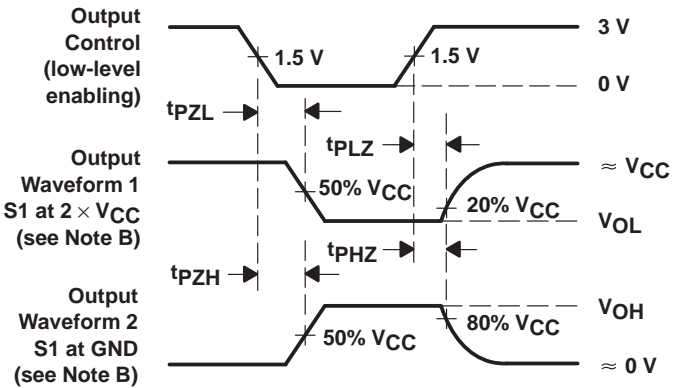
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74ACT11652DW	ACTIVE	SOIC	DW	28	20	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
74ACT11652DWR	ACTIVE	SOIC	DW	28	1000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

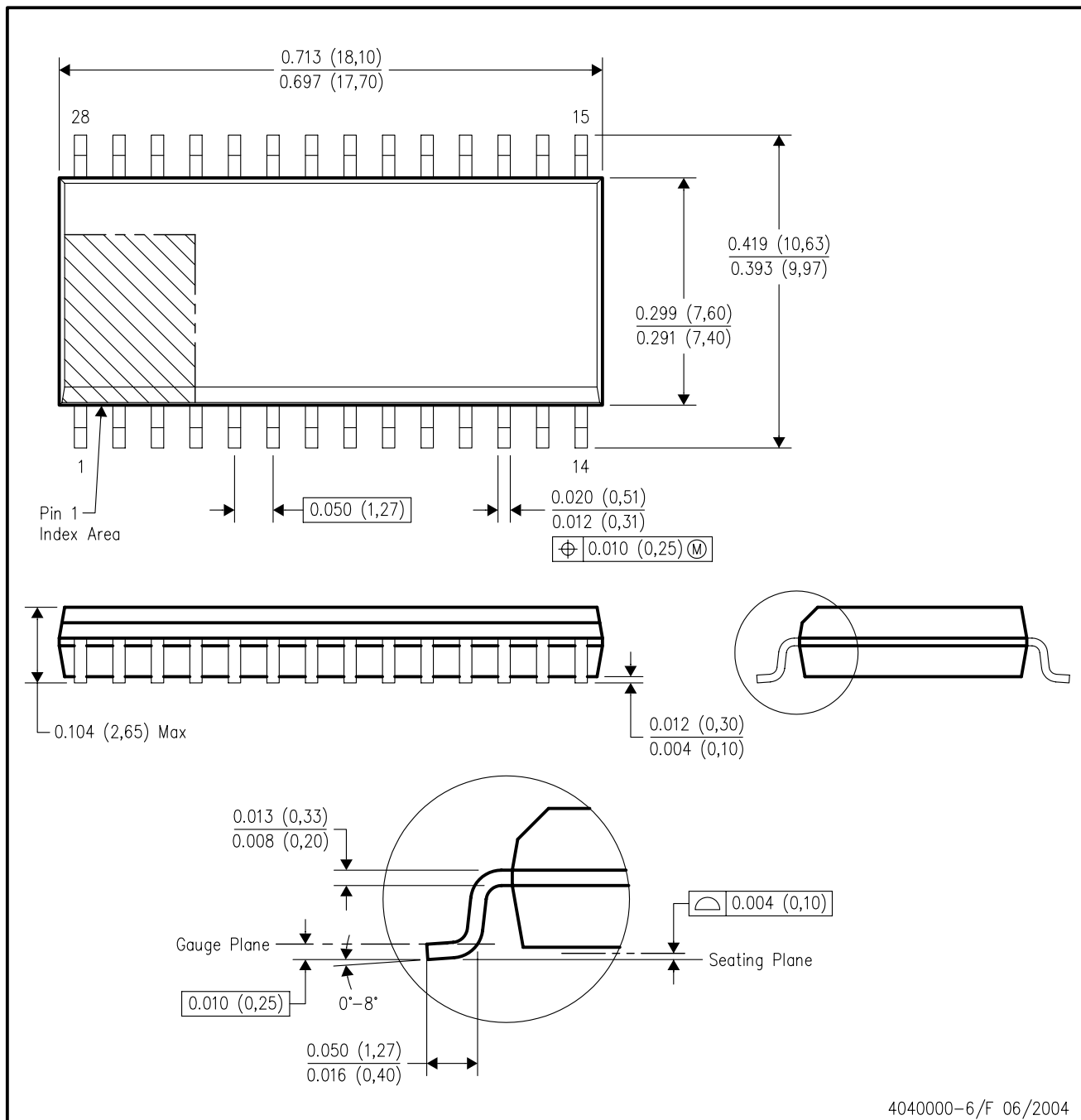
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G28)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AE.

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74ACT11652DWR - <http://www.ti.com/product/74act11652dwr?HQS=TI-null-null-dscatalog-df-pf-null-wwe>

74ACT11652DW - <http://www.ti.com/product/74act11652dw?HQS=TI-null-null-dscatalog-df-pf-null-wwe>

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