

MITSUBISHI MICROCOMPUTERS
M50734SP/FP
M50734SP/FP-10
8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50734SP is a microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP (flat package type also available). This microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50734SP-10 and the M50734SP are noted below.

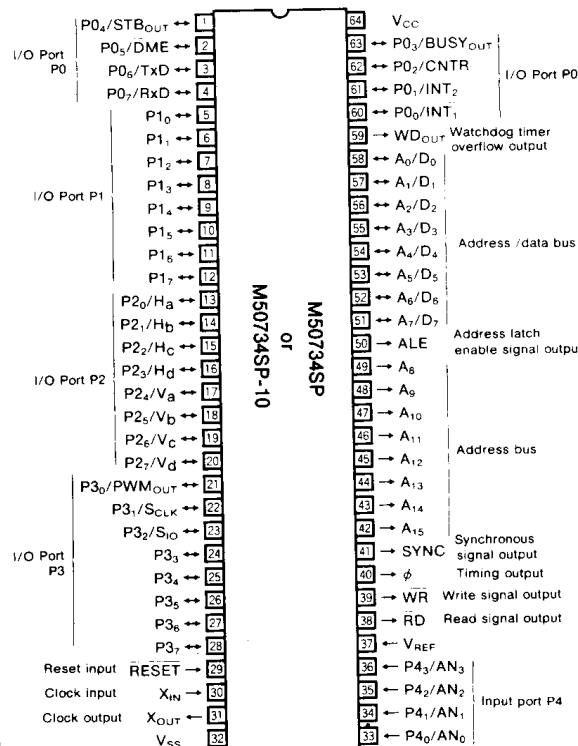
Type name	maximum value of clock generating frequency
M50734SP	8MHz
M50734SP-10	10MHz

The differences between the M50734SP and the M50734FP, and M50734SP-10 and M50734FP-10 are the package outline, the voltage input pins for A-D, and power dissipation ability (absolute maximum ratings).

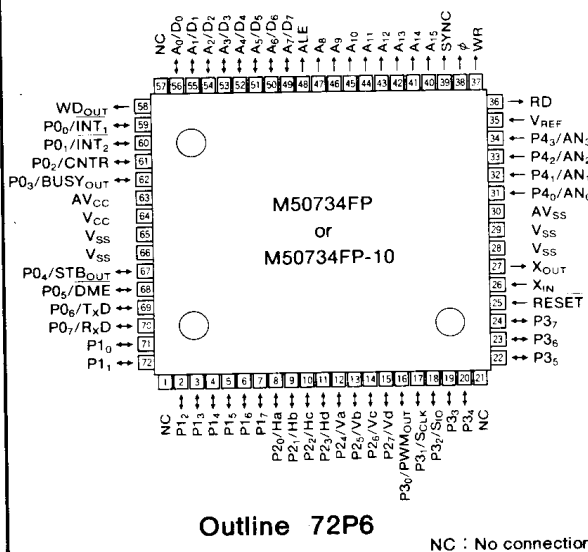
FEATURES

- Number of basic instructions 69
- Memory size (internal memories are not provided)
 Memory area programmable memory 64K bytes
 data memory 64K bytes
- Instruction execution time (minimum instructions)
 1 μ s (at 8MHz frequency M50734SP)
 0.8 μ s (at 10MHz frequency, M50734SP-10)
- Single power supply 5V \pm 10%
- Power dissipation
 normal operation mode (at 8MHz frequency) 30mW
 (at 10MHz frequency) 35mW
- Subroutine nesting 128 levels (Max.)
- Interrupt 11 types, 5 vectors
- Timers
 16-bit timer/event counter (general purpose) 1
 8-bit timer (general purpose) 3
 8-bit timer (watchdog timer) 1
 8-bit timer (strobe timer) 1
 8-bit timer (baud rate timer) 1
 8-bit counter (control for stepper motor) 2
- Stepper motor control circuit
 1 channel for the X or Y direction
- Programmable I/O ports (Ports P0, P1, P2, P3) 32
- Input port (Port P4) 4
- Serial I/O
 8-bit clock synchronous 1
 8-bit UART 1
 Baud rate (at 7.37MHz frequency) 75bps~57600bps
 (at 9.83MHz frequency) 75bps~76800bps
- A-D converter 8-bit successive approximation
- PWM function 1
- Multiplex-type bus
 Address bus 16
 Data bus (multiplexed with lower address bus) 8

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B



Outline 72P6

NC : No connection

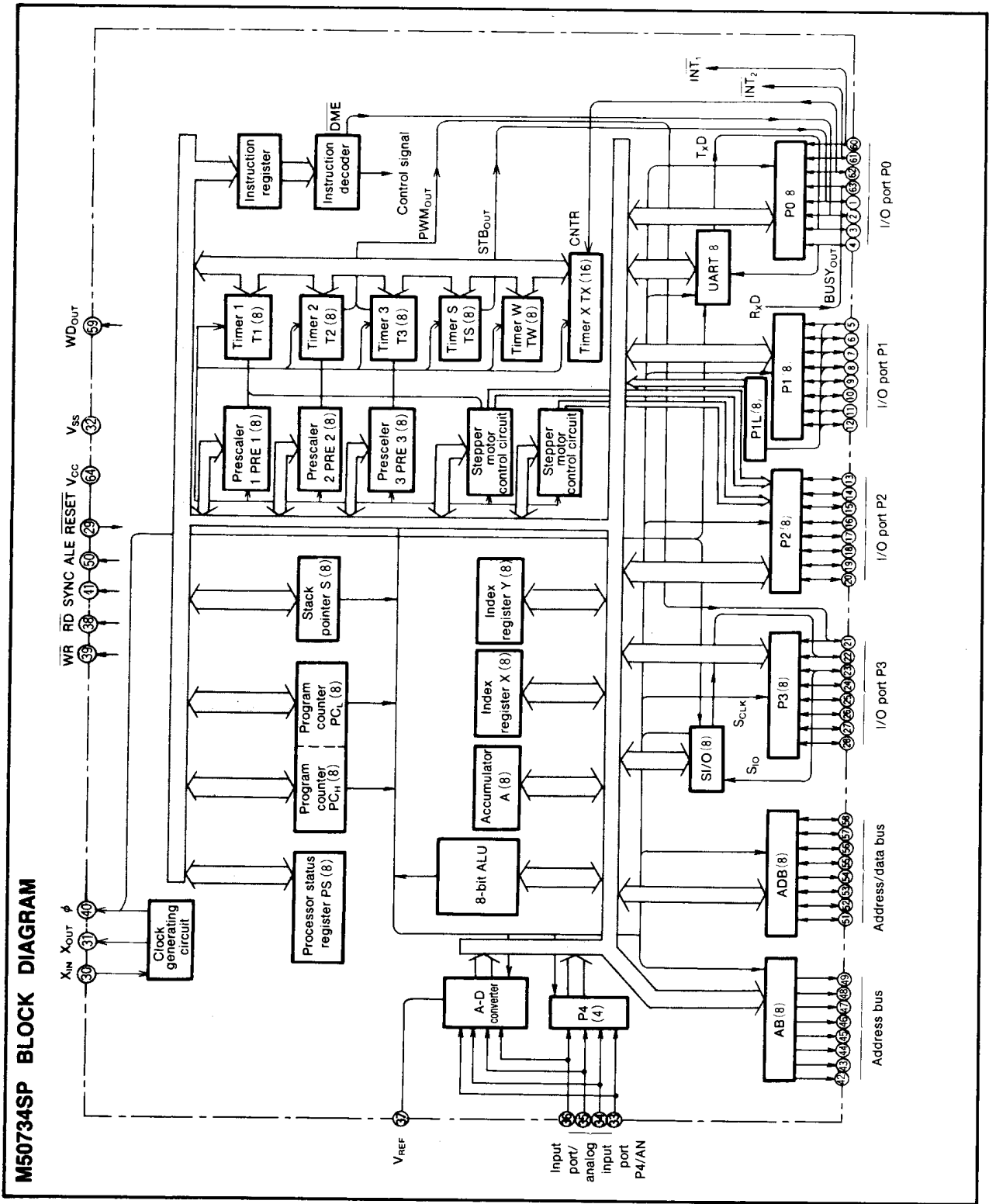
APPLICATION

Printer/plotter, Electronic typewriter, PPC, FAX, Portable word processor, Robotics



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FUNCTIONS OF M50734SP and M50734SP-10

Parameter		Functions
Number of basic instructions		69
Instruction execution time	M50734SP	1 μ s (minimum instructions, at 8MHz frequency)
	M50734SP-10	0.8 μ s (minimum instructions, at 10MHz frequency)
Clock frequency	M50734SP	8MHz
	M50734SP-10	10MHz
Memory size		64K bytes (up to 128k bytes with DME signal)
Input/output ports	P0, P1, P2, P3	I/O
	P4	input
UART	M50734SP	1 (built-in baud rate generator 75~57600bps)
	M50734SP-10	1 (built-in baud rate generator 75~76800bps)
Clock synchronized serial I/O		8-bitX1
Timers	Timer X	16-bitX1
	Timer 1	8-bitX1 (with 8-bit prescaler)
	Timer 2	8-bitX1 (with 8-bit prescaler)
	Timer 3	8-bitX1 (with 8-bit prescaler)
	Timer S	8-bitX1 (with 1/4 frequency divider)
	Timer W	8-bitX1 (with 1/1024 frequency divider)
A-D converter		Four analog inputs, 8-bit successive approximation
Subroutine nesting		128 levels (max.)
Interrupt		Three external interrupts, four timer interrupts Two counter interrupts, one UART interrupt
Clock generating circuit		Built-in (externally connected to a ceramic resonator or a quartz crystal resonator)
Supply voltage		5V \pm 10%
Power dissipation	at normal operation	30mW (M50734SP) 35mW (M50734SP-10)
	at wait mode	5mW
	at stop mode	5 μ W
Operating temperature range		-10~70 $^{\circ}$ C
Device structure		CMOS silicon gate process
Package	M50734SP, M50734SP-10	64-pin shrink plastic molded DIP
	M50734FP, M50734FP-10	72-pin plastic molded QFP

M50734SP ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.3~7	V
V _I	Input voltage, RESET, X _{IN}		-0.3~7	V
V _{REF}	Input voltage, P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₇ , P ₄ ~P ₄₃ , AD ₀ ~AD ₇ , V _{REF}	With respect to V _{SS} .	-0.3~V _{CC} +0.3	V
V _O	Output voltage, P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₇ , AD ₀ ~AD ₇ , A ₈ ~A ₁₅ , RD, WR, φ, SYNC, ALE, WD _{OUT} , X _{OUT}	Output transistors are at "off" state.	-0.3~V _{CC} +0.3	V
P _d	Power dissipation	T _a =25°C	1000	mW
T _{opr}	Operating temperature		-10~70	°C
T _{stg}	Storage temperature		-40~125	°C

Note 1 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = -10~70°C, f(X_{IN}) = 8MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{SS}	Supply voltage		0		V
V _{IH}	"H" input voltage, P ₀ ~P ₀₇ (During using as a port), P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₇ , P ₄ ~P ₄₃ , AD ₀ ~AD ₇	2.0		V _{CC} +0.3	V
V _{IH}	"H" input voltage, RxD, CNTR, INT ₁ , INT ₂ , RESET, X _{IN}	0.8V _{CC}		V _{CC} +0.3	V
V _{IL}	"L" input voltage, P ₀ ~P ₀₇ (During using as a port), P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₇ , P ₄ ~P ₄₃ , AD ₀ ~AD ₇	-0.3		0.8	V
V _{IL}	"L" input voltage, RxD, CNTR, INT ₁ , INT ₂	-0.3		0.2V _{CC}	V
V _{IL}	"L" input voltage, RESET	-0.3		0.12V _{CC}	V
V _{IL}	"L" input voltage, X _{IN}	-0.3		0.16V _{CC}	V
V _{REF}	Standard voltage input	0.5V _{CC}		V _{CC}	V
V _{IA}	Analog input voltage, P ₄ ~P ₄₃	-0.3		V _{CC} +0.3	V
I _{OL(peak)}	"L" peak output current, P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₇ , AD ₀ ~AD ₇ , A ₈ ~A ₁₅ , RD, WR, φ, SYNC, ALE, WD _{OUT}			5	mA
I _{OL(avg)}	"L" average output current (Note1), P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₇ , AD ₀ ~AD ₇ , A ₈ ~A ₁₅ , RD, WR, φ, SYNC, ALE, WD _{OUT}			2	mA
I _{OH(peak)1}	"H" peak output current, P ₀ ~P ₀₇ , AD ₀ ~AD ₇ , A ₈ ~A ₁₅ , RD, WR, φ, SYNC, ALE, WD _{OUT}			-5	mA
I _{OH(peak)2}	"H" peak output current, P ₀ ~P ₀₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₇			-10	mA
I _{OH(avg)1}	"H" average output current, (Note1) P ₀ ~P ₀₇ , AD ₀ ~AD ₇ , A ₈ ~A ₁₅ , RD, WR, φ, SYNC, ALE, WD _{OUT}			-2	mA
I _{OH(avg)2}	"H" average output current, (Note1) P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₇			-10	mA

Note 1 : I_{OL(avg)}, I_{OH(avg)} is the average current in 100ms.

2 : The total of I_{OL(peak)} of P₀~P₀₇, AD₀~AD₇, A₈~A₁₅, RD, WR, φ, SYNC, ALE and WD_{OUT} should be 80mA max

The total of I_{OL(peak)} of P₁~P₁₇, P₂~P₂₇ and P₃~P₃₇ should be 80mA max

The total of I_{OH(peak)} of P₀~P₀₇, AD₀~AD₇ and A₈~A₁₅, RD, WR, φ, SYNC, ALE and WD_{OUT} should be -60mA max

The total of I_{OH(peak)} of P₁~P₁₇, P₂~P₂₇ and P₃~P₃₇ should be -80mA max



ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = -10 \sim 70^\circ C$, $f(X_{IN}) = 8MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage all output pin except X_{OUT} pin	$I_{OH} = -200\mu A$ $I_{OH} = -10\mu A$	2.4			V
V_{OL}	"H" output voltage all output pin except X_{OUT} pin	$I_{OL} = 1.6mA$			0.5	V
I_I	Input leak current, $P_0 \sim P_4$, RESET	$V_{SS} \leq V_i \leq V_{CC}$	-5		5	μA
I_{OZ}	Three state leak current, all input/output pin	$V_{SS} + 0.5V \leq V_O \leq V_{CC} - 0.5V$	-5		5	μA
$V_{T+} - V_{T-}$	Hysteresis width, INT_1 , INT_2 , CNTR, RxD , RESET	When used as function except port		0.6		V
I_{OH}	"H" output current, $P_2_0 \sim P_2_7$	$V_{OH} = 1.5V$	-1		-10	mA
I_{CC}	Supply current	During operating (Output transistors cut-off)		6	15	mA
		Wait mode (Output transistors cut-off)		1	3	mA
		Stop mode (Output transistors cut-off)		1	20	μA
I_{ACC}	A/D supply current	During executing A/D convert			6	mA

TIMING REQUIREMENTS ($V_{CC} = 5V \pm 10\%$, $T_a = -10 \sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU} (D-\phi)$	Data input set-up time	Fig.32	80			ns
$t_{SU} (P_0-\phi)$	Port P0 input set-up time		250			ns
$t_{SU} (P_1-\phi)$	Port P1 input set-up time		250			ns
$t_{SU} (P_2-\phi)$	Port P2 input set-up time		250			ns
$t_{SU} (P_3-\phi)$	Port P3 input set-up time		250			ns
$t_{SU} (P_4-\phi)$	Port P4 input set-up time		250			ns
$t_{SU} (P_1-INT_1)$	Port P1 latch input set-up time		250			ns
$t_{SU} (S_{IN}-S_{CLK})$	Serial input set-up time		250			ns
$t_h (\phi-D)$	Data input hold time		0			ns
$t_h (\phi-P_0)$	Port P0 input hold time		50			ns
$t_h (\phi-P_1)$	Port P1 input hold time		50			ns
$t_h (\phi-P_2)$	Port P2 input hold time		50			ns
$t_h (\phi-P_3)$	Port P3 input hold time		50			ns
$t_h (\phi-P_4)$	Port P4 input hold time		50			ns
$t_h (INT_1-P_1)$	Port P1 latch input hold time		50			ns
$t_h (S_{CLK}-S_{IN})$	Serial input hold time		50			ns
$t_{WL} (INT_1)$	INT_1 input "L" pulse width		250			ns
$t_{WL} (INT_2)$	INT_2 input "L" pulse width		1			μs
$t_{WL} (CNTR)$	CNTR input "L" pulse width		1			μs
$t_{WH} (INT_1)$	INT_1 input "H" pulse width		1			μs
$t_{WH} (INT_2)$	INT_2 input "H" pulse width		1			μs
$t_{WH} (CNTR)$	CNTR input "H" pulse width		1			μs
$t_C (X_{IN})$	External clock input cycle time		125			ns
$t_{WL} (X_{IN})$	External clock input "L" pulse width		45			ns
$t_{WH} (X_{IN})$	External clock input "H" pulse width		45			ns
$t_W (RESET)$	RESET input "L" pulse width		2			μs

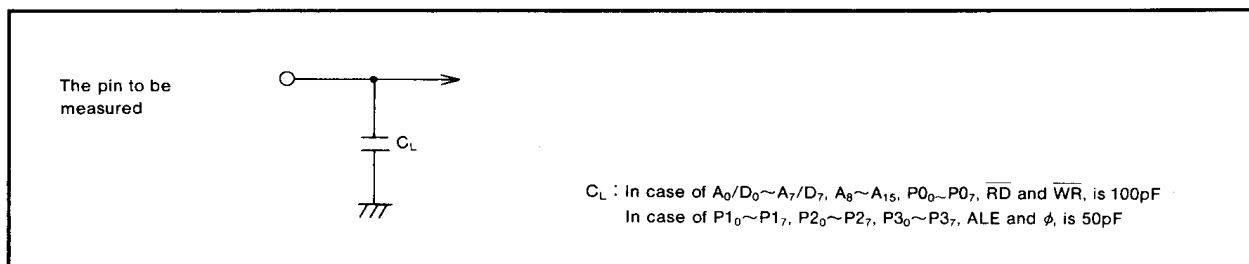


Fig.32 Measurement circuit diagram

M50734SP/FP
M50734SP/FP-10

8-BIT CMOS MICROCOMPUTER

SWITCHING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = -10 \sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
* $t_C(\phi)$	Cycle time (Note 6)	Fig.32	500			ns
* $t_{WH}(\phi)$	ϕ clock pulse width (High level) (Note 2)		220			ns
* $t_{WL}(\phi)$	ϕ clock pulse width (Low level) (Note 2)		220			ns
$t_r(\phi)$	ϕ clock rising edge time				30	ns
$t_f(\phi)$	ϕ clock falling edge time				30	ns
* $t_d(\phi-ALE)$	Address strobe pulse delay time (Note 4)				60	ns
* $t_W(ALE)$	Address strobe pulse width (Note 3)			100		ns
$t_d(A-ALE)$	Address-ALE delay time			30		ns
$t_V(ALE-A)$	Address effective time after ALE			30		ns
$t_{d1}(\phi-A)$	Address delay time 1				130	ns
* $t_{d2}(\phi-A)$	Address delay time 2 (Note 1)				150	ns
$t_V(\phi-A)$	Address effective time after ϕ			10		ns
* $t_W(RD)$	\overline{RD} , \overline{WR} pulse width (Note 2)			220		ns
$t_d(\phi-RD)$	\overline{RD} , \overline{WR} delay time				20	ns
$t_V(\phi-RD)$	\overline{RD} , \overline{WR} effective time after ϕ				10	ns
$t_d(AZ-RD)$	address floating- \overline{RD} delay time			0		ns
$t_d(\phi-D)$	Data delay time (write cycle)				150	ns
* $t_V(\phi-D)$	Data effective time after ϕ (Note 5)			40		ns
$t_d(\phi-P0)$	Port P0 data output delay time				250	ns
$t_d(\phi-P1)$	Port P1 data output delay time				250	ns
$t_d(\phi-P2)$	Port P2 data output delay time				250	ns
$t_d(\phi-P3)$	Port P3 data output delay time				250	ns
$t_d(\phi-SCLK)$	Serial clock delay time				60	ns
$t_V(\phi-SCLK)$	Serial clock effective time after ϕ				40	ns
$t_d(SCLK-SOUT)$	Serial output delay time				150	ns
$t_V(SCLK-SOUT)$	Serial output effective time after serial clock			0		ns
$t_d(INT1-BSY)$	Busy output delay time				250	ns

* This timing is changed by $t_C(X_{IN})$. The timing of this list is the value in $t_C(X_{IN}) = 125ns$

- Note 1 : This value is defined as follows : $t_{d2}(\phi-A) = t_C(\phi)/8 + 8.75$
 2 : This value is defined as follows : $t_W(RD) = t_C(\phi)/2 - 30$
 3 : This value is defined as follows : $t_W(ALE) = t_C(\phi)/4 - 25$
 4 : This value is defined as follows : $t_d(\phi-ALE) = t_C(\phi)/8 - 2.5$
 5 : This value is defined as follows : $t_V(\phi-D) = t_C(\phi)/8 - 22.5$
 6 : This value is defined as follows : $t_C(\phi) = 4t_C(X_{IN})$

A-D CONVERTER CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = -10 \sim 70^\circ C$, $f(X_{IN}) = 8MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution		8			Bits
—	Absolute accuracy	$V_{CC} = V_{REF} = 5.12V$		$\pm 1 \frac{1}{2}$	± 3	LSB
R_{LADDER}	Ladder resistance value		1			$K\Omega$
t_{CONV}	Conversion time				36	μs
$I_{I(AD)}$	Input current in A-D convert	$0 \leq V_I \leq V_{REF}$			50	μA

