National Semiconductor

MILITARY DATA SHEET

MN54F74-X REV 1A0

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DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

General Description

The F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary ($Q/\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse Input threshold voltage has been passed, the Data inputs is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

LOW Input to $\overline{S}d$ sets Q to HIGH level

LOW Input to $\overline{C}d$ sets Q to LOW level

Clear and Set are Independent of clock

Simultaneous LOW on $\overline{C}d$ and $\overline{S}d$ makes both Q and Q HIGH

Industry Part Number

54F74

NS Part Numbers

54F74DMQB
54F74FMQB
54F74LMQB

Prime Die

M074

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Guaranteed 4000V minimum ESD protection

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature	-65 C to +150 C
Ambient Temperature under Bias	-55 C to +125 C
Junction Temperature under Bias	-55 C to +175 C
Vcc Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0mA
Voltage Applied to Output in HIGH State (with Vcc=0V)	
Standard Output	-0.5V to Vcc
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated Iol(mA)
ESD Last Passing VOltage (Min)	4000V

Note 1: Absolute Maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these condtions is not implied.
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0 C to +70 C
Military	-55 C to +125 C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

Electrical Characteristics

DC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, Temp range: -55C to 125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input High Current	VCC=5.5V, VM=2.7V, VINH=5.5V, VINL=0.0V	1, 3	INPUTS		20	uA	1, 2, 3
IBVI	Input High Current	VCC=5.5V, VM=7.0V, VINH=5.5V, VINL=0.0V	1, 3	INPUTS		100	uA	1, 2, 3
IIL	Input LOW Current	VCC=5.5V, VM=0.5V, VINH=5.5V, VINL=0.0V	1, 3	D, CP		-0.6	mA	1, 2, 3
IIL3	Input LOW Current	VCC=5.5V, VM=0.5V, VINH=5.5V, VINL=0.0V	1, 3	CLR/SET		-1.8	mA	1, 2, 3
VOL	Output LOW Voltage	VCC=4.5V, VIH=2.0V, IOL=20mA, VINH=5.5V, VIL=0.8V	1, 3	OUTPUTS		0.5	V	1, 2, 3
VOH	Output HIGH Voltage	VCC=4.5V, VIL=0.8V, IOH=-1.0mA, VINH=5.0V, VIH=2.0V	1, 3	OUTPUTS	2.5		V	1, 2, 3
IOS	Short Circuit Current	VCC=5.5V, VINH=5.5V, VM=0.0V, VINL=0.0V	1, 3	OUTPUTS	-60	-150	mA	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IM=-18mA, VINH=5.5V	1, 3	INPUTS		-1.2	V	1, 2, 3
ICC	Supply Current	VCC=5.5V, VINL=0.0V, VINH=5.5V	1, 3	VCC		16	mA	1, 2, 3
ICEX	Output HIGH Leakage Current	VCC=5.5V, VINL=0.0V, VINH=5.5V, VM=5.5V	1, 3	OUTPUTS		250	uA	1, 2, 3

Electrical Characteristics

AC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pf, RL=500 OHMS, TR=2.5ns, TF=2.5ns SEE AC FIGS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH(1)	Propagation Delay	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C	2, 4	CPn to Q/$\overline{Q}$	3.8	6.8	ns	9
			2, 4	CPn to Q/$\overline{Q}$	3.8	8.5	ns	10, 11
tpHL(1)	Propagation Delay	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C	2, 4	CPn to Q/$\overline{Q}$	4.4	8.0	ns	9
			2, 4	CPn to Q/$\overline{Q}$	4.4	10.5	ns	10, 11
tpLH(2)	Propagation Delay $\overline{CD}$ or $\overline{SD}$ to Q/$\overline{Q}$	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C	2, 4		3.2	6.1	ns	9
tpLH(2)	Propagation Delay $\overline{CD}$ or $\overline{SD}$ to Q/$\overline{Q}$	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C	2, 4		3.2	8.0	ns	10, 11
tpHL(2)	Propagation Delay $\overline{CD}$ or $\overline{SD}$ to Q/$\overline{Q}$	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C	2, 4		3.5	9.0	ns	9
tpHL(2)	Propagation Delay $\overline{CD}$ or $\overline{SD}$ to Q/$\overline{Q}$	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C	2, 4		3.5	11.5	ns	10, 11
ts(H)	Setup Time (High)	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C	5	Dn to CPn	2.0		ns	9
			5	Dn to CPn	3.0		ns	10, 11
ts(L)	Setup Time (Low)	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C	5	Dn to CPn	3.0		ns	9
			5	Dn to CPn	4.0		ns	10, 11
th(H/L)	Hold Time (High or Low)	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C	5	Dn to CPn	1.0		ns	9
			5	Dn to CPn	2.0		ns	10, 11
tREC	Recovery Time $\overline{CD}$n or $\overline{SD}$n to CP	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C	5		2.0		ns	9
tREC	Recovery Time $\overline{CD}$n or $\overline{SD}$n to CP	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C	5		3.0		ns	10, 11
tw(L)	Pulse Width	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C, TR/TF=1.0ns	5	$\overline{CD}$n or $\overline{SD}$	4.0		ns	9, 10, 11
tw(H)	Pulse Width (High)	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C, TR/TF=1.0ns	5	CPn	4.0		ns	9, 10, 11
tw (L)	Pulse Width (Low)	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C, TR/TF=1.0ns	5	CPn	5.0		ns	9
			5	CPn	6.0		ns	10, 11
fMAX	Maximum Clock Frequency	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C, TR/TF=1.0ns	5		100		MHz	9
			5		80		MHZ	10, 11

Note 1: Screen tested 100% on each device at +25C, +125C & -55C temperature, subgroups A1, 2, 3, 7 & 8.
Note 2: Screen tested 100% on each device at +25C temperature only, subgroup A9.
Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C & -55C temperature, subgroups A1, 2, 3, 7 & 8.
Note 4: Sample tested (Method 5005, Table 1) at +25C subgroup A9, and periodically at +125C & -55C temperature, subgroups 10 & 11.
Note 5: Guaranteed but not tested. (Design characterization data).

National Semiconductor was acquired by Texas Instruments.

http://www.ti.com/corp/docs/investor_relations/pr_09_23_2011_national_semiconductor.html

This file is the datasheet for the following electronic components:

JM38510/34101BDA - http://www.ti.com/product/jm38510/34101bda?HQS=TI-null-null-dscatalog-df-pf-null-wwe

JM38510/34101SCA - http://www.ti.com/product/jm38510/34101sca?HQS=TI-null-null-dscatalog-df-pf-null-wwe

54F74DMQB - http://www.ti.com/product/54f74dmqb?HQS=TI-null-null-dscatalog-df-pf-null-wwe

JM38510/34101SDA - http://www.ti.com/product/jm38510/34101sda?HQS=TI-null-null-dscatalog-df-pf-null-wwe

54F74FMQB - http://www.ti.com/product/54f74fmqb?HQS=TI-null-null-dscatalog-df-pf-null-wwe

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