

**MNDS16F95-X-RH REV 0A1**

 Original Creation Date: 01/26/96  
 Last Update Date: 04/29/99  
 Last Major Revision Date: 01/26/96

**DIFFERENTIAL BUS TRANSCEIVER, ALSO AVAILABLE  
 GUARANTEED TO 300K RAD (Si) TESTED TO MIL-STD-883  
 METHOD 1019.**

**General Description**

The DS16F95 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on balanced multipoint bus transmission lines. The Transceiver meets EIA standard RS-485 as well as RS-422A.

The DS16F95 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS16F95 features lower power, extended temperature range, and improved specifications.

The DS16F95 combines a TRI-STATE differential input line receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active Enable that can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or when Vcc = 0V. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive and negative current-limiting and thermal shutdown for protection from line fault conditions.

The DS16F95 can be used in transmission line applications employing the DS96F172 and DS96F174 quad differential line drivers and the DS96F173 and DS96F175 quad differential line receivers.

**Industry Part Number**

DS16F95

**Prime Die**

M176

**Controlling Document**

SEE FEATURES PAGE

**NS Part Numbers**

 DS16F95E/883  
 DS16F95J-QMLV  
 DS16F95J/883  
 DS16F95JFQML  
 DS16F95JFQMLV  
 DS16F95W-QMLV  
 DS16F95W-SMD  
 DS16F95W/883  
 DS16F95WFQML  
 DS16F95WFQMLV  
 DS16F95WG-QMLV  
 DS16F95WG/883  
 DS16F95WGFQML  
 DS16F95WGFQMLV

**Processing**

MIL-STD-883, Method 5004

**Quality Conformance Inspection**

MIL-STD-883, Method 5005

**Subgrp Description**
**Temp ( °C)**

1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

**Features**

- Meets EIA Standard RS-422A and RS-485
- Meets SCSI specifications
- Designed for multipoint transmission
- Wide positive and negative input/output bus voltage ranges
- Thermal shutdown protection
- Driver positive and negative current-limiting
- High impedance receiver input
- Receiver input hysteresis of 50mV typical
- Operates from single 5.0V supply
- Low power 28mA max
- Pin compatible with DS3695 and SN75176A
- CONTROLLING DOCUMENT

DS16F95E/883	5962-89615012A
DS16F95J/883	5962-8961501PA
DS16F95J-QMLV	5962-8961501VPA
DS16F95JFQML	5962F8961501QPA
DS16F95JFQMLV	5962F8961501VPA
DS16F95W-SMD	5962-8961501HA
DS16F95W/883	
DS16F95W-QMLV	5962-8961501VHA
DS16F95WFQML	5962F8961501QHA
DS16F95WFQMLV	5962F8961501VHA
DS16F95WG/883	5962-8961501QXA
DS16F95WG-QMLV	5962-8961501VXA
DS16F95WGFQML	5962F8961501QXA
DS16F95WGFQMLV	5962F8961501VXA

**(Absolute Maximum Ratings)**

(Note 1)

Storage Temperature Range Ceramic DIP	-65 C to +175 C
Lead Temperature Ceramic DIP (Soldering, 60 sec.)	300 C
Maximum Power Dissipation at 25 C (Note 2)	
Ceramic J Package	1274mW
Ceramic E Package	1800mW
Ceramic W & WG Packages	725mW
Supply Voltage	7.0V
Differential Input Voltage	+15V/-10V
Enable Input Voltage	5.5V
Thermal Resistance	
ThetaJA	
8 pin Cerdip (J pkg)	118 C/W @ 1.0W
20 pin LCC (E pkg)	83 C/W @ 0.5W
10 pin Cerpak (W pkg)	207 C/W @ 0.5W
Ceramic SOIC (WG pkg)	207 C/W @ 0.5W
ThetaJC	
8 pin Cerdip (J pkg)	14 C/W
20 pin LCC (E pkg)	17 C/W
10 pin Cerpak (W pkg)	18 C/W
Ceramic SOIC (WG pkg)	18 C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: \*Derate J package 8.5mW/C above +25C. \*Derate E package 12.1mW/C above +25C.  
\*Derate W & WG packages 4.8mW/C above +25C.

**Recommended Operating Conditions**

Supply Voltage (Vcc)	Min.	Typ.	Max.	Units
	4.5	5.0	5.50	V
Voltage at Any Bus Terminal (Separately or Common Mode) (Vi or Vcm)	Min.	Typ.	Max.	Units
	-7.0		12	V
Differential Input Voltage (Vid)	Min.	Typ.	Max.	Units
	-7.0		±12	V
Output Current HIGH (Ioh)	Min.	Typ.	Max.	Units
Driver			-60	mA
Receiver			-400	uA
Output Current LOW (Iol)	Min.	Typ.	Max.	Units
Driver			60	mA
Receiver			16	mA
Operating Temperature (TA)	Min.	Typ.	Max.	Units
	-55	+25	+125	C

## Electrical Characteristics

### DC PARAMETERS: DRIVER (See Note 7)

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $V_{cc} = 5.5V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vod1	Differential Vout	$V_{cc} = 5.5V, I_o = 0A, V_{in} = .8V$				6	V	1, 2, 3
		$V_{cc} = 5.5V, I_o = 0A, V_{in} = 2V$				6	V	1, 2, 3
Vod2	Differential Vout	$V_{cc} = 4.5V, R_L = 100 \text{ Ohms}$			2		V	1, 2, 3
		$V_{cc} = 4.5V, R_L = 54 \text{ Ohms}$			1.5		V	1, 2, 3
Delta Vod	Change In Differential Vout	$V_{cc} = 4.5V, R_L = 100 \text{ Ohms}$	1		-200	200	mV	1, 2, 3
		$V_{cc} = 4.5V, R_L = 54 \text{ Ohms}$	1		-200	200	mV	1, 2, 3
Delta Voc	Change In Common Mode Vout	$V_{cc} = 4.5V, R_L = 100 \text{ Ohms}$	1		-200	200	mV	1, 2, 3
		$V_{cc} = 4.5V, R_L = 54 \text{ Ohms}$	1		-200	200	mV	1, 2, 3
Voc	Common Mode Vout	$R_L = 100 \text{ Ohms}$				3	V	1, 2, 3
		$R_L = 54 \text{ Ohms}$				3	V	1, 2, 3
Iih	Logical "1" Input Current	$V_i = 2.4V$				20	$\mu A$	1, 2, 3
Io	Output Current	Output Disable, $V_o = 12V$				1	mA	1, 2, 3
		Output Disable, $V_o = -7V$	2		-0.8		mA	1, 2, 3
		$V_{cc} = 0, \text{ Output Disable, } V_o = 12V$				1	mA	1, 2, 3
		$V_{cc} = 0, \text{ Output Disable, } V_o = -7V$	2		-0.8		mA	1, 2, 3

## Electrical Characteristics

### DC PARAMETERS: DRIVER (See Note 7) (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $V_{cc} = 5.5V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ios	Output Short Circuit	$V_{in} = 3V, V_{out} = V_{cc}$				150	mA	1, 2, 3
		$V_{in} = 3V, V_{out} = -7V$	2		-250		mA	1, 2, 3
		$V_{in} = 3V, V_{out} = 0V$	2		-150		mA	1, 2, 3
		$V_{in} = 3V, V_{out} = 12V$				250	mA	1, 2, 3
		$V_{in} = 0V, V_{out} = 12V$				250	mA	1, 2, 3
		$V_{in} = 0V, V_{out} = V_{cc}$				150	mA	1, 2, 3
		$V_{in} = 0V, V_{out} = -7V$	2		-250		mA	1, 2, 3
		$V_{in} = 0V, V_{out} = 0V$	2		-150		mA	1, 2, 3
Voh	Logical "1" Output Voltage	$V_{cc} = 4.5V, I_o = -20mA$			3		V	1, 2, 3
Vol	Logical "0" Output Voltage	$V_{cc} = 4.5V, I_o = 20mA$				2	V	1, 2, 3
Vod3	Differential Vout	$V_{cm} = -7V \text{ to } 12V$			1		V	1, 2, 3

## Electrical Characteristics

### DC PARAMETERS: RECEIVER (See NOTE 7)

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $V_{cc} = 5.5V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Voh	Logical "1" Output Voltage	$V_{cc} = 4.5V, V_{id} = 200mV, I_{oh} = -400\mu A$			2.5		V	1, 2, 3
Vol	Logical "0" Output Voltage	$V_{cc} = 4.5V, V_{id} = -200mV, I_{ol} = 8mA$				.45	V	1, 2, 3
		$V_{cc} = 4.5V, V_{id} = -200mV, I_{ol} = 16mA$				.5	V	1, 2, 3
Ii	Line Input Current	Untested Input = 0V, $V_i = 12V$				1	mA	1, 2, 3
		Untested Input = 0V, $V_i = -7V$	2		-.8		mA	1, 2, 3
		$V_{cc} = 0V$ , Untested Input = 0V, $V_i = 12V$	2			1	mA	1, 2, 3
		$V_{cc} = 0V$ , Untested Input = 0V, $V_i = -7V$			-.8		mA	1, 2, 3
Iih	Logical "1" Input Current	$V_i = 2.7V$ (Receiver)				20	$\mu A$	1, 2, 3
Rin	Input Resistance	Untested Input = 0V, $V_i = 12V$	3		10		K Ohms	1, 2, 3
		Untested Input = 0V, $V_i = -7V$	3		10		K Ohms	1, 2, 3
		$V_{cc} = 0V$ , Untested Input = 0V, $V_i = 12V$	3		10		K Ohms	1, 2, 3
		$V_{cc} = 0V$ , Untested Input = 0V, $V_i = -7V$	3		10		K Ohms	1, 2, 3
Ioz	High Impedance State	$V_i = .4V$			-20	20	$\mu A$	1, 2, 3
		$V_i = 2.4V$			-20	20	$\mu A$	1, 2, 3
Ios	Output Short Circuit	$V_{in} = 1V, V_{out} = 0V$			-85	-15	mA	1, 2, 3
Vth	Differential Input High Threshold	$V_{cc} = 4.5V, V_o = 2.5V, V_{cm} = 12V \& 0V \& -7V, I_o = -.4mA$				.2	V	1, 2, 3
		$V_{cc} = 5.5V, V_o = 2.5V, V_{cm} = 12V \& 0V \& -7V, I_o = -.4mA$				.2	V	1, 2, 3
Vtl	Differential Input Low Threshold	$V_{cc} = 4.5V, V_o = .5V, V_{cm} = 12V \& 0V \& -7V, I_o = 8mA$			-.2		V	1, 2, 3
		$V_{cc} = 5.5V, V_o = .5V, V_{cm} = 12V \& 0V \& -7V, I_o = 8mA$			-.2		V	1, 2, 3

## Electrical Characteristics

### DC PARAMETERS: RECEIVER (See NOTE 7) (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $V_{cc} = 5.5V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
V <sub>th+</sub> - (V <sub>th-</sub> )	Hysteresis	$V_{cc} = 4.5V, V_{cm} = 0V$			35		mV	1, 2, 3
		$V_{cc} = 5.5V, V_{cm} = 0V$			35		mV	1, 2, 3

### DC PARAMETERS: BOTH DRIVER AND RECEIVER (See NOTE 7)

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $V_{cc} = 5.5V$

I <sub>cc</sub>	Supply Current I <sub>cc</sub> Both Disable	$R_e = 2V, D_e = .8V$				25	mA	1, 2, 3
I <sub>cc</sub>	Supply Current I <sub>cc</sub> Both Enable	$R_e = .8V, D_e = 2V$				28	mA	1, 2, 3
V <sub>ic</sub>	Input Clamp Volt	$I_i = -18mA$			-1.3		V	1, 2, 3
V <sub>ih</sub>	Logical "1" Input Voltage				2		V	1, 2, 3
V <sub>il</sub>	Logical "0" Input Voltage					.8	V	1, 2, 3
V <sub>ih</sub>	Logical "1" Enable Input Voltage				2		V	1, 2, 3
V <sub>il</sub>	Logical "0" Enable Input Voltage					.8	V	1, 2, 3
I <sub>il</sub>	Logical "0" Input Current	$V_i = .4V$	2		-50		uA	1, 2, 3

## Electrical Characteristics

### AC PARAMETERS: DRIVER (See NOTE 7)

(The following conditions apply to all the following parameters, unless otherwise specified.)  
 AC:  $V_{cc} = 5V$ ,  $PRR = 1MHz$ ,  $T_r \leq T_f \leq 6nS$ , 50% duty cycle,  $AMP = 3V$ ,  $V_{Lo} = 0V$ ,  $Z_{out} = 50\ \Omega$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tdd	Differential Output Delay Time	RL = 60 Ohms	6		8	25	nS	9
			6		8	30	nS	10, 11
tTD	Differential Output Transition Time	RL = 60 Ohms	5, 6		8	25	nS	9
			5, 6		8	30	nS	10, 11
tPLH	Propagation Delay Time Low to High	RL = 27 Ohms			6	18	nS	9
					6	25	nS	10, 11
tPHL	Propagation Delay Time high to Low	RL = 27 Ohms			6	18	nS	9
					6	25	nS	10, 11
tPZH	Output Enable Time to H	RL = 110 Ohms				35	nS	9
						45	nS	10, 11
tPZL	Output Enable Time to L	RL = 110 Ohms				40	nS	9
						50	nS	10, 11
tPHZ	Output Disable Time to H	RL = 110 Ohms				30	nS	9
						40	nS	10, 11
tPLZ	Output Disable Time to L	RL = 110 Ohms				30	nS	9
						40	nS	10, 11
Tskew	Differential Output Skew Time					6	nS	9
						12	nS	10, 11

## Electrical Characteristics

### AC PARAMETERS: RECEIVER (See NOTE 7)

(The following conditions apply to all the following parameters, unless otherwise specified.)  
 AC:  $V_{cc} = 5V$ ,  $PRR = 1MHz$ ,  $T_r \leq T_f \leq 6nS$ , 50% duty cycle,  $AMP = 3V$ ,  $V_{Lo} = 0V$ ,  $Z_{out} = 50\ \Omega$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPLH	Propagation Delay Time Low to High	Cl = 15pF			10	27	nS	9
					10	38	nS	10, 11
tPHL	Propagation Delay Time High to Low	Cl = 15pF			10	27	nS	9
					10	38	nS	10, 11
tPZH	Output Enable Time to H	Cl = 15pF				20	nS	9
						30	nS	10, 11
tPZL	Output Enable Time to L	Cl = 15pF				20	nS	9
						30	nS	10, 11
tPLH - tPHL	Output to Output Delay Time					8	nS	9
						16	nS	10, 11
tPHZ	Output Disable Time From H	Cl = 20pF	4			30	nS	9
			4			40	nS	10, 11
		Cl = 5pF	4			20	nS	9
			4			30	nS	10, 11
tPLZ	Output Disable Time From L	Cl = 5pF				20	nS	9
						30	nS	10, 11

Note 1:  $\Delta V_{od}$  and  $\Delta V_{oc}$  are the changes in magnitude of  $V_{od}$  and  $V_{oc}$ .

Note 2: Negative sign of the limits indicates the direction of the current flow only.

Note 3: Rin is guaranteed by testing "Line Input Current" (II).

Note 4: Testing at 20pF assures conformance to spec at 5pF.

Note 5:  $t_{TD} = \text{Non-inverting output rise time} + \text{inverting output fall time} / 2$ ,  $\text{Non-inverting output fall time} + \text{inverting output rise time} / 2$ .

Note 6: Rise time 20% to 80%, Fall time 80% to 20%

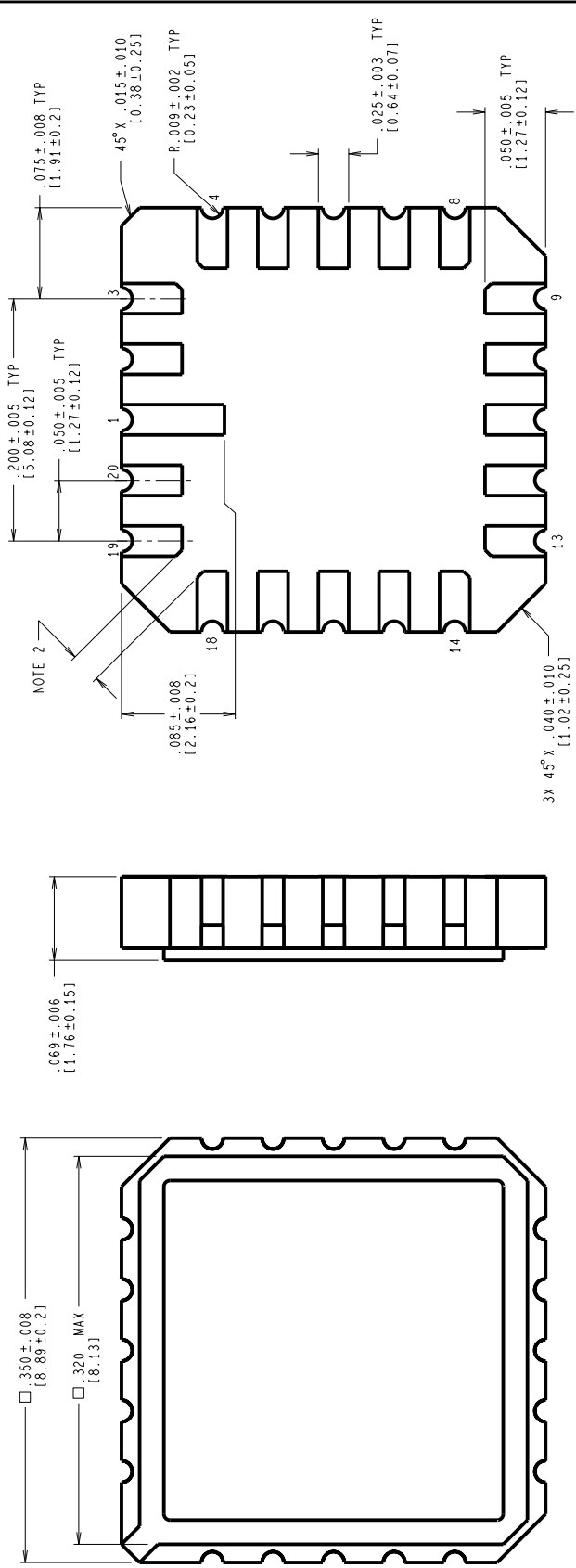
Note 7: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD 883, Method 1019.5, condition A.

## Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06070HRA2	LCC (E), TYPE C, 20 TERMINAL (B/I CKT)
06140HRA2	CERDIP (J), 8 LEAD (B/I CKT)
06141HRA2	CERPACK (W), 10 LEAD (B/I CKT)
06186HRA2	CERDIP (J), 8 LEAD (B/I CKT)
06187HRA2	CERPACK (W), 10 LEAD (B/I CKT)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000356B	CERAMIC SOIC (WG), 10 LEAD (PINOUT)
P000433A	CERDIP (J), 8 LEAD (PINOUT)
P000434A	LCC (E), TYPE C, 20 TERMINAL (PINOUT)
W10ARG	CERPACK (W), 10 LEAD (P/P DWG)
WG10ARC	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
E	REVISE AND REDRAW	10005	02/10/94 DEG/



- NOTES: UNLESS OTHERWISE SPECIFIED.
- LEAD FINISH TO BE ONE OF THE FOLLOWING:
    - 50 MICRONS/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICRONS/1.27-8.89 MICROMETERS NICKEL.
    - SOLDER DIP.
      - SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.
    - CORNER PADS MAY HAVE A  $45^\circ$  X  $0.20$  IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE  $0.015$  IN/0.38mm DIMENSION.
    - REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

CONTROLLING DIMENSION IS INCH  
VALUES IN [ ] ARE MILLIMETERS

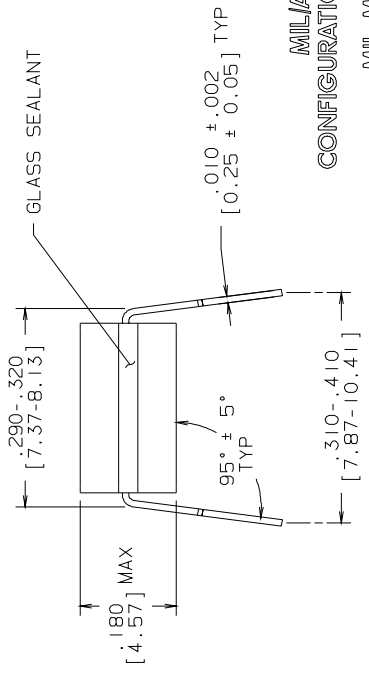
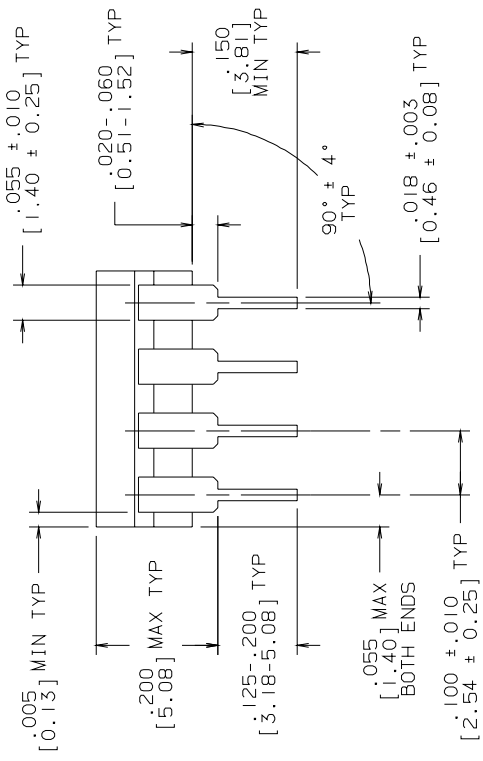
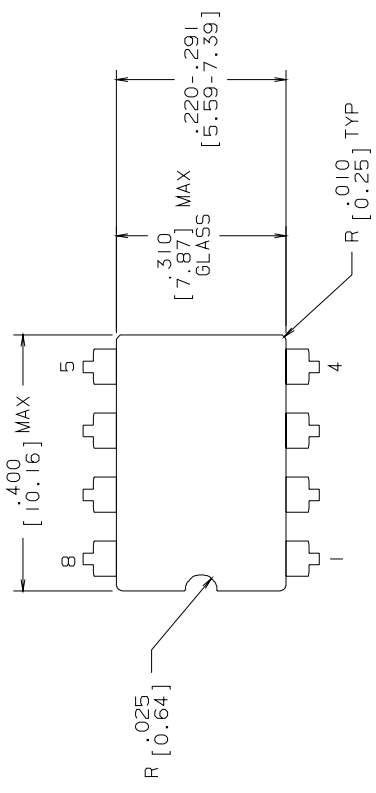
MIL/AERO  
CONFIGURATION CONTROL

APPROVALS		DATE
DRN	<i>Deane Gedy</i>	02/10/94
DTG - CHK.		
ENGR - CHK.		
APPROVAL		

NATIONAL SEMICONDUCTOR CORPORATION		2300 Semiconductor Drive, Santa Clara, Ca. 95052-8000	
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL			
SCALE	SIZE	DRAWING NUMBER	REV.
N/A	C	MKT-E20A	E
DO NOT SCALE DRAWING			SHEET 1 of 1

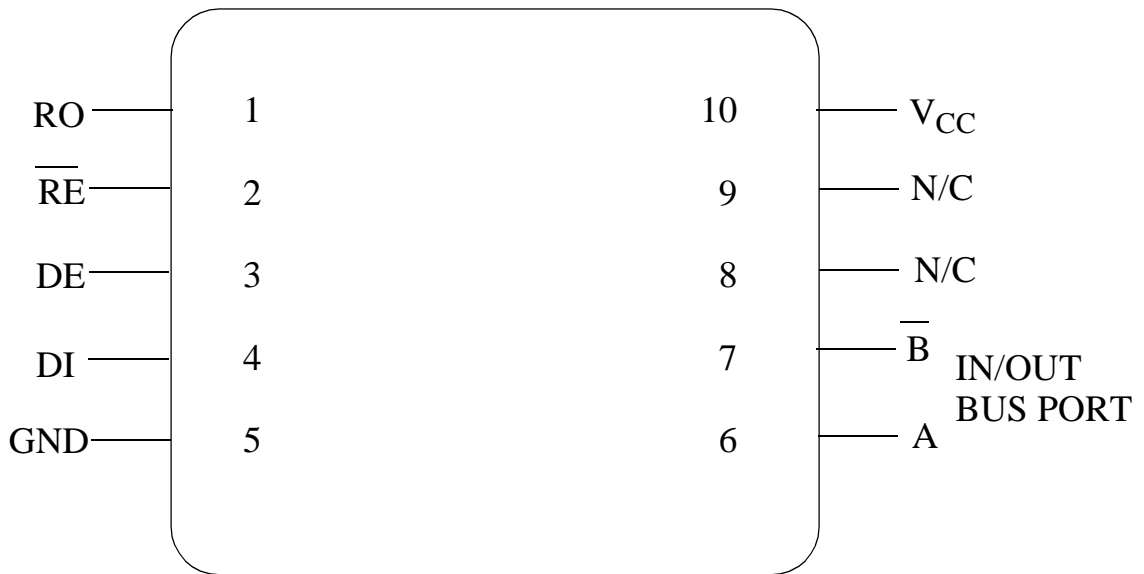
R E V I S I O N S			
LTR	DESCRIPTION	E. C. N.	DATE
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93
			BY/APP'D TL/



MILAERO  
CONFIGURATION CONTROL  
MIL-M-38510  
CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH	
APPROVALS	DATE
DRAWN <b>T. LEQUANG</b>	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	
 INCH [MM]	
SCALE	DRAWING NUMBER
N/A	B MKT-J08A
DO NOT SCALE DRAWING	SHEET 1 OF 1
NATIONAL SEMICONDUCTOR CORPORATION 2900 Semiconductor Drive, Santa Clara, CA 95052-8090	
CERDIP (J), 8 LEAD	
REV	L

- NOTES: UNLESS OTHERWISE SPECIFIED
- LEAD FINISH TO BE 200 MICROMETERS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
  - JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

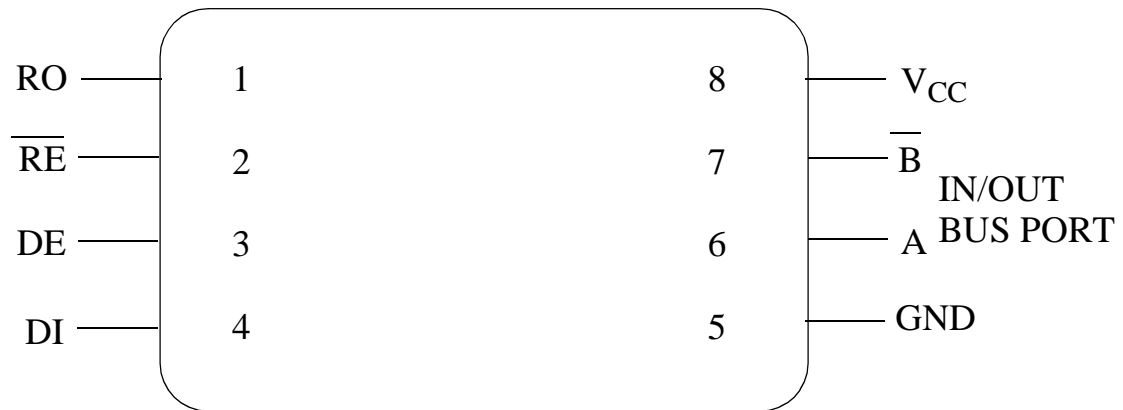


**DS16F95WG/W**  
**10 - LEAD CERAMIC SOIC**  
**CONNECTION DIAGRAM**  
**TOP VIEW**  
**P000356B**



National Semiconductor™

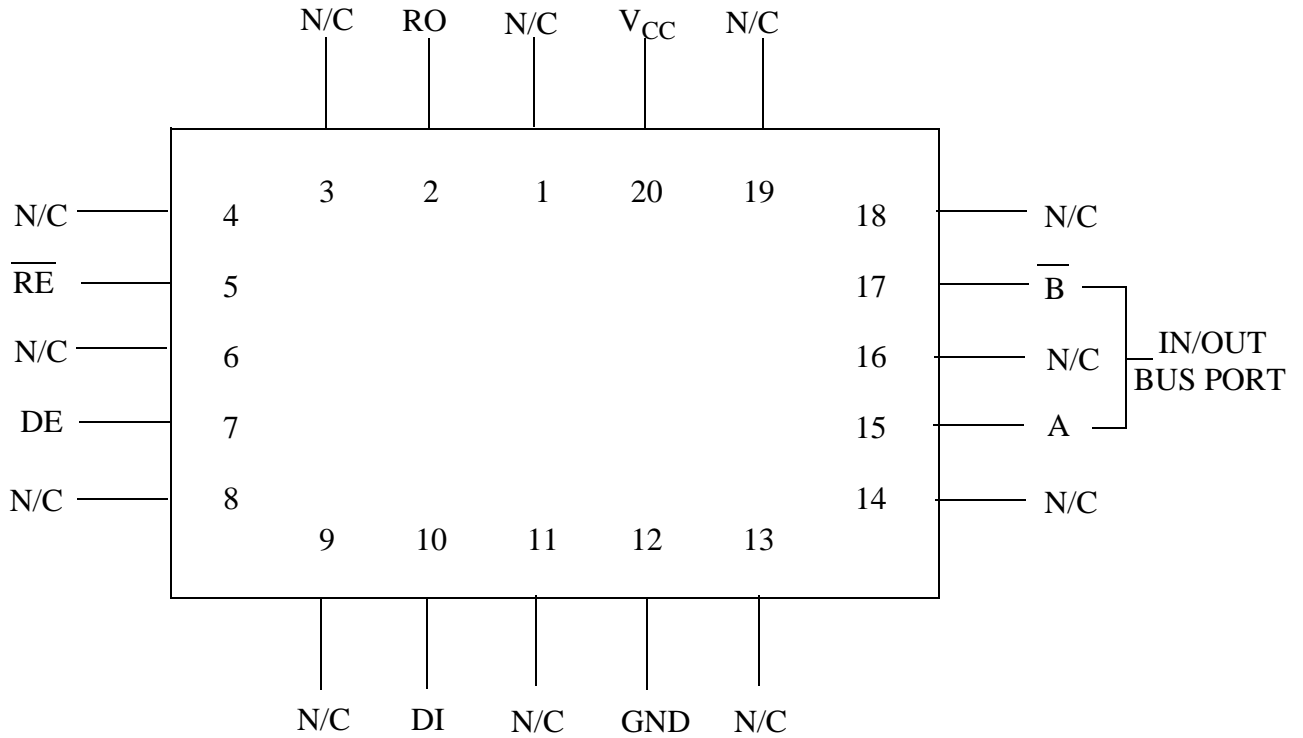
MIL/AEROSPACE OPERATIONS  
 2900 SEMICONDUCTOR DRIVE  
 SANTA CLARA, CA 95050



DS16F95J  
8 - LEAD DIP  
CONNECTION DIAGRAM  
TOP VIEW  
P000433A

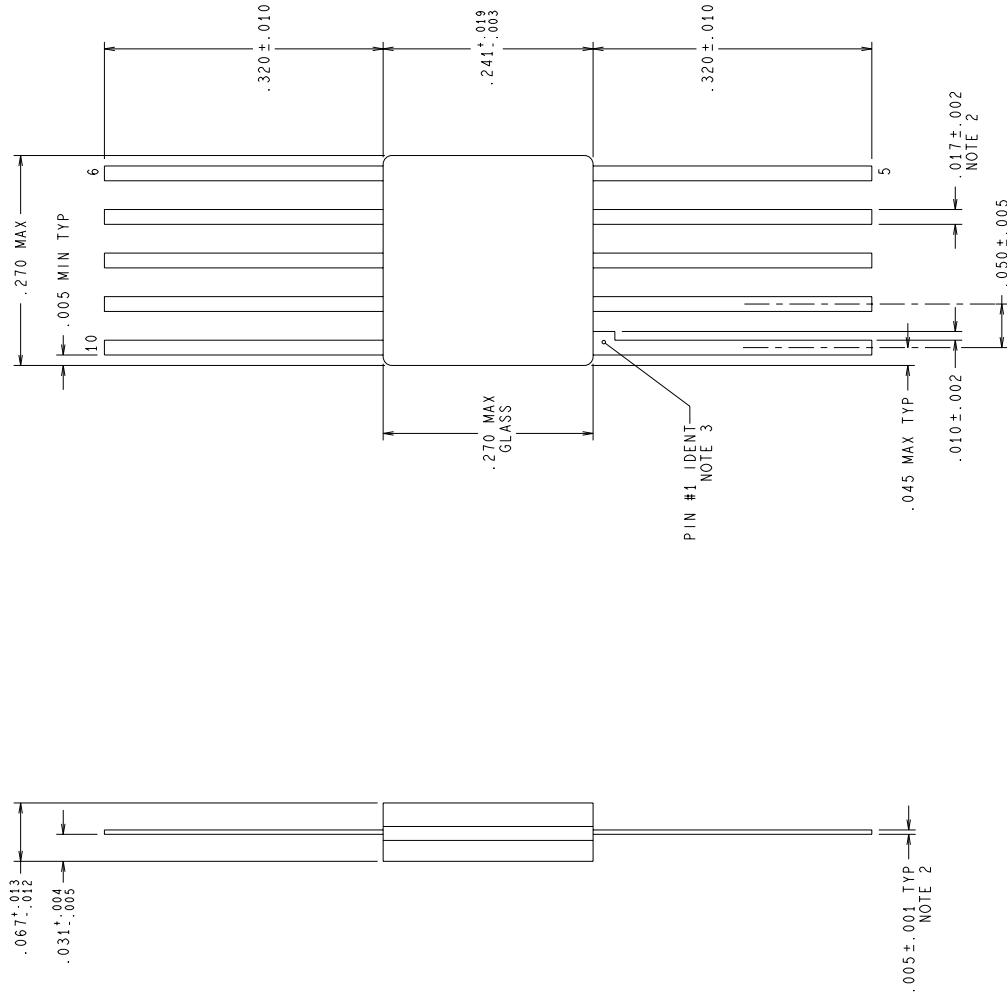


National Semiconductor™  
MIL/AEROSPACE OPERATIONS  
2900 SEMICONDUCTOR DRIVE  
SANTA CLARA, CA 95050



**DS16F95E**  
**20 - LEAD LCC**  
**CONNECTION DIAGRAM**  
**TOP VIEW**  
**P000434A**

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
F	REVISE AND REDRAW PER NEW STANDARD.	10510	07/28/94 DEG/AEP
G	.017±.002 WAS .017±.020.	10654	10/21/94 DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
- MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
- LEAD 1 IDENTIFICATION SHALL BE:
  - A NOTCH OR OTHER MARK WITHIN THIS AREA
  - A TAB ON LEAD 1, EITHER SIDE
- REFERENCE JEDEC REGISTRATION M0-003, VARIATION AG, DATED 06/01/76.

MIL/AERO  
CONFIGURATION CONTROL

MIL-M-38510  
CONFIGURATION CONTROL

APPROVALS		DATE	
DRWN	<i>D. F. Grady</i>		07/28/94
DTG. CHK.			
ENGR. CHK.			

PROJECTION			
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W10A	G

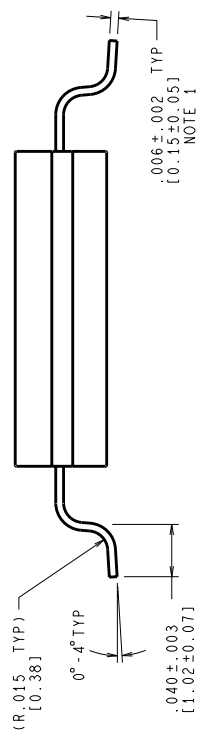
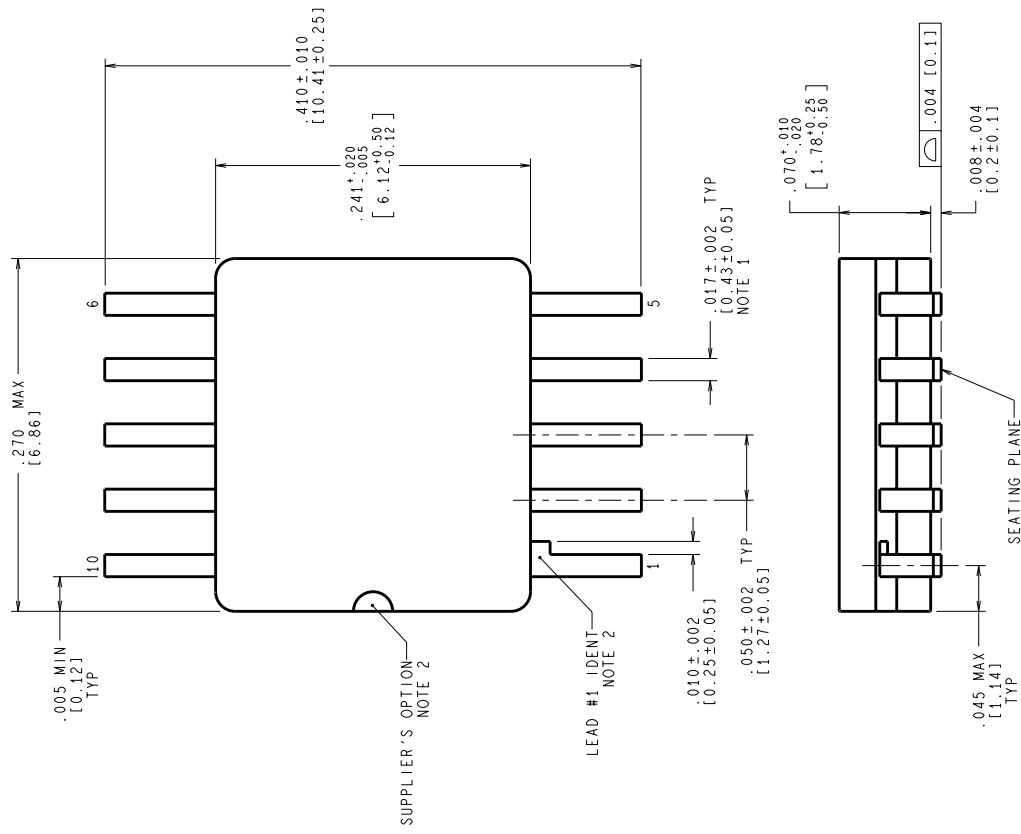
DO NOT SCALE DRAWING SHEET 1 of 1

**National Semiconductor**  
2800 Semiconductor dr., Santa Clara, CA 95052-8090

CERPACK, 10 LEAD

REVISIONS

LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM. .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015(0.38) WAS R .006(0.15)	11838	10/08/1997	TL/



CONTROLLING DIMENSION IS INCH  
VALUES IN | ARE MILLIMETERS

MIL-PRF-38535  
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICRONS/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
- LEAD 1 IDENTIFICATION SHALL BE:
  - A NOTCH OR OTHER MARK WITHIN THIS AREA
  - A TAB ON LEAD 1, EITHER SIDE
- NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

APPROVALS	DATE	SCALE	SIZE	DRAWING NUMBER	REV
DRN: MARYA SUCHY	02/29/96	N/A	C	(SC)MKT-WG10A	C
DATE: 02/29/96					
ENGR. CHK.					
NATIONAL SEMICONDUCTOR 2800 Semiconductor Dr., Santa Clara, CA 95052-8090					
CERPACK, 10 LEAD, GULL WING					
DO NOT SCALE DRAWING SHEET 1 of 1					

**Revision History**

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003240	04/29/99	Linda Collins	Renamed MDS: MND16F95-X Rev. 0A0 to MND16F95-X-RH, Rev. 0A0. Added new NSPN's for WG package, RHA and QMLV. Added Marketing DWG and Pinout for WG package. Updated Thermal Resistance and Max Power Dissipation ratings for all packages.
0A1	M0003374	04/29/99	Rose Malone	Update MDS: MND16F95-X-RH, Rev. 0A0 to MND16F95-X-RH, Rev. 0A1. Added Pin Out graphics and B/I ckts for all packages.

# National Semiconductor was acquired by Texas Instruments.

[http://www.ti.com/corp/docs/investor\\_relations/pr\\_09\\_23\\_2011\\_national\\_semiconductor.html](http://www.ti.com/corp/docs/investor_relations/pr_09_23_2011_national_semiconductor.html)

This file is the datasheet for the following electronic components:

DS16F95W/883 - <http://www.ti.com/product/ds16f95w/883?HQS=TI-null-null-dscatalog-df-pf-null-wwe>  
5962-8961501HA - <http://www.ti.com/product/5962-8961501ha?HQS=TI-null-null-dscatalog-df-pf-null-wwe>  
5962-89615012A - <http://www.ti.com/product/5962-89615012a?HQS=TI-null-null-dscatalog-df-pf-null-wwe>  
59628961501VXA - <http://www.ti.com/product/59628961501vxa?HQS=TI-null-null-dscatalog-df-pf-null-wwe>  
5962-8961501VPA - <http://www.ti.com/product/5962-8961501vpa?HQS=TI-null-null-dscatalog-df-pf-null-wwe>  
5962-8961501QXA - <http://www.ti.com/product/5962-8961501qxa?HQS=TI-null-null-dscatalog-df-pf-null-wwe>  
5962F8961501QXA - <http://www.ti.com/product/5962f8961501qxa?HQS=TI-null-null-dscatalog-df-pf-null-wwe>  
5962F8961501QPA - <http://www.ti.com/product/5962f8961501qpa?HQS=TI-null-null-dscatalog-df-pf-null-wwe>  
5962F8961501VHA - <http://www.ti.com/product/5962f8961501vha?HQS=TI-null-null-dscatalog-df-pf-null-wwe>  
5962-8961501PA - <http://www.ti.com/product/5962-8961501pa?HQS=TI-null-null-dscatalog-df-pf-null-wwe>  
5962F8961501VXA - <http://www.ti.com/product/5962f8961501vxa?HQS=TI-null-null-dscatalog-df-pf-null-wwe>  
59628961501VHA - <http://www.ti.com/product/59628961501vha?HQS=TI-null-null-dscatalog-df-pf-null-wwe>  
DS16F95J - <http://www.ti.com/product/ds16f95j?HQS=TI-null-null-dscatalog-df-pf-null-wwe>  
DS16F95 MWA - [http://www.ti.com/product/ds16f95\\_mwa?HQS=TI-null-null-dscatalog-df-pf-null-wwe](http://www.ti.com/product/ds16f95_mwa?HQS=TI-null-null-dscatalog-df-pf-null-wwe)  
5962F8961501QHA - <http://www.ti.com/product/5962f8961501qha?HQS=TI-null-null-dscatalog-df-pf-null-wwe>  
DS16F95 MDA - [http://www.ti.com/product/ds16f95\\_mda?HQS=TI-null-null-dscatalog-df-pf-null-wwe](http://www.ti.com/product/ds16f95_mda?HQS=TI-null-null-dscatalog-df-pf-null-wwe)



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