

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4731B; HEF4731V**

### **LSI**

## **Quadruple 64-bit static shift register**

Product specification  
File under Integrated Circuits, IC04

January 1995

# Quadruple 64-bit static shift register

## HEF4731B; HEF4731V LSI

### DESCRIPTION

The HEF4731B and HEF4731V are quadruple 64-bit static shift registers each with separate serial data inputs ( $D_A$  to  $D_D$ ), clock inputs ( $\overline{CP}_A$  to  $\overline{CP}_D$ ) and data outputs ( $O_{63A}$  to  $O_{63D}$ ) from the 64th register position.

Recommended supply voltage range for HEF4731B is 3 to 15 V and for HEF4731V is 4,5 to 12,5 V.

Data are shifted to the next stage on the negative-going transitions of the clock. Low impedance outputs are provided for direct interface to TTL.

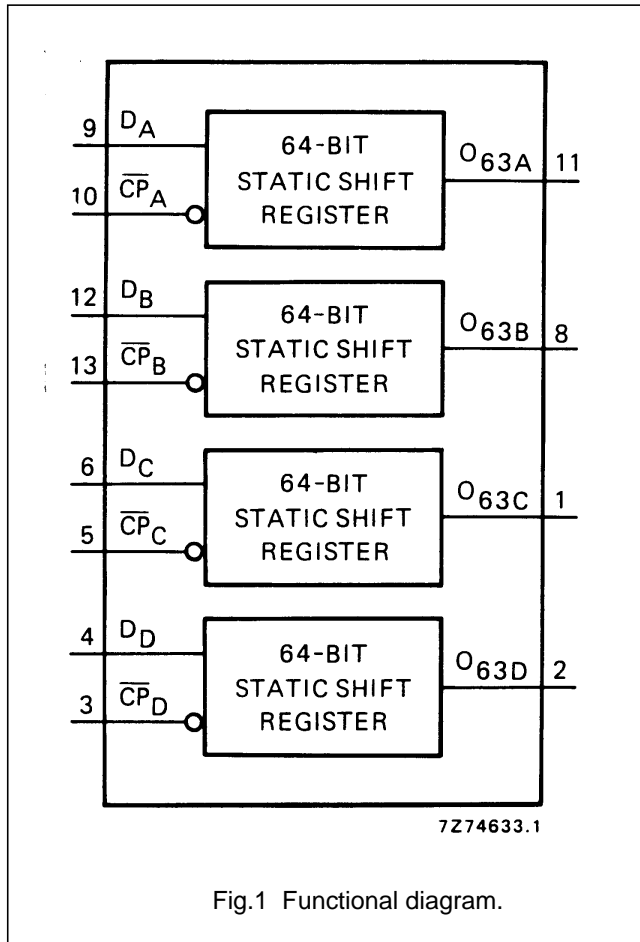


Fig.1 Functional diagram.

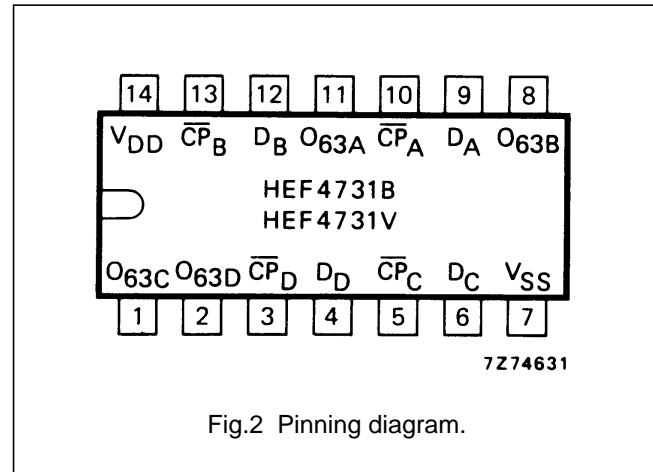


Fig.2 Pinning diagram.

HEF4731BP;            14-lead DIL; plastic  
HEF4731VP(N):      (SOT27-1)

HEF4731BD;            14-lead DIL; ceramic (cerdip)  
HEF4731VD(F):      (SOT73)

( ): Package Designator North America

### FAMILY DATA, I<sub>DD</sub> LIMITS category LSI

See Family Specifications

Quadruple 64-bit static shift register

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LSI

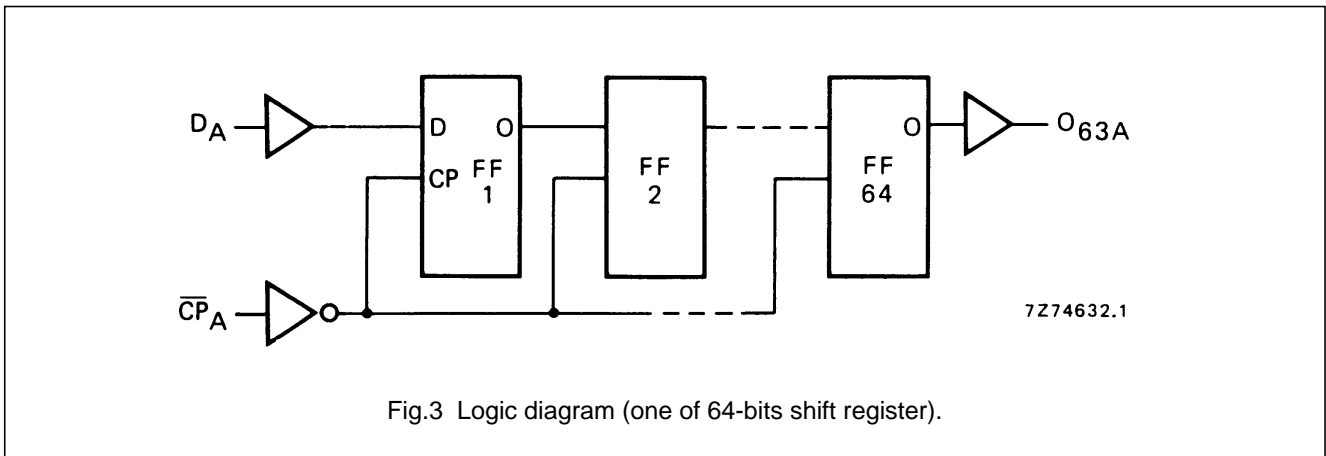


Fig.3 Logic diagram (one of 64-bits shift register).

The values given at  $V_{DD} = 15\text{ V}$  in the following DC and AC characteristics, are not applicable to the HEF4731V, because of its reduced supply voltage range.

**DC CHARACTERISTICS**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$

	$V_{DD}$ V	$V_{OL}$ V	$V_{OH}$ V	SYMBOL	$T_{amb} (\text{°C})$						
					-40		+ 25		+ 85		
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Output (source) current HIGH	5		2,5	$-I_{OH}$	3		2,5		2,0		mA
	5		4,6		1		0,85		0,65		mA
	10		9,5		3		2,5		2,0		mA
	15		13,5		10		8,5		6,5		mA
Output (sink) current LOW	4,75	0,4		$I_{OL}$	2,3		2,0		1,6		mA
	10	0,5			6,0		5,0		4,0		mA
	15	1,5			20,0		18,0		14,0		mA

**AC CHARACTERISTICS**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; input transition times  $\leq 20\text{ ns}$

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu\text{W}$ )	
Dynamic power dissipation per package (P)	5	$13\ 000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
	10	$55\ 000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$140\ 000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	

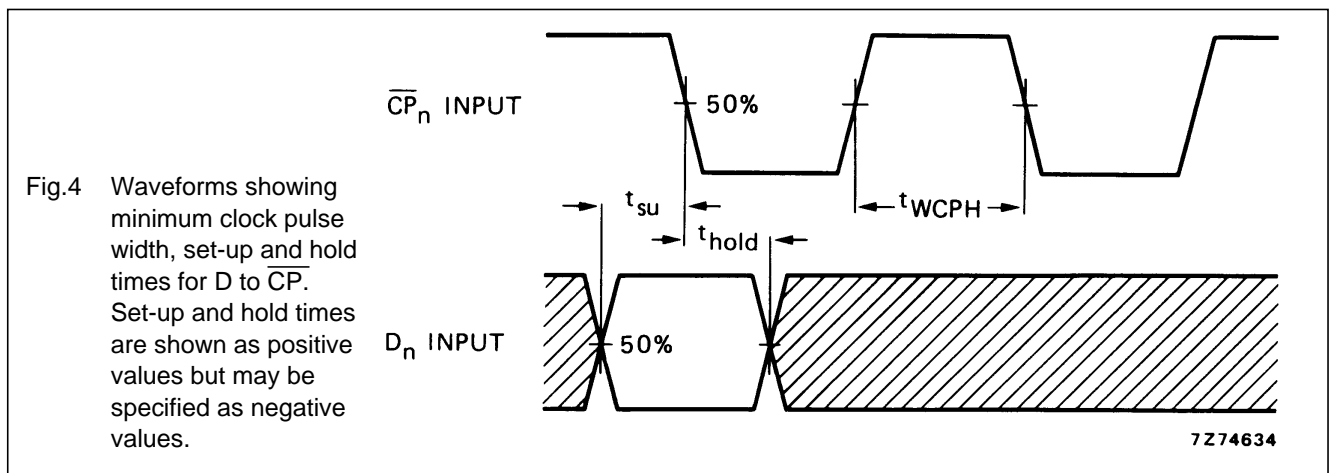
Quadruple 64-bit static shift register

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LSI

AC CHARACTERISTICS

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $\overline{CP} \rightarrow O_{63}$ HIGH to LOW	5	$t_{PHL}$		115	230 ns	$132\text{ ns} + (0,26\text{ ns/pF}) C_L$	
	10		55	110 ns	$47\text{ ns} + (0,16\text{ ns/pF}) C_L$		
	15		40	80 ns	$34\text{ ns} + (0,11\text{ ns/pF}) C_L$		
	LOW to HIGH	5	$t_{PLH}$		130	260 ns	$138\text{ ns} + (0,45\text{ ns/pF}) C_L$
		10		65	130 ns	$56\text{ ns} + (0,19\text{ ns/pF}) C_L$	
		15		45	90 ns	$39\text{ ns} + (0,13\text{ ns/pF}) C_L$	
Transition times $O_{63}$ HIGH to LOW	5	$t_{THL}$		30	60 ns	$10\text{ ns} + (0,40\text{ ns/pF}) C_L$	
	10		12	24 ns	$3\text{ ns} + (0,18\text{ ns/pF}) C_L$		
	15		10	20 ns	$3\text{ ns} + (0,13\text{ ns/pF}) C_L$		
	LOW to HIGH	5	$t_{TLH}$		40	80 ns	$8\text{ ns} + (0,65\text{ ns/pF}) C_L$
		10		20	40 ns	$5\text{ ns} + (0,30\text{ ns/pF}) C_L$	
		15		15	30 ns	$5\text{ ns} + (0,20\text{ ns/pF}) C_L$	
Minimum clock pulse width; HIGH	5	$t_{WCPH}$	200	80	ns	see also waveforms Fig.4	
	10		75	30	ns		
	15		50	20	ns		
Set-up time $D \rightarrow \overline{CP}$	5	$t_{su}$	25	-5	ns		
	10		15	-5	ns		
	15		15	-5	ns		
Hold time $D \rightarrow \overline{CP}$	5	$t_{hold}$	50	20	ns		
	10		30	10	ns		
	15		20	5	ns		
Maximum clock pulse frequency	5	$f_{max}$	2.25	6	MHz	Note: the maximum power dissipation has to be observed	
	10		6	16	MHz		
	15		9	25	MHz		





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