

Integrated Device Technology, Inc.

FAST CMOS OCTAL FLIP-FLOP WITH MASTER RESET

IDT54/74FCT273
IDT54/74FCT273A
IDT54/74FCT273C

FEATURES:

- IDT54/74FCT273 equivalent to FAST™ speed;
- **IDT54/74FCT273A 45% faster than FAST**
- **IDT54/74FCT273C 55% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- IOL = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST (5µA max.)
- Octal D flip-flop with Master Reset
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

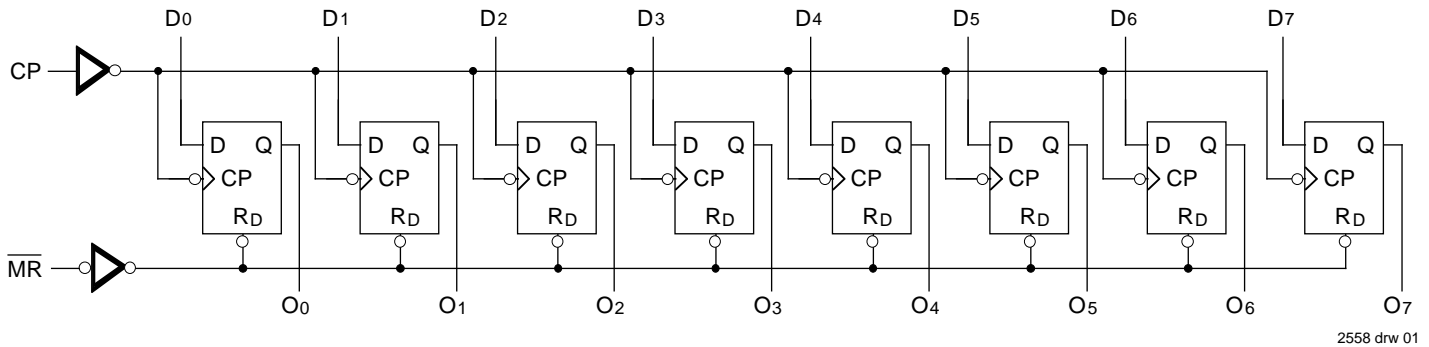
DESCRIPTION:

The IDT54/74FCT273/A/C are octal D flip-flops built using an advanced dual metal CMOS technology. The IDT54/74FCT273/A/C have eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

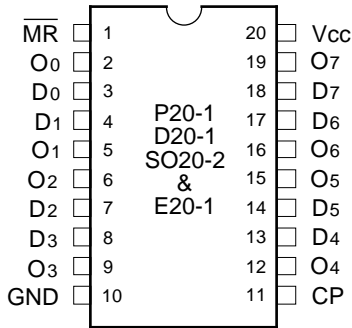
The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

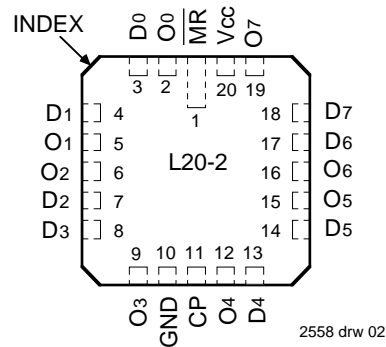
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



**DIP/SOIC/CERPACK
TOP VIEW**



**LCC
TOP VIEW**

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 1992

PIN DESCRIPTION

Pin Names	Description
DN	Data Input
$\overline{\text{MR}}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
ON	Data Outputs

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FUNCTION TABLE

Operating Mode	Inputs			Outputs
	$\overline{\text{MR}}$	CP	DN	ON
Reset (Clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

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NOTES:

H = HIGH voltage level steady-state

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition

L = LOW voltage level steady state

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

X = Don't care

↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
$V_{\text{TERM}}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
$V_{\text{TERM}}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_{A}	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_{T}	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Outputs and I/O terminals only.

CAPACITANCE ($T_{\text{A}} = +25^{\circ}\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{\text{IN}} = 0\text{V}$	6	10	pF
C_{OUT}	Output Capacitance	$V_{\text{OUT}} = 0\text{V}$	8	12	pF

NOTE:

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- This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^{\circ}C$ to $+70^{\circ}C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55^{\circ}C$ to $+125^{\circ}C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V	
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$ $V_I = V_{CC}$ $V_I = 2.7V$ $V_I = 0.5V$ $V_I = GND$	—	—	5	μA	
I_{IL}	Input LOW Current		—	—	$5^{(4)}$		
			—	—	$-5^{(4)}$		
			—	—	-5		
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18mA$	—	-0.7	-1.2	V	
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = GND$	-60	-120	—	mA	
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OH} = -32\mu A$	V_{HC}	V_{CC}	—	V	
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -300\mu A$	V_{HC}	V_{CC}		—
			$I_{OH} = -12mA \text{ MIL.}$	2.4	4.3		—
			$I_{OH} = -15mA \text{ COM'L.}$	2.4	4.3		—
V_{OL}	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OL} = 300\mu A$	—	GND	V_{LC}	V	
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 300\mu A$	—	GND		$V_{LC}^{(4)}$
			$I_{OL} = 32mA \text{ MIL.}$	—	0.3		0.5
			$I_{OL} = 48mA \text{ COM'L.}$	—	0.3		0.5

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0V$, $+25^{\circ}C$ ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
I _{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$	—	0.2	1.5	mA	
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$	—	0.5	2.0	mA	
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{MR} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/MHz
I _C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{MR} = V_{CC}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2.2	6.0		
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{MR} = V_{CC}$ Eight Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8 ⁽⁵⁾	
		$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.2	16.8 ⁽⁵⁾		

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, +25°C ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \text{DHNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 DH = Duty Cycle for TTL Inputs High
 NT = Number of TTL Inputs at DH
 I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	IDT54/74FCT273				IDT54/74FCT273A				IDT54/74FCT273C				Unit	
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.			
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.		
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	5.8	2.0	6.5	ns	
tPHL	Clock to Output															
tPHL	Propagation Delay MR to Output		2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	6.1	2.0	6.8	ns	
tsu	Set-up Time HIGH or LOW Data to CP		3.0	—	3.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	
th	Hold Time HIGH or LOW Data to CP		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	
tw	Clock Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns	
tw	MR Pulse Width LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns	
tREM	Recovery Time MR to CP	4.0	—	5.0	—	2.0	—	2.5	—	2.0	—	2.5	—	ns		

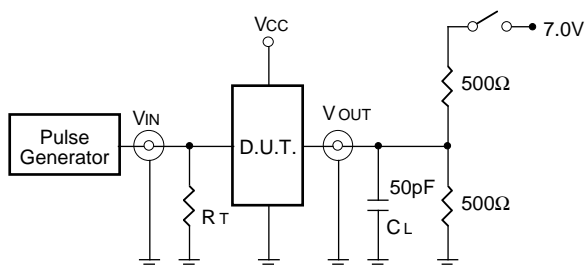
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2558 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

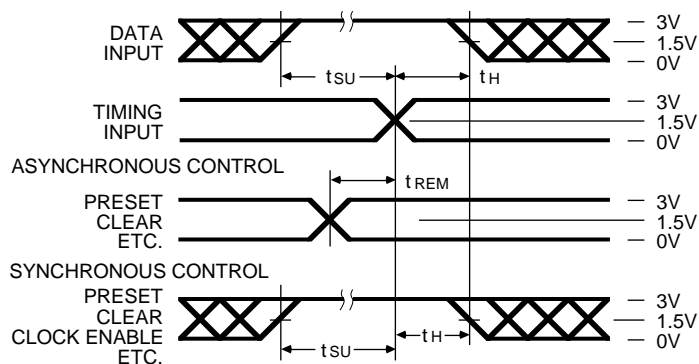
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

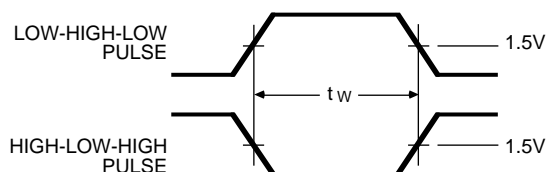
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

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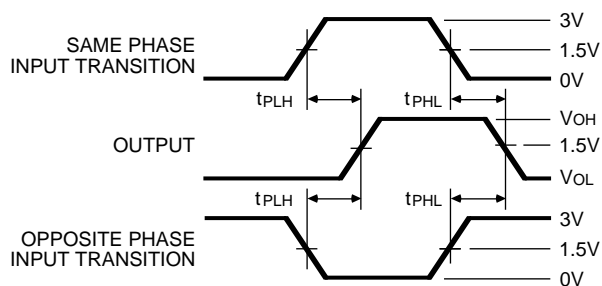
SET-UP, HOLD AND RELEASE TIMES



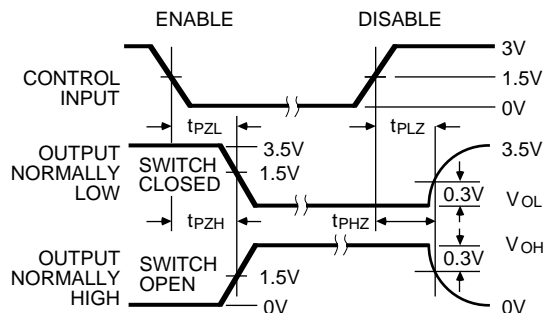
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

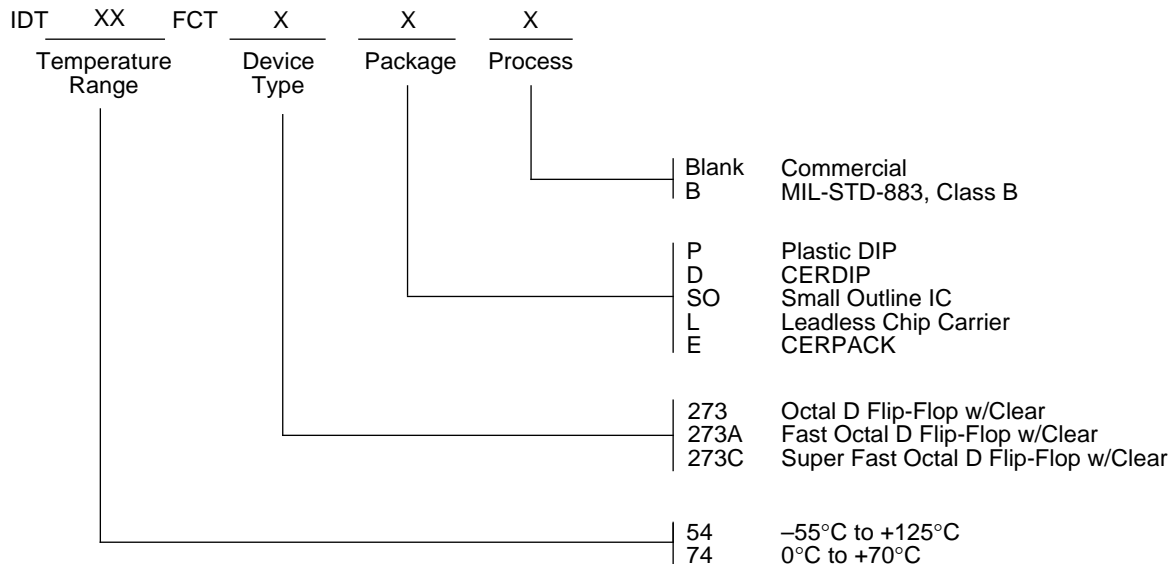


NOTES

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $Z_o \leq 50\Omega$; $t_f \leq 2.5$ ns; $t_r \leq 2.5$ ns.

2558 drw 04

ORDERING INFORMATION



2558 drw 03

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