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# HD74AC273

Octal D Flip-Flop

# HITACHI

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## Description

The HD74AC273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ( $\overline{MR}$ ) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flops's Q output

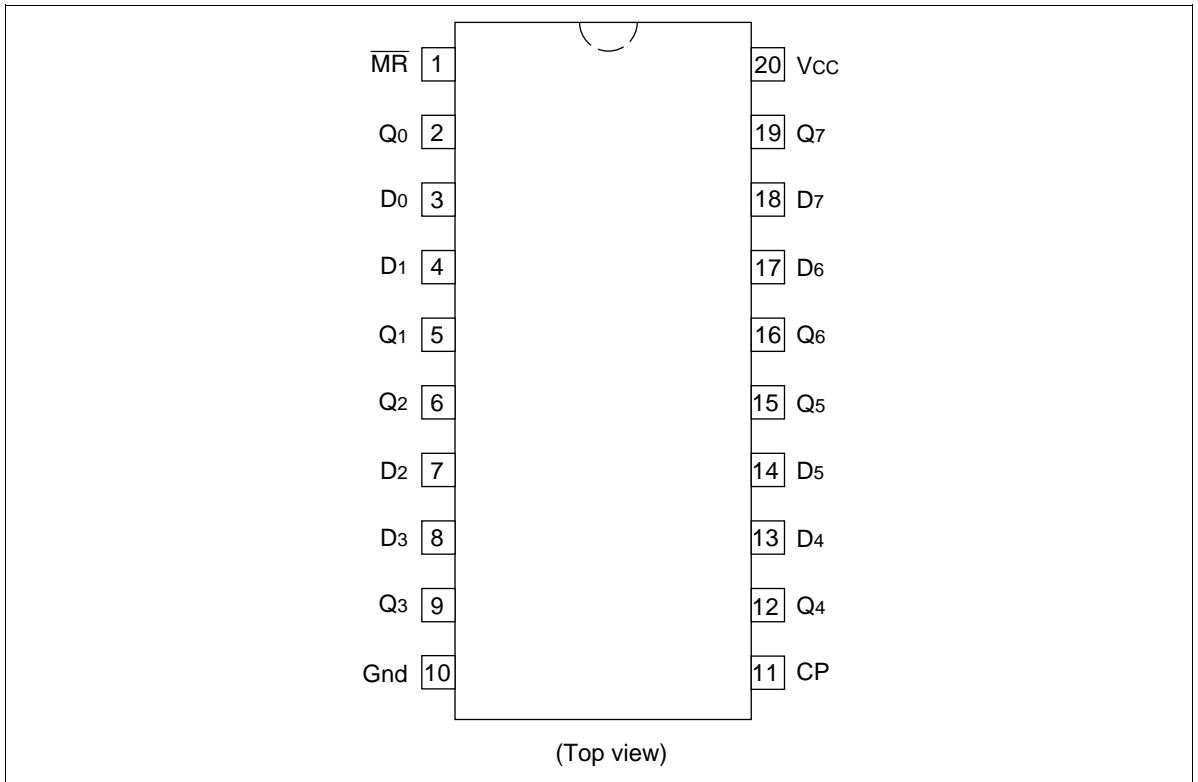
All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the  $\overline{MR}$  input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

## Features

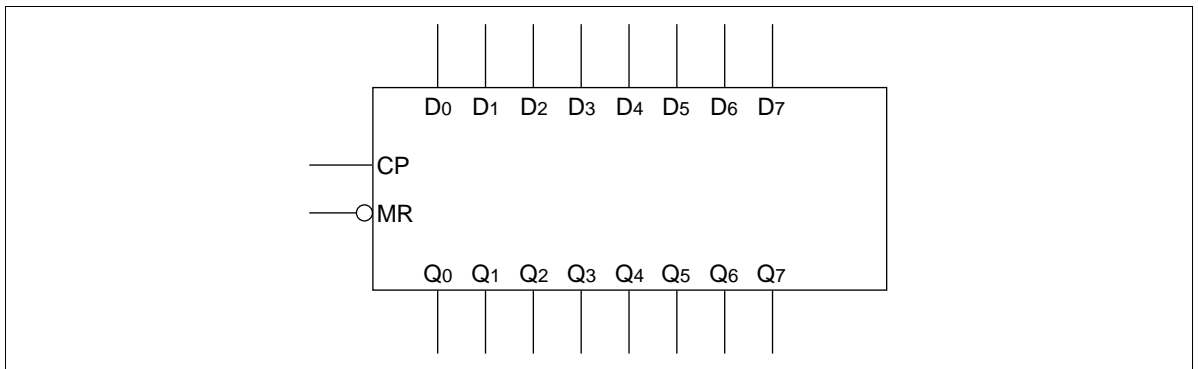
- Ideal Buffer for MOS Microprocessor or Memory
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- Buffered, Asynchronous Master Reset
- See HD74AC373 for Transparent Latch Version
- See HD74AC374 for 3-State Version
- Outputs Source/Sink 24 mA

# HD74AC273

## Pin Arrangement



## Logic Symbol

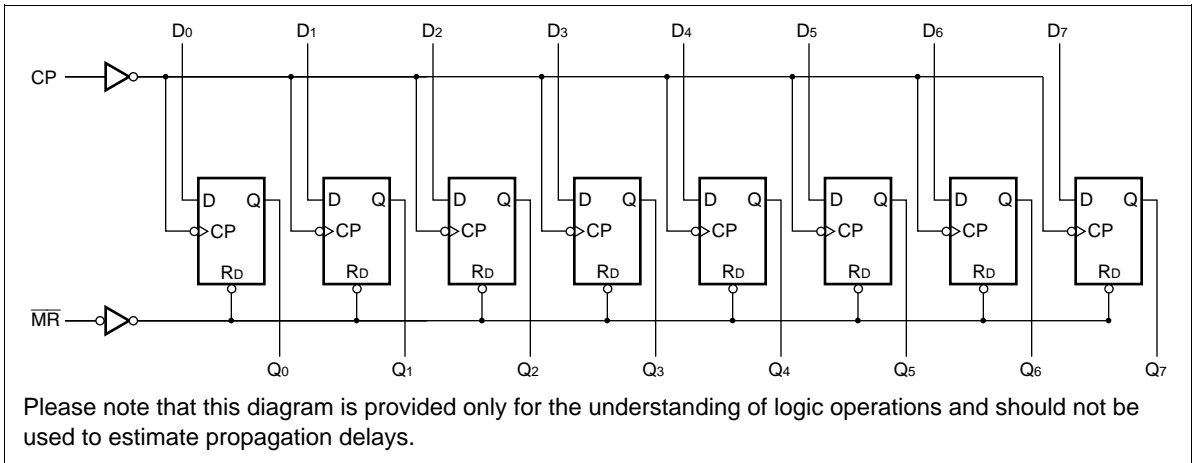


## Pin Names

- D<sub>0</sub> – D<sub>7</sub> Data Inputs
- $\overline{MR}$  Master Reset
- CP Clock Pulse Input
- Q<sub>0</sub> – Q<sub>7</sub> Data Outputs

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**Logic Diagram**



**Mode Select-Truth Table**

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	$D_n$	$Q_n$
Reset (Clear)	L	X	X	L
Load "1"	H		H	H
Load "0"	H		L	L

H : High Voltage Level  
 L : Low Voltage Level  
 X : Immaterial  
 : Low-to-High Clock Transition

**DC Characteristics (unless otherwise specified)**

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	$I_{CC}$	80	$\mu A$	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$ , $T_a = \text{Worst case}$
Maximum quiescent supply current	$I_{CC}$	8.0	$\mu A$	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$ , $T_a = 25^\circ C$

# HD74AC273

## AC Characteristics: HD74AC273

Item	Symbol	V <sub>CC</sub> (V)* <sup>1</sup>	Ta = +25°C C <sub>L</sub> = 50 pF			Ta = -40°C to +85°C C <sub>L</sub> = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f <sub>max</sub>	3.3	90	125	—	75	—	MHz
		5.0	140	175	—	125	—	
Propagation delay Clock to output	t <sub>PLH</sub>	3.3	1.0	7.0	12.5	1.0	14.0	ns
		5.0	1.0	5.5	9.0	1.0	10.0	
Propagation delay Clock to output	t <sub>PHL</sub>	3.3	1.0	7.0	13.0	1.0	14.5	ns
		5.0	1.0	5.0	10.0	1.0	11.0	
Propagation delay MR to output	t <sub>PHL</sub>	3.3	1.0	7.0	13.0	1.0	14.0	ns
		5.0	1.0	5.0	10.0	1.0	10.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

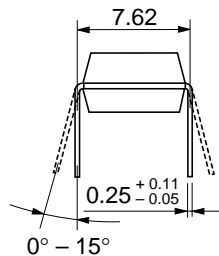
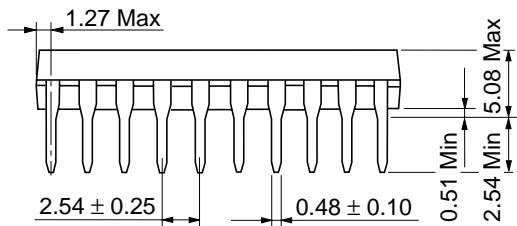
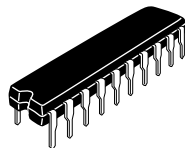
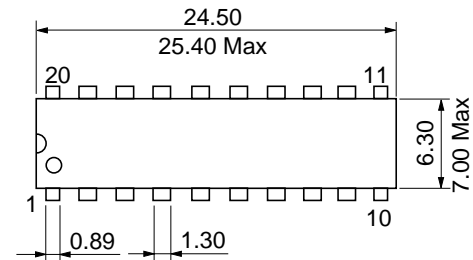
## AC Operating Requirements: HD74AC273

Item	Symbol	V <sub>CC</sub> (V)* <sup>1</sup>	Typ	Guaranteed Minimum		Unit
			Ta = +25°C C <sub>L</sub> = 50 pF			
Setup time, HIGH or LOW Data to CP	t <sub>su</sub>	3.3	3.5	5.5	6.0	ns
		5.0	2.5	4.0	4.5	
Hold time, HIGH or LOW Data to CP	t <sub>h</sub>	3.3	-2.0	0.0	0.0	ns
		5.0	-1.0	1.0	1.0	
Clock pulse width HIGH or LOW	t <sub>w</sub>	3.3	3.5	5.5	6.0	ns
		5.0	2.5	4.0	4.5	
MR Pulse width HIGH or LOW	t <sub>w</sub>	3.3	2.0	5.5	6.0	ns
		5.0	1.5	4.0	4.5	
Recovery time MR to CP	t <sub>rec</sub>	3.3	1.5	3.5	4.5	ns
		5.0	1.0	2.0	3.0	

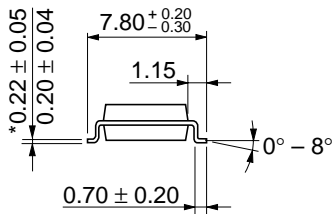
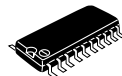
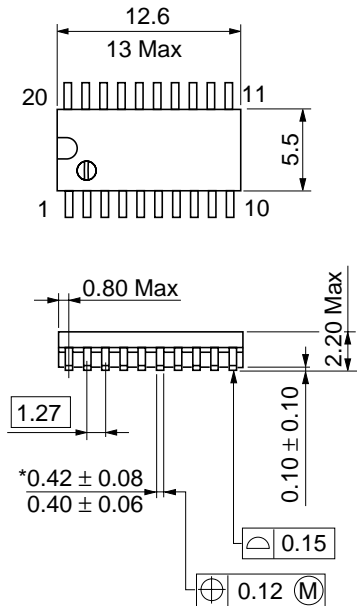
Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

**Capacitance**

<b>Item</b>	<b>Symbol</b>	<b>Typ</b>	<b>Unit</b>	<b>Condition</b>
Input capacitance	$C_{IN}$	4.5	pF	$V_{CC} = 5.5 \text{ V}$
Power dissipation capacitance	$C_{PD}$	50.0	pF	$V_{CC} = 5.0 \text{ V}$

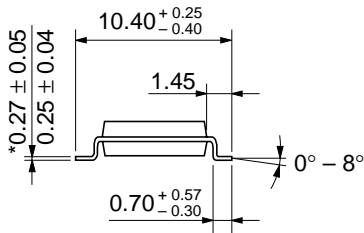
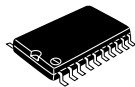
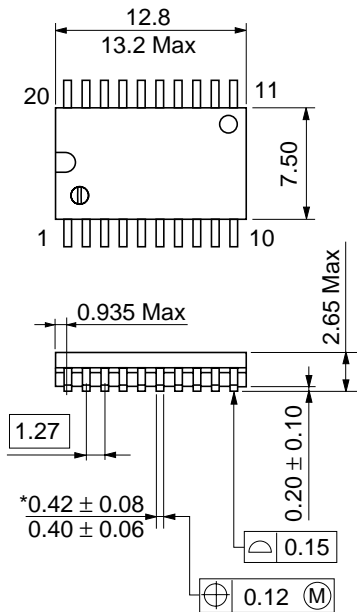


Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g



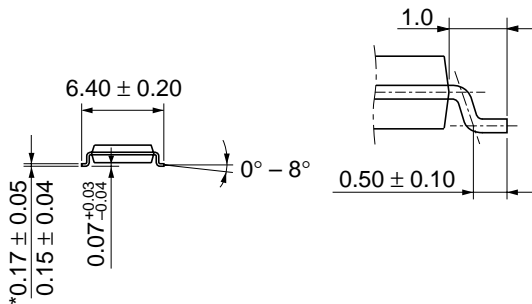
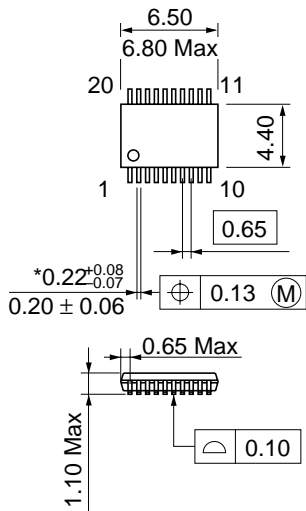
Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g

\*Dimension including the plating thickness  
Base material dimension



Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

\*Dimension including the plating thickness  
 Base material dimension



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g

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