

# 9-bit D-type flip-flop with reset and enable (3-State)

## 74ABT823

### FEATURES

- High speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/−32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up Reset

### DESCRIPTION

The 74ABT823 Bus interface Register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT823 is a 9-bit wide buffered register with Clock Enable ( $\overline{CE}$ ) and Master Reset ( $\overline{MR}$ ) which are ideal for parity bus interfacing in high microprogrammed systems.

The register is fully edge-triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

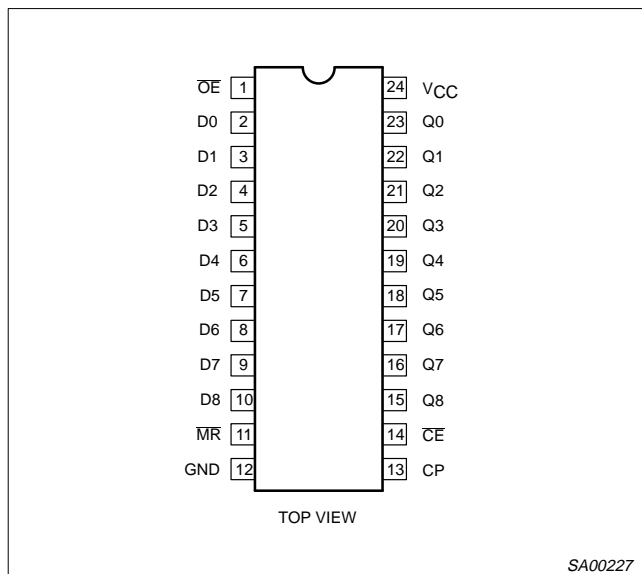
### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay CP to Qn	$C_L = 50\text{pF}; V_{CC} = 5\text{V}$	4.4	ns
$C_{IN}$	Input capacitance	$V_I = 0\text{V}$ or $V_{CC}$	4	pF
$C_{OUT}$	Output capacitance	Outputs disabled; $V_O = 0\text{V}$ or $V_{CC}$	7	pF
$I_{CCZ}$	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	500	nA

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	−40°C to +85°C	74ABT823 N	74ABT823 N	SOT222-1
24-Pin plastic SO	−40°C to +85°C	74ABT823 D	74ABT823 D	SOT137-1
24-Pin Plastic SSOP Type II	−40°C to +85°C	74ABT823 DB	74ABT823 DB	SOT340-1
24-Pin Plastic TSSOP Type I	−40°C to +85°C	74ABT823 PW	74ABT823PW DH	SOT355-1

### PIN CONFIGURATION



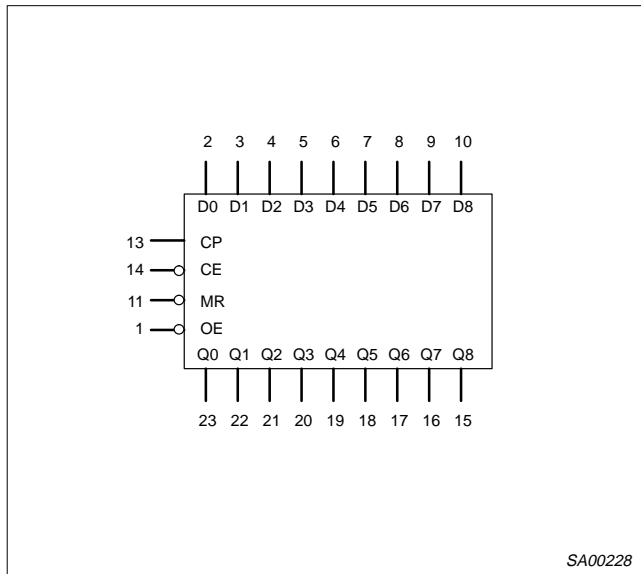
### PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10	D0-D8	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15	Q0-Q8	Data outputs
13	CP	Clock pulse input (active rising edge)
14	$\overline{CE}$	Clock enable input (active-Low)
11	$\overline{MR}$	Master reset input (active-Low)
12	GND	Ground (0V)
24	$V_{CC}$	Positive supply voltage

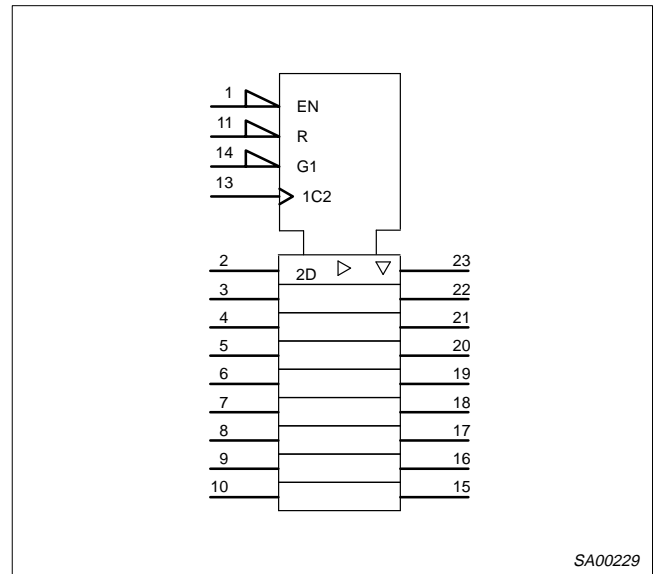
# 9-bit D-type flip-flop with reset and enable (3-State)

74ABT823

## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



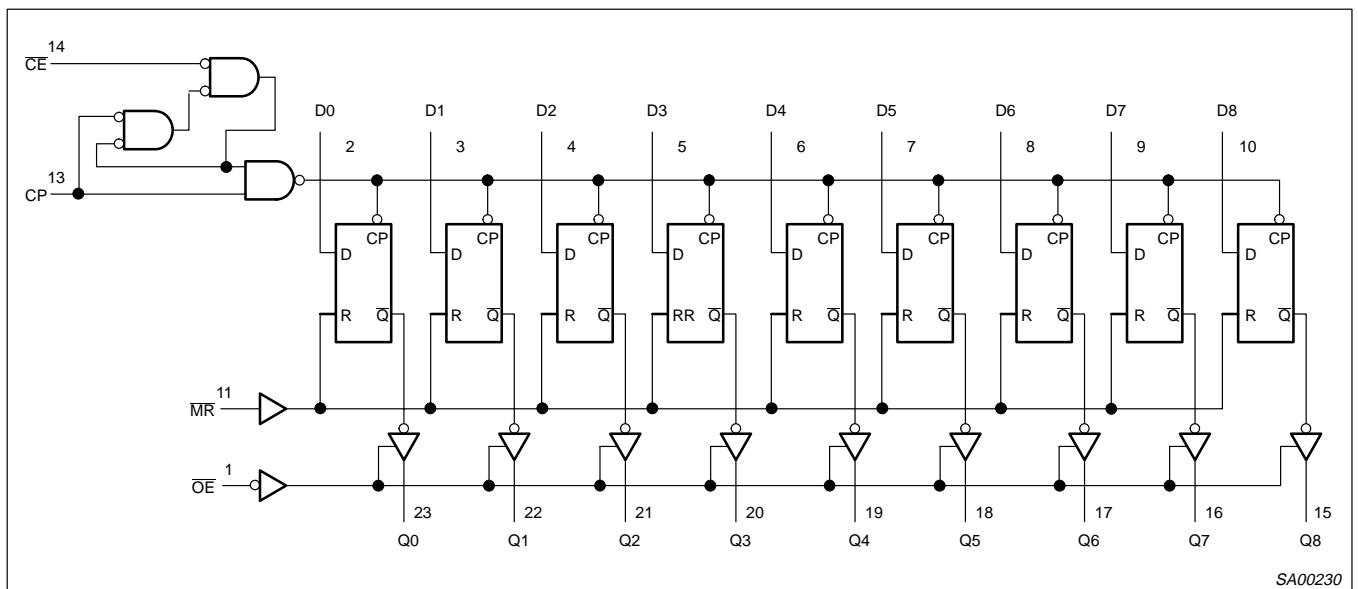
## FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
OE	MR	CE	CP	Dn	Q0 – Q8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	↑	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level  
 h = High voltage level one set-up time prior to the Low-to-High clock transition  
 L = Low voltage level  
 l = Low voltage level one set-up time prior to the Low-to-High clock transition

NC = No change  
 X = Don't care  
 Z = High impedance "off" state  
 ↑ = Low to High clock transition  
 † = Not a Low-to-High clock transition

## LOGIC DIAGRAM



# 9-bit D-type flip-flop with reset and enable (3-State)

74ABT823

## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$I_{IK}$	DC input diode current	$V_I < 0$	-18	mA
$V_I$	DC input voltage <sup>3</sup>		-1.2 to +7.0	V
$I_{OK}$	DC output diode current	$V_O < 0$	-50	mA
$V_{OUT}$	DC output voltage <sup>3</sup>	output in Off or High state	-0.5 to +5.5	V
$I_{OUT}$	DC output current	output in Low state	128	mA
$T_{stg}$	Storage temperature range		-65 to 150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_{IH}$	High-level input voltage	2.0		V
$V_{IL}$	Low-level input voltage		0.8	V
$I_{OH}$	High-level output current		-32	mA
$I_{OL}$	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
$T_{amb}$	Operating free-air temperature range	-40	+85	°C

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74ABT823

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5V; I <sub>IK</sub> = -18mA		-0.9	-1.2		-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.5	2.9		2.5		V
		V <sub>CC</sub> = 5.0V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	3.0	3.4		3.0		V
		V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -32mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.0	2.4		2.0		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OL</sub> = 64mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		0.42	0.55		0.55	V
V <sub>RST</sub>	Power-up output low voltage <sup>3</sup>	V <sub>CC</sub> = 5.5V; I <sub>O</sub> = 1mA; V <sub>I</sub> = GND or V <sub>CC</sub>		0.13	0.55		0.55	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or 5.5V		±0.01	±1.0		±1.0	μA
I <sub>OFF</sub>	Power-off leakage current	V <sub>CC</sub> = 0.0V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5V		±5.0	±100		±100	μA
I <sub>PU</sub> /I <sub>PD</sub>	Power-up/down 3-State output current <sup>4</sup>	V <sub>CC</sub> = 2.0V; V <sub>O</sub> = 0.5V; V <sub>OE</sub> = V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub>		±5.0	±50		±50	μA
I <sub>OZH</sub>	3-State output High current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.7V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		5.0	50		50	μA
I <sub>OZL</sub>	3-State output Low current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		-5.0	-50		-50	μA
I <sub>CEX</sub>	Output High leakage current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 5.5V; V <sub>I</sub> = GND or V <sub>CC</sub>		5.0	50		50	μA
I <sub>O</sub>	Output current <sup>1</sup>	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.5V	-50	-100	-180	-50	-180	mA
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 5.5V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub>		0.5	250		250	μA
I <sub>CCL</sub>		V <sub>CC</sub> = 5.5V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub>		27	34		34	mA
I <sub>CCZ</sub>		V <sub>CC</sub> = 5.5V; Outputs 3-State; V <sub>I</sub> = GND or V <sub>CC</sub>		0.5	250		250	μA
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 5.5V; one input at 3.4V, other inputs at V <sub>CC</sub> or GND		0.5	1.5		1.5	mA

### NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V<sub>CC</sub> between 0V and 2.1V with a transition time of up to 10msec. For V<sub>CC</sub> = 2.1V to V<sub>CC</sub> = 5V ± 10%, a transition time of up to 100μsec is permitted.

## AC CHARACTERISTICS

GND = 0V, t<sub>R</sub> = t<sub>F</sub> = 2.5ns, C<sub>L</sub> = 50pF, R<sub>L</sub> = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V			T <sub>amb</sub> = -40 to +85°C V <sub>CC</sub> = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	1	125	200		125		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Qn	1	2.1	4.3	5.9	2.1	6.8	ns
			2.2	4.4	6.1	2.2	6.7	
t <sub>PHL</sub>	Propagation delay MR to Qn	2	2.0	4.1	6.3	2.0	7.1	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to High and Low level	4 5	1.0	3.0	4.5	1.0	5.3	ns
			2.2	4.1	5.6	2.2	6.3	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from High and Low level	4 5	2.7	4.8	6.2	2.7	6.9	ns
			2.8	5.0	6.4	2.8	6.9	

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74ABT823

## AC SETUP REQUIREMENTS

GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$

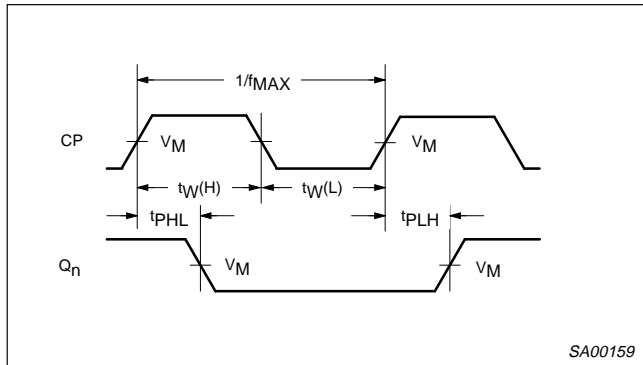
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$	
			Min	Typ	Min	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low Dn to CP	3	2.1 2.1	0.5 0.2	2.1 2.1	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low Dn to CP	3	1.3 1.3	0.0 -0.3	1.3 1.3	ns
$t_w(\text{H})$ $t_w(\text{L})$	CP pulse width High or Low	1	2.9 3.8	1.9 2.8	2.9 3.8	ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low $\overline{\text{CE}}$ to CP	3	2.0 3.3	-0.5 1.5	2.0 3.3	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low $\overline{\text{CE}}$ to CP	3	1.0 2.0	-1.4 0.7	1.0 2.0	ns
$t_w(\text{L})$	MR pulse width, Low	2	5.5	4.0	5.5	ns
$t_{\text{rec}}$	Recovery time MR to CP	2	2.5	0.6	2.5	ns

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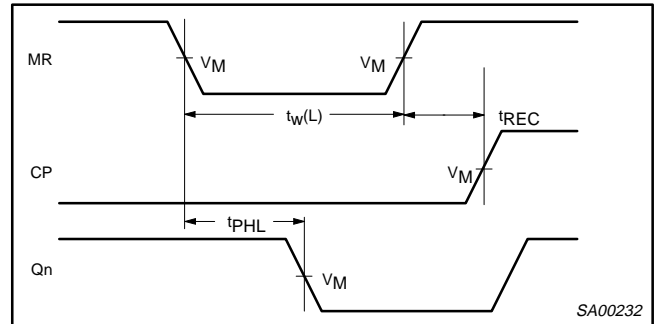
74ABT823

## AC WAVEFORMS

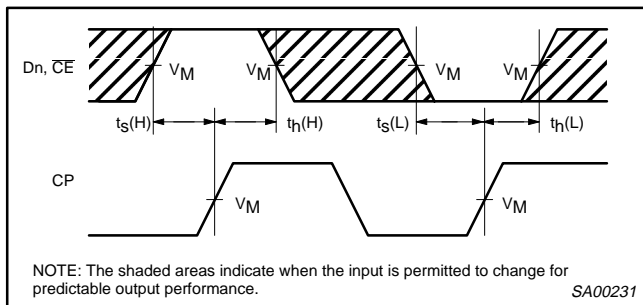
$V_M = 1.5V$ ,  $V_{IN} = GND$  to  $3.0V$



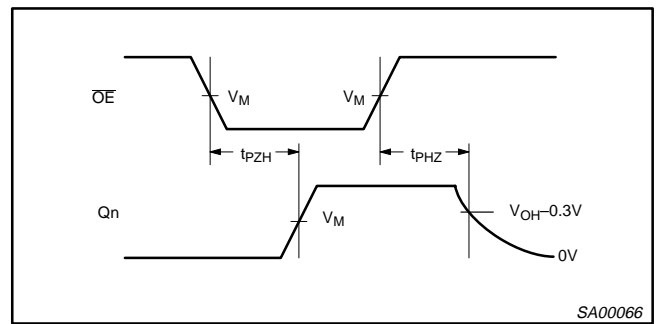
**Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency**



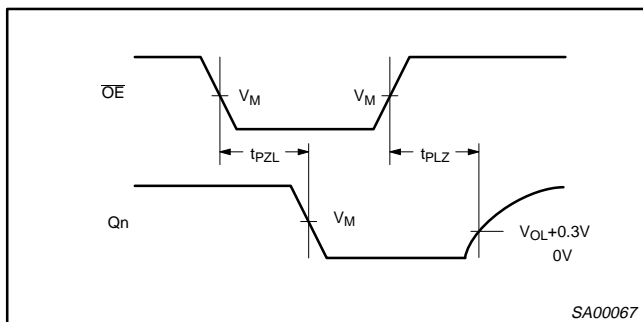
**Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time**



**Waveform 3. Data Setup and Hold Times**



**Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level**

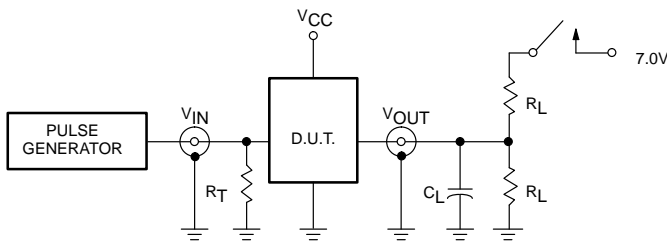


**Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**

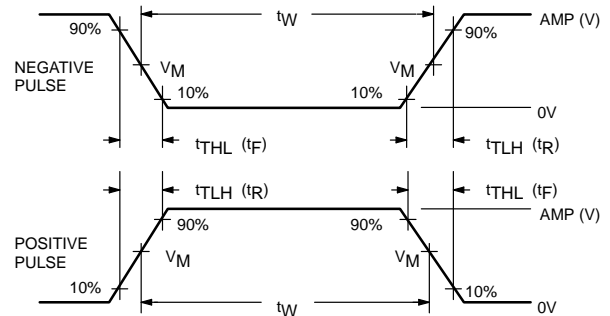
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74ABT823

## TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

### SWITCH POSITION

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

### DEFINITIONS

- $R_L$  = Load resistor; see AC CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_W$	$t_R$	$t_F$
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

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