

# DATA SHEET

## **74F113**

Dual J-K negative edge-triggered  
flip-flops without reset

Product specification

1991 Feb 14

IC15 Data Handbook

# Dual J-K negative edge-triggered flip-flops without reset

74F113

## FEATURE

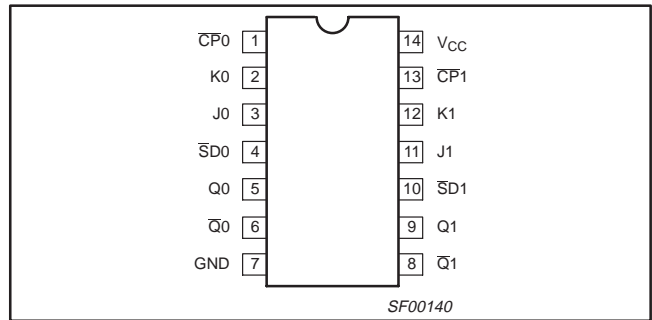
- Industrial temperature range available (−40°C to +85°C)

## DESCRIPTION

The 74F113, dual negative edge-triggered JK-type flip-flop, features individual J, K, clock ( $\overline{CP}$ ), set ( $\overline{SD}$ ) inputs, true and complementary outputs. The asynchronous  $\overline{SD}$  input, when low, forces the outputs to the steady state levels as shown in the function table regardless of the level at the other inputs.

A high level on the clock ( $\overline{CP}$ ) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the  $\overline{CP}$  is high and flip-flop will perform according to the function table as long as minimum setup and hold times are observed. Output changes are initiated by the high-to-low transition of the  $\overline{CP}$ .

## PIN CONFIGURATION



TYPE	TYPICAL $f_{max}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F113	100MHz	15mA

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG. DWG. #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$	
14-pin plastic DIP	N74F113N	I74F113N	SOT27-1
14-pin plastic SO	N74F113D	I74F113D	SOT108-1

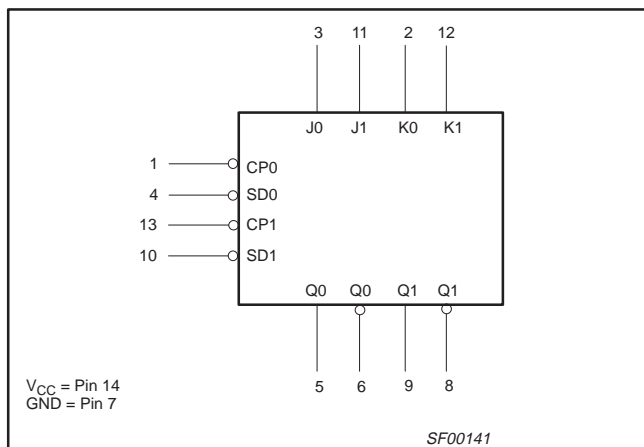
## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J0, J1	J inputs	1.0/1.0	20 $\mu$ A/0.6mA
K0, K1	K inputs	1.0/1.0	20 $\mu$ A/0.6mA
$\overline{CP}$ 0, $\overline{CP}$ 1	Clock inputs (active falling edge)	1.0/4.0	20 $\mu$ A/2.4mA
$\overline{SD}$ 0, $\overline{SD}$ 1	Set inputs (active low)	1.0/5.0	20 $\mu$ A/3.0mA
Q0, Q1, $\overline{Q}$ 0, $\overline{Q}$ 1	Data outputs	50/33	1.0mA/20mA

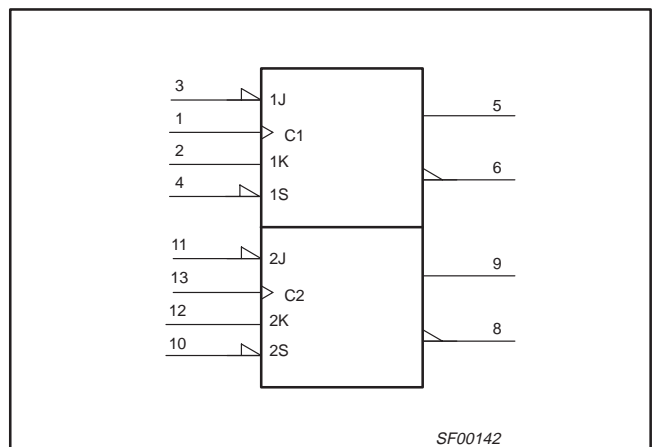
### NOTE:

One (1.0) FAST unit load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

## LOGIC SYMBOL



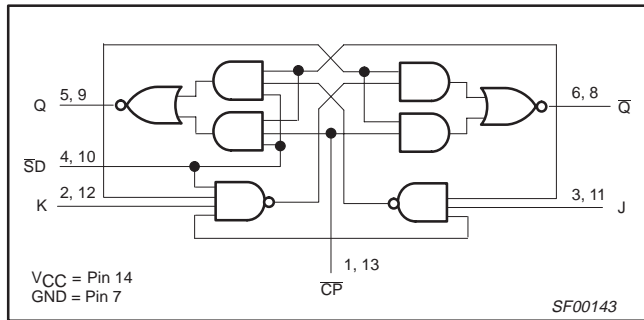
## IEC/IEEE SYMBOL



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## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{CP}$	J	K	Q	$\overline{Q}$	
L	X	X	X	H	L	Asynchronous set
H	↓	h	h	$\overline{q}$	q	Toggle
H	↓	h	l	H	L	Load "1" (set)
H	↓	l	h	L	H	Load "0" (reset)
H	↓	l	l	q	$\overline{q}$	Hold 'no change'

### NOTES:

- H = High-voltage level
- h = High-voltage level one setup time prior to high-to-low clock transition
- L = Low-voltage level
- l = Low-voltage level one setup time prior to high-to-low clock transition
- q = Lower case indicate the state of the referenced output prior to the high-to-low clock transition
- X = Don't care
- ↓ = high-to-low clock transition

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	40	mA
T <sub>amb</sub>	Operating free-air temperature range	Commercial range	0 to +70 °C
		Industrial range	-40 to +85 °C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-1	mA
I <sub>OL</sub>	Low-level output current			20	mA
T <sub>amb</sub>	Operating free-air temperature range	Commercial range	0	+70	°C
		Industrial range	-40	+85	°C

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## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT		
			MIN	TYP <sup>2</sup>	MAX			
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = MAX	±10%V <sub>CC</sub>	2.5		V	
				±5%V <sub>CC</sub>	2.7	3.4	V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.30	0.50	V
				±5%V <sub>CC</sub>		0.30	0.50	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V				100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V				20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V	Jn, Kn				-0.6	mA
			CPn				-2.4	mA
			SDn				-3.0	mA
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX			-60		-150	mA
I <sub>CC</sub>	Supply current <sup>4</sup> (total)	V <sub>CC</sub> = MAX				15	21	mA

### NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
- Measure I<sub>CC</sub> with the clock input grounded and all outputs open, then with Q and  $\bar{Q}$  outputs high in turn.

## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			V <sub>CC</sub> = +5.0V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5.0V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω		V <sub>CC</sub> = +5.0V ± 10% T <sub>amb</sub> = -40°C to +85°C C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
f <sub>max</sub>	Maximum clock frequency	Waveform 1	85	100		80		80		ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CPn to Qn or $\bar{Q}$ n	Waveform 1	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.0	2.0 2.0	7.5 7.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay SDn, to Qn or $\bar{Q}$ n	Waveform 2	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	2.0 2.0	8.0 7.5	ns

## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			V <sub>CC</sub> = +5.0V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5.0V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω		V <sub>CC</sub> = +5.0V ± 10% T <sub>amb</sub> = -40°C to +85°C C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
t <sub>su</sub> (H) t <sub>su</sub> (L)	Setup time, high or low Jn, Kn to CPn	Waveform 1	4.0 3.5			5.0 4.0		5.0 4.5		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, high or low Jn, Kn to CPn	Waveform 1	0.0 0.0			0.0 0.0		0.0 0.0		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP pulse width, high or low	Waveform 1	4.5 4.5			5.0 5.0		5.0 5.0		ns
t <sub>w</sub> (L)	SDn pulse width, low	Waveform 2	4.5			5.0		5.0		ns
t <sub>rec</sub>	Recovery time SDn to CPn	Waveform 2	4.5			5.0		5.0		ns

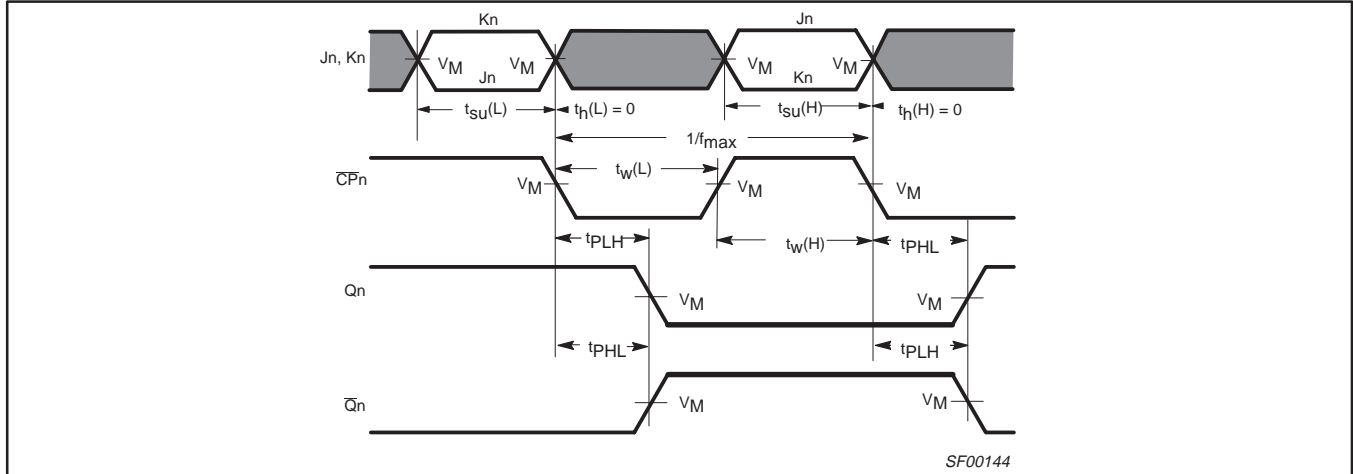
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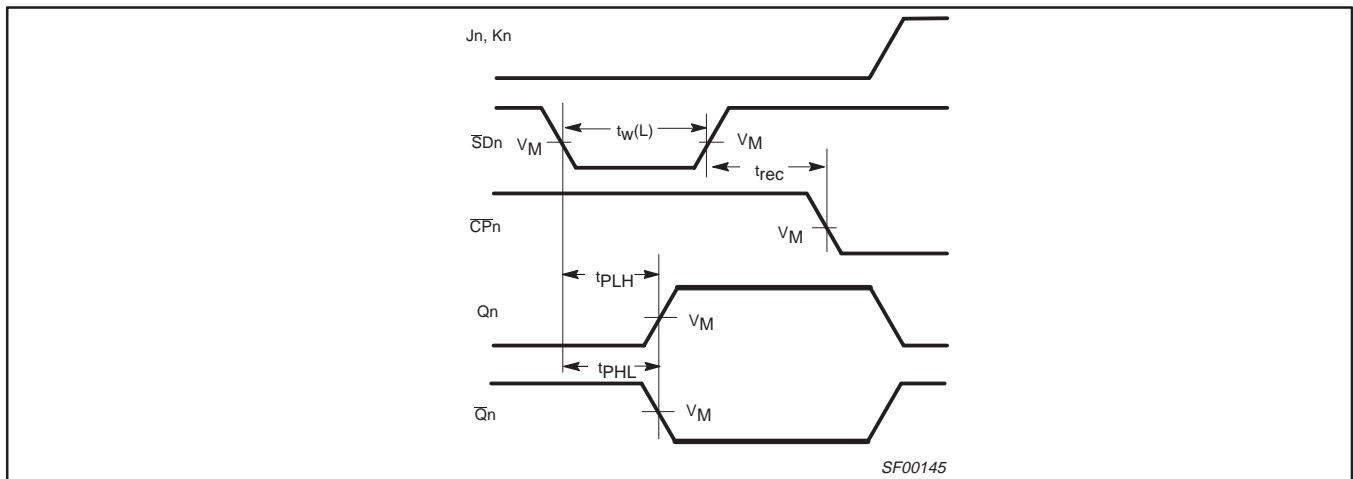
## AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$ .

The shaded areas indicate when the input is permitted to change for predictable output performance.



**Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Times, and Clock Width, and Maximum Clock Frequency**

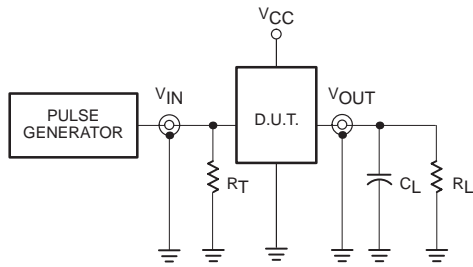


**Waveform 2. Propagation Delay for Set to Output, Set Pulse Width, and Recovery Time for Set to Clock**

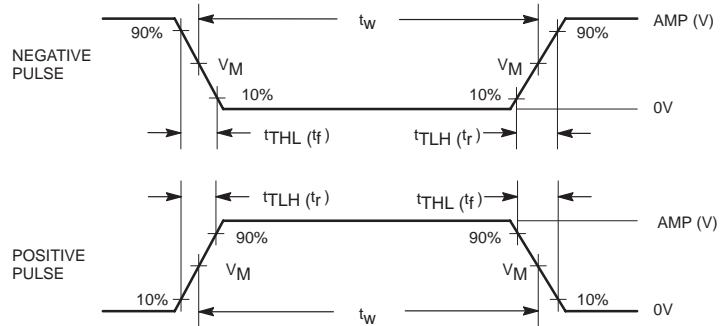
# Dual J-K negative edge-triggered flip-flops without reset

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### TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

**DEFINITIONS:**

- $R_L$  = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

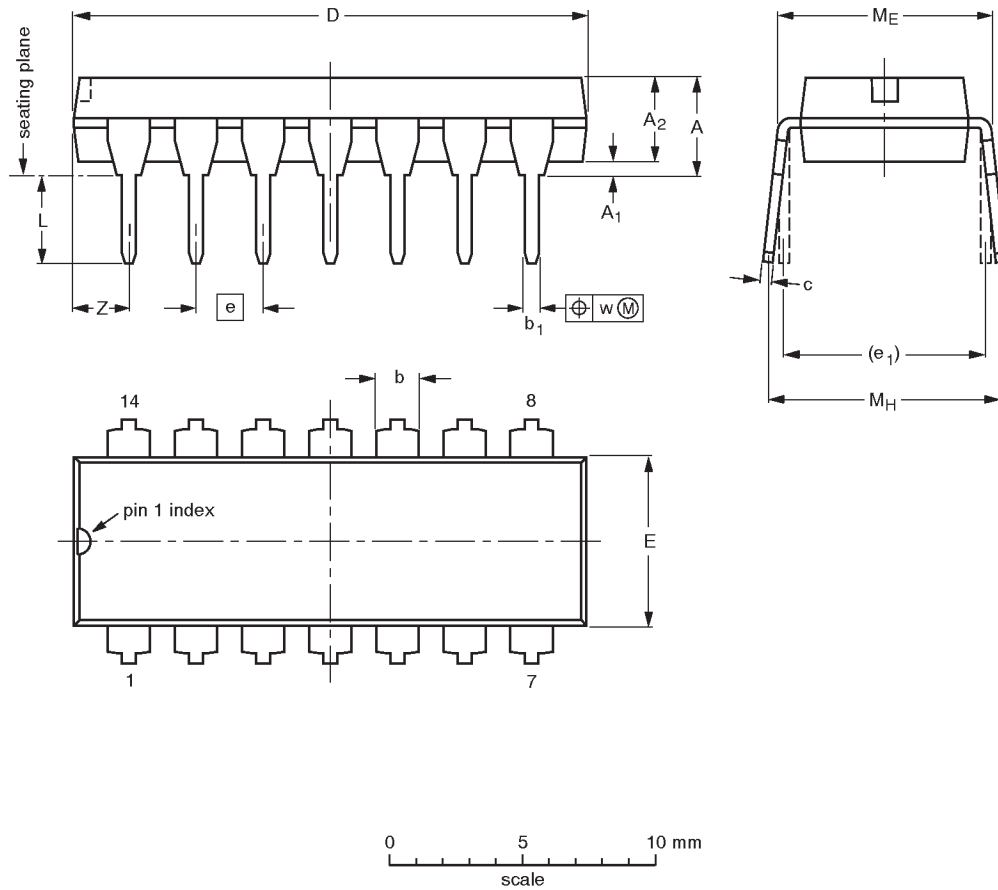
SF00006

# Dual J-K negative edge-triggered flip-flops without reset

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

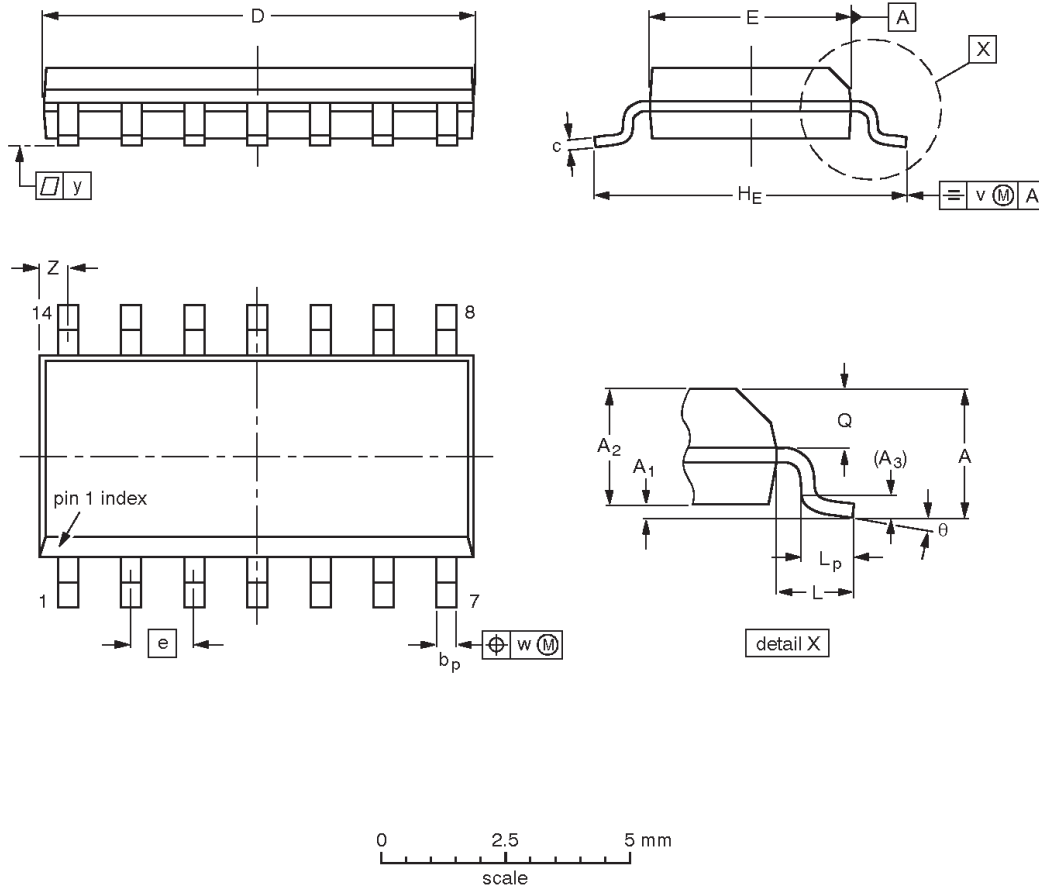
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT27-1	050G04	MO-001AA			92-11-17 95-03-11

# Dual J-K negative edge-triggered flip-flops without reset

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT108-1	076E06S	MS-012AB			95-01-23 97-05-22

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**NOTES**

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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